Agenda

► Who is Analog Devices?

► AD9361 – insights, features

► State of the Art / Improvements
  ▪ Is SDR keeping up with Moore’s law?
  ▪ Peek into the future
Who is Analog Devices?

► Acknowledged industry-wide as the world leader in data conversion and signal conditioning technology, Analog Devices serves over 60,000 customers, representing virtually all types of electronics.

► Founded in 1965 in Cambridge, Massachusetts
► $3 Billion in sales, 9,600 employees, 60,000 customers of all sizes and experience levels
The recognized connectivity leader across the radio spectrum

Offers optimum architectures, both discrete and integrated, that provide flexibility, range, and power efficiency

Solutions that cover a broad range of applications across the frequency spectrum
Analog Devices – not just IC’s anymore!

► Connectorized Modules
  - Amplifiers
  - Attenuators
  - Block Upconverters
  - Dielectric Resonator Oscillators
  - Freq. Dividers & Detectors
  - Freq. Multipliers
  - High Speed Digital Logic
  - MicroSynth
  - Mixers
  - Phase Shifters
  - Successive Detection Log Video Amplifier
  - Switches
  - VCOs

► Signal Generators
  - 10 - 70 GHz Signal Generator
    
    **HMC-T2220**
    10 MHz to 20 GHz
    
    Spurious: -70 dBc @ 10 GHz
    100 kHz Phase Noise -99 @ 10 GHz
    
    $9,998

    **HMC-T2240**
    10 MHz to 40 GHz
    
    Spurious: -70 dBc @ 10 GHz
    100 kHz Phase Noise -99 @ 10 GHz
    
    $19,498

    **HMC-T2220B**
    10 MHz to 20 GHz
    
    Battery Powered!
    Spurious: -60 dBc @ 67 GHz
    100 kHz Phase Noise -98 @ 10 GHz
    
    $14,998

    **HMC-T2270**
    10 MHz to 70 GHz
    
    Spurious: -70 dBc @ 10 GHz
    100 kHz Phase Noise -98 @ 10 GHz
    
    $34,998
What’s the most important thing when picking a chip:

- **The chip itself**: 27% (UBM 2015 embedded study: 42%)
- **The ecosystem surrounding the chip (software, tools, support, etc.)**: 65% (UBM 2015 embedded study: 45%)
- **The chip’s supplier/vendor**: 8% (UBM 2015 embedded study: 13%)

UBM 2015 embedded study: 2,258 respondents, 95% +/- 2%
AD9361 brief intro
Traditional RF Evaluation Platforms (Antenna to Bits, circa 2010)

- Discrete single product evaluation boards, connected with wires
- 6 power supplies
- 4 different USB applications
  - not all compatible, required different PCs
- Not easy to replicate, or use as part of a SDR prototyping solution
FMCOMMS2 – Moore’s Law in action - Now

**AD9361**
RF Agile Transceiver™
70 MHz – 6000 MHz Turning range
200kHz – 56 MHz RF channel Bandwidth

**ADP1755**
Low $V_{in}$ / $V_{out}$ LDO

**ADP2164**
synchronous, step-down dc-to-dc regulator

**AD7291**
8-channel, SAR ADC

**M24C02**
EEPROM

**40 MHz Crystal**

**AD7291**
8-channel, SAR ADC
Housekeeping
ADI General Purpose SDR Boards

**AD-FMCOMMS1**
- Discrete
- 1Rx, 1Tx
- 400 MHz – 4GHz tuning range
- 200+ MHz channel bandwidth
- Shipping Now!

**AD-FMCOMMS2**
- AD9361 Integrated
- 2 x Rx, 2 x Tx
- 2.2 GHz – 2.6GHz tuning range
- 200kHz - 56 MHz channel bandwidth
- Shipping Now!

**AD-FMCOMMS3**
- AD9361 Integrated
- 2 x Rx, 2 x Tx
- 70 MHz – 6GHz tuning range
- 200kHz - 56 MHz channel bandwidth
- Shipping Now!

**AD-FMCOMMS4**
- AD9364 Integrated
- 1 x Rx, 1 x Tx
- 70 MHz – 6GHz tuning range
- 200kHz - 56 MHz channel bandwidth
- Shipping Now!

**AD-FMCOMMS5**
- 2 x AD9361 Integrated
- 4 x Rx, 4 x Tx
- 70 MHz – 6GHz tuning range
- 200kHz - 56 MHz channel bandwidth
- Shipping Now!

**AD-FMCOMMS6**
- Discrete
- Rx only
- Shipping Now!

**FMC FREQ CONVERTER**
- Power, Clocks, ADC, DAC, PLL, DVGA,
- Power, Transceiver

**FMC COMMS BOOSTER**
- Rx LNA (ADL5521)
- Tx Pre-Amp (ADL5610)
- Power (ADP2370, ADP7104)

**ARRADIO from ARROW**
- Power, Clocks, ADC, PLL, LNA
Applications for the AD9361/AD9364 SW-Defined RF Transceiver IC

- Defense electronics
  - Radar, handheld and manpack battlefield radios
- RF test equipment and instrumentation
- Communications and telemetry equipment
- Communications infrastructure
  - Femtocell / picocell / microcell basestations, data card dongles
- General software-defined radio platforms
AD9361 / AD9364 Under the Hood

- **AD9361**: 2 Rx + 2 Tx
- **AD9364**: 1 Rx + 1 Tx

**Major sections:**
- RF input/output paths
- RF PLL/LO (70 – 6000 MHz)
- BB fractional N synthesizer
- Clock generation
- ADC/DAC
- Digital filters
- Digital interface
- Enable state machine
- RX Gain (AGC)
- TX Attenuation
- Aux DAC/ADC and GPOs
- Analog and Digital Correction/Calibration
AD9361 Calibrations

► Initialization Calibrations
  ▪ BBPLL VCO Calibration
  ▪ RF Synthesizer Charge Pump Calibration
  ▪ RF Synthesizer VCO calibration
  ▪ Baseband RX Analog Filter Calibration
  ▪ Baseband TX Analog Filter Calibration
  ▪ Baseband TX Secondary Filter
  ▪ RX TIA Calibration Equations
  ▪ RX ADC Setup
  ▪ Baseband DC Offset Calibration
  ▪ RF DC Offset Calibration
  ▪ RX Quadrature Calibration
  ▪ TX Quadrature Calibration

► Factory Calibrations
  ▪ Internal DCXO
  ▪ TX RSSI (TX Monitor)
  ▪ RX RSSI
  ▪ RX GM / LNA Gain Step Calibration
  ▪ TX Power Out Vs TX Attenuation and TX Power Out Vs Carrier Frequency
Errors in $F_{\text{REF}}$ cause errors in PLL and sample rates.

- Low cost crystals have errors.
  - Accuracy
  - Stability
  - Temperature
  - Doppler

- Use digital tuning to correct errors, to sub ppm.

70MHz to 6GHz operation covers FM radio, ISM Bands, TV whitespace, 2G/3G/4G cellular, WiFi bands… and everything in between!
Fast Lock – it’s fast.

- Typical ‘normal’ calibration plus lock times are on the order of 45-60us, but can be as long as 100ms.
- For many applications – this is way too slow.
- The device includes a Fast Lock mode
  - storing sets of synthesizer programming information (called “profiles”)
  - eliminates most of the overhead of synthesizer programming by allowing up to 8 RX profiles and 8 TX profiles of frequency configuration information (including cal results) to be stored.
  - Need more than 8? Store them off chip.

- 3 GHz “sweep” = 60 LO changes
- 512 samples
- 7.2 fps (screen fresh rate on ZedBoard’s HDMI output)
  - 137.9 ms per 60 LO changes, or 2.3 ms each capture
  - 30720 bins in total
AD9361 Filter Stages

Each filter stage results in some unique amplitude rolloff and group delay in the passband.

Problem:
- How to understand each filter stage effect on:
  - Amplitude rolloff in passband
  - Group delay in passband
- How to design a FIR filter that compensates for effects from previous stages?

-3dB point defines "bandwidth", but still not flat from DC to half of "bandwidth"
AD9361 Multistage Filter
(Analog + Digital + FIR)

- AD9361 analog filters in Tx and Rx chains
- SINC Filter effects from ADC/DAC
- Digital Half Band interpolators & decimators
- FIR design for filtering, equalization and optional additional interpolation & decimation
Gain is variable in all stages
Two separate but identical receive paths
Slow attack
Fast attack

Each Rx has own programmable HW gain table and index pointers.
Pointer moves up and down the table, which changes the gain in one or more of the blocks shown left.
Full Table and Split Table mode
Detectors are used:
- Determine if the received signal is overloading a particular block
- If the signal has dropped below programmable thresholds

“LMT” and “ADC” Overload/Peak detectors react to nearly instantaneous overload events. (LMT is analog signal)

In contrast - A digital power measurement in the AD9361 occurs over 16 or more Rx samples.
Peeking through the window to the future
This document contains "forward-looking statements" – that is, statements related to future events.

In this context, forward-looking statements often address expected future business performance, and often contain words such as "expect," "anticipate," "intend," "plan," "believe," "seek," "see," "will," "would," or "target." Forward-looking statements by their nature address matters that are, to different degrees, uncertain.

For us, particular uncertainties that could cause actual performance to be materially different than those expressed in our forward-looking statements.
Moore’s law

- the observation that, over the history of computing hardware, the number of transistors in a dense integrated circuit has doubled approximately every two years.

- According to Ray Kurzweil, the raw processing power of the human brain is on track to being artificially replicable by 2025

- Intel Presentation
Moore’s law in a different light… Lara Croft

- Moore’s law through the evolution Lara Croft
- 1996 to 2014 (18 years, or $2^9$ times transistors)
- from 540 polygons to motion capture realism
  - Robert Browne on HalloweenCostumes.com
Xilinx: Charting an Aggressive Course Forward...

CAPABILITY

In Production NOW!

28nm

System
- +4x System Performance
- Power, Safety & Security enhancements

Processor
- 3.2x CPU Memory Bandwidth
- 8x Video Processing
- 4x more bandwidth between the PS/PL

Programmable Logic
- 60% Performance/Watt
- 4x DSP
- 2x BRAM
- 8x Transceiver Bandwidth

16nm

ZYNQ™

UltraSCALE™

TIMELINE

2012

2015/16
Xilinx Zynq® UltraScale+™ Block Diagram

- **Scaling across**
  - 4 ARM 64-bit cores (running at 1.3 GHz) and
  - FPGA and
  - Real Time Processing Cores (R5),
  - All inside a VM (TrustZone)

- **How to split algorithms for “best” location.**
More than Moore

This is happening today, and we have seen it!
Converter Performance

- Speed and resolution
  - Application dependent
  - Key performance metrics, but not all
    - Power
    - Size / density
    - SFDR
    - Linearity
    - Bandwidth
    - Etc

[Diagram showing bits of resolution and speed]
Throw down: Plato vs Steve Jobs

- **Necessity is the mother of invention**
  - Plato, The Republic

- Market Pull

- **It’s really hard to design products by focus groups. A lot of times, people don’t know what they want until you show it to them.**
  - Steve Jobs

- Technology Push
Sorry – you need to come to the conference next year
YEAH, WE ARE HIRING TOO.

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