NEWS RELEASE

HARVARD RESEARCHERS SELECT FLEX LOGIX'S EMBEDDED FPGA TECHNOLOGY TO DESIGN DEEP LEARNING SoCs

Another EFLX™Design Win Highlights the Growing Momentum for Flex Logix's Reconfigurable RTL Technology

MOUNTAIN VIEW, Calif., June 5, 2017 – Flex Logix™ Technologies, Inc., announced today that its embedded FPGA will be integrated into a next-generation deep learning chip in TSMC 16FFC that is being developed by the research group of Professors David Brooks and Gu-Yeon Wei at Harvard's John A. Paulson School of Engineering and Applied Sciences. Flex Logix and the Harvard researchers have already completed the chip design and tape-out and are now going into fabrication, highlighting the ease-of-use and stability of using the Flex Logix embedded FPGA platform.

"This cooperation with Harvard's researchers highlights the wide range of applications that can be addressed by our EFLX embedded FPGA technology," said Geoff Tate, CEO and co-founder of Flex Logix. "Deep learning has the potential to grow significantly and we are excited to demonstrate the value of our platform for deep learning in a variety of uses. Harvard Professors Brooks and Wei are respected leaders in this field, having presented their work on deep learning accelerators at ISSCC this year, and we are honored to be chosen as their lab's embedded FPGA partner."

"We see a huge opportunity for reconfigurable logic in SoCs targeting deep learning for a wide range of applications such as data centers, mobile, and IoT. Embedded FPGA is changing the way chips are designed and we recognize the power of being able to reconfigure RTL when designing our deep learning chip," said Professor Gu-Yeon Wei, Gordon McKay Professor of Electrical Engineering and Computer Science at Harvard University. "An important attribute of modern deep learning research is how quickly the algorithms change and improve. With embedded FPGAs from Flex Logix we can accommodate these changes in real-time and iterate them for rapid improvement."

The Harvard researchers join other Flex Logix customers such as DARPA who have chosen the EFLX platform to design their next generation chips, ICs, and SoCs. These organizations recognize that the ability to update critical RTL enables chips to evolve as needed for fast changing algorithms and standards. Embedded FPGA eliminates these potential setbacks by providing engineers the flexibility to update or change RTL at any time after fabrication, even in-system.

About the EFLX Embedded FPGA IP Cores

Flex Logix provides an EFLX-2.5K Logic IP core and EFLX-2.5K DSP IP core which are the building blocks for almost 50 different sized arrays. These can mix and match the logic and DSP cores to meet the needs of a wide range of applications. The EFLX-2.5K Logic IP core has 2520 LUTs, 632 inputs and 632 output and is a complete embedded FPGA. The EFLX-2.5K core can be tiled to make larger arrays as required. The EFLX-2.5K DSP core is interchangeable in EFLX arrays with the Logic IP core: the EFLX-2.5K DSP core has 40 MACs (pre-adder, 22-bit multiplier and 48-bit accumulator) which are pipelineable; the number of LUTs is 1880.

The TSMC 16FFC/FF+ implementation offers multiple enhancements: 6-input LUTs for more logic and fewer stages leading to faster clock rates; an enhanced interconnect for more performance especially for large arrays; multiple DFT features for increased fault coverage, faster test time and increased reliability.

EFLX is available in two core sizes (-100 and -2.5K) today on multiple mainstream foundry processes: TSMC40ULP, TSMC28HPM/HPC and TSMC16FF+/FFC. EFLX can also be ported to any proprietary CMOS process for organizations with their own fabs.

EFLX is a digital architecture for development of embedded FPGAs for integration into SoCs, ASICs and MCUs of a wide range of sizes. The EFLX arrays are programmed using VHDL or Verilog; the EFLX compiler takes the output of a synthesis tool such as Synopsys Synplify and does packing, placement, routing, timing and bitstream generation. The bitstream when loaded into the array programs it to execute the desired RTL.

About Flex Logix

Flex Logix, founded in March 2014, provides solutions for reconfigurable RTL in chip and system designs using embedded FPGA IP cores and software. The company's technology platform delivers significant customer benefits by dramatically reducing design and manufacturing risks, accelerating technology roadmaps, and bringing greater flexibility to customers' hardware. Flex Logix has raised more than $12 million of venture capital. It is headquartered in Mountain View, California and has sales rep offices in

China, Europe, Israel, Japan, Taiwan and Texas. More information can be obtained at http://www.flex-logix.com/or follow on Twitter at @efpga.

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