FLEX LOGIX WORKS WITH DARPA TO DEVELOP FLEX LOGIX'S EMBEDDED FPGA IP FOR GOVERNMENT PROJECTS

Another EFLX Design Success Highlights the Growing Momentum for Flex Logix's Reconfigurable RTL Technology

MOUNTAIN VIEW, Calif., Date January 23, 2017 – DARPA, the Defense Advanced Research Projects Agency, announced today that it has signed an agreement to work with Flex Logix to develop Flex Logix's EFLX embedded FPGA technology for use by any company or government agency designing integrated circuits for the US Government. As part of the agreement, Flex Logix will make available EFLX arrays in the TSMC 16FFC process node from 2.5K to 122.5K LUTs so that these companies and agencies can reconfigure RTL at any point during the design process. Having this flexibility will enable chip designers to increase performance, reduce power and lower the size/weight of their critical systems. The EFLX platform will also allow companies to customize one chip in software for numerous applications; or even upgrade the chip when already deployed in the field.

"Embedded FPGA technology is a game changer in the chip design process and we are pleased to be working with DARPA," said Geoff Tate, CEO and co-founder of Flex Logix. "Chip development costs and lead times keep increasing and the ability to reconfigure RTL at any time can eliminate expensive chip spins, enable one chip to address many customers and applications, and extend the life of chips and systems. As a result, designers can easily keep up with changing standards and customer requirements."

Flex Logix is already engaged with additional IC designs under this agreement with DARPA, and it also provides the software for programming the embedded FPGA. The EFLX-2.5K Logic and DSP IP cores are also available for license to any commercial customer directly from Flex Logix.

About the EFLX Embedded FPGA IP Cores

Flex Logix provides an EFLX-2.5K Logic IP core and EFLX-2.5K DSP IP core which are the building blocks for almost 50 different sized arrays. These can mix and match the logic and DSP cores to meet the needs of a wide range of applications. The EFLX-2.5K Logic IP core has 2520 LUTs, 632 inputs and 632 output and is a complete embedded FPGA. The EFLX-2.5K core can be tiled to make larger arrays as required.   The EFLX-2.5K DSP core is interchangeable in EFLX arrays with the Logic IP core: the EFLX-2.5K DSP core has 40 MACs (pre-adder, 22-bit multiplier and 48-bit accumulator) which are pipelineable; the number of LUTs is 1880.

EFLX is available in two core sizes (-100 and -2.5K) today on multiple mainstream foundry processes: TSMC40ULP, TSMC28HPM/HPC and TSMC16FF+; and now is in development for TSMC16FFC as well. EFLX can also be ported to any proprietary CMOS process as well for organizations with their own fabs.

EFLX is a digital architecture for development of embedded FPGAs for integration into SoCs, ASICs and MCUs of a wide range of sizes. The EFLX arrays are programmed using VHDL or Verilog; the EFLX compiler takes the output of a synthesis tool such as Synopsys Synplify and does packing, placement, routing, timing and bitstream generation. The bitstream when loaded into the array programs it to execute the desired RTL.

About Flex Logix

Flex Logix, founded in March 2014, provides solutions for reconfigurable RTL in chip and system designs using embedded FPGA IP cores and software. The company's technology platform delivers significant customer benefits by dramatically reducing design and manufacturing risks, accelerating technology roadmaps, and bringing greater flexibility to customers' hardware. Flex Logix recently secured $7.4 million of venture backed capital. It is headquartered in Mountain View, California and has sales rep offices in China, Europe, Israel, Taiwan and Texas. More information can be obtained at http://www.flex-logix.com or follow on Twitter at @efpga.

PRESS CONTACT:

Kelly Karr
Tanis Communications, Inc.
kelly.karr@taniscomm.com
+408-718-9350