EFLX® Embedded FPGA
Design With Confidence

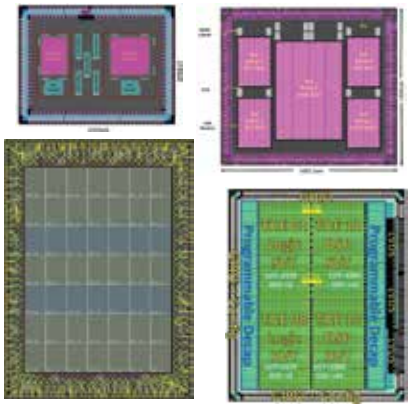
flexlogix EFLX embedded FPGA™

TSMC IP Alliance Member

Flex Logix™ is now a TSMC IP Alliance Member based on the work it has done with TSMC over the past several years to develop embedded FPGA IP meeting TSMC's standards for documentation, design methodology, and engineering validation in silicon. Flex Logix will continue to prove all EFLX embedded FPGA IP in silicon after rigorous engineering checks and sign-offs. EFLX is available in three major TSMC process nodes and we will port on demand to any TSMC node.

Dense, Portable, Scalable Silicon-Proven GDS

EFLX eFPGA validation chips are available for TSMC 16FF+, TSMC 16FFC, TSMC 28HPM/HPC and TSMC 40ULP/LP. All have PLL and PVT monitors to confirm performance and power specifications from -40C to +125C across the full voltage range.



Our patented interconnect uses 5-7 metal layers so we are compatible with most metal stacks, with no GDS change. Traditional FPGA interconnect typically requires many more metal layers: so eFPGA derived from FPGA chips will need to be redesigned for most metal stacks, taking months and changing the GDS; and metal stacks with fewer metal layers may be impossible.

Traditional FPGA interconnect uses 70-80% of the FPGA fabric area. Our patented interconnect is much denser, allowing us to use standard cells for portability while matching the density of eFPGA derived from FPGA chips. Since we use standard cells, our GDS is typically portable across incremental variations in process nodes.

Our IP cores can be arrayed to make ~75 sizes from 100 LUTs to 200K LUTs without GDS change.

Multiple Customers Have Taped Out

Flex Logix EFLX IP taped out successfully in chips by multiple customers, with fully working silicon. Harvard built an AI chip with EFLX in 16nm. DARPA chose us for a license for any Supplier to the US Government to use EFLX in TSMC 16FFC. We have done a port for Sandia's 180nm fab. SiFive has selected us for their 28nm and 180nm platform chips. More customers are in design and evaluation.

SiFive

Proven Management

Our CEO was a GM at AMD since 1983 ending up as Senior VP of processors; then was founding CEO of Rambus joining as the 4th employee, achieving IPO 7 years later and running the company until it reached $2 Billion in Market Capitalization. Our Silicon Engineering VP, our Sales VP and our Director of Solutions Architecture all have >20 years experience at firms like ARM, Intel, and Rambus and our Software Director has >10 years experience at Synopsys and did his PhD thesis on FPGA Place & Route.

Well Financed

We have raised ~$13Million from Lux Ventures and Eclipse Capital and have a strong cash balance.

LUX eclipse

Intensive Support at Every Step of the Way

Our software is available for free to evaluate your RTL to determine size and speed; training too. Our Architecture/Application Engineers can provide you with multiple application notes using EFLX; and can consult on your design including in Mandarin and Hebrew. We have AXI, AHB and APB bus interface RTL. Our Silicon Engineers can show you the details of our design flow and the multiple signoffs we go through to ensure EFLX IP meets spec over the full operating range, even with 1GHz+ speeds, >90% utilization and very large arrays. Our team works with yours week by week on integration. DFT coverage is >>98.5%.

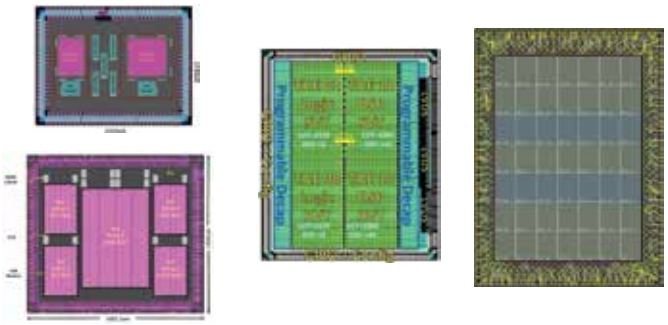
EFLX Embedded FPGA

Get Exactly the Array you Need, Proven in Silicon

TSMC 40, 28, 16 available now

TSMC 40ULP/LP - *PROVEN IN SILICON*
TSMC 28HPM/HPC - *PROVEN IN SILICON*
TSMC 28HPC/HPC+ Gen 2 in design
TSMC 16FF+/FFC - EFLX100 Gen 2 *PROVEN IN SILICON*
TSMC 16FF+/FFC - EFLX4K Gen 2 *FULLY FUNCTIONAL; IN VALIDATION*

We will port to any other TSMC process 180nm to 7nm on customer request.



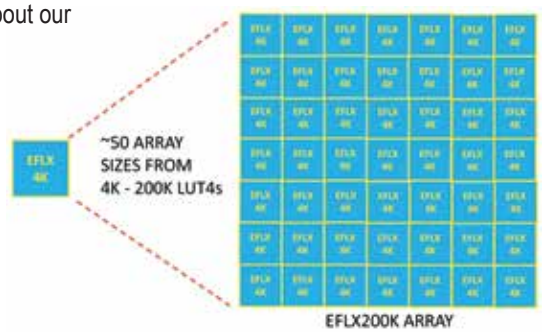
MULTIPLE VT, 5-7LAYERS OF METAL: We design our IP blocks to be compatible with multiple Vt (threshold voltage) mask options and to be compatible with almost all metal stacks. eFPGA IP from FPGA chip companies will use far more metal layers so they'll typically need to redesign for your stack.

Embedded FPGAs from 150 LUTs to ~200K LUT4s

Like Xilinx, we measure array capacity in LUT4 equivalents. EFLX arrays are constructed from one of two building blocks: the EFLX150 core with ~150 LUT4s and the EFLX4K core with ~4K LUT4s. Both are complete embedded FPGAs with programmable logic, programmable interconnect, I/O, clock circuitry and configuration logic. To build arrays of larger size, the cores are design to "tile" into arrays with no GDS change. The EFLX150 can be used in arrays up to ~3.7K LUT4s; the EFLX4K up to ~200K LUT4s. The LUTs in our new Gen 2 architecture are now 6-input LUTs for higher speed and density. All EFLX cores are proven in silicon in arrays of at least 2x2 so all array sizes are proven out. If you need even larger arrays, ask about our roadmap to ~800K LUT4 arrays.

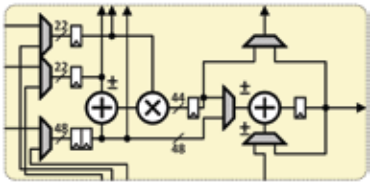
Hundreds to Thousands of Interconnects

A single EFLX-00 core has 152 inputs and 152 outputs (224/224 for 16nm EFLX-150 version); a 5x5 array of EFLX-00/150 cores has 5 times more inputs and outputs.
A single EFLX4K core has 632 inputs and 632 outputs; larger arrays have thousands of interconnects. You can connect EFLX embedded FPGAs into wide, fast buses and wide data and control paths; the interconnects are standard CMOS so they run very fast.



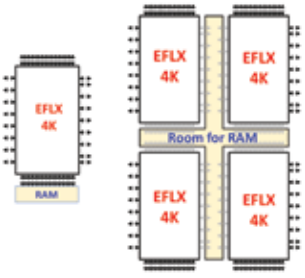
Optional MACs for DSP Acceleration

Both the EFLX-100/150 and EFLX4K cores are offered in versions where some of the LUTs are replaced with Multiplier-Accumulator (MAC) blocks consisting of a 22-bit pre-adder, 22-bit multiplier and 48-bit accumulator which can be pipelined for very fast DSP implementations.



Optional RAM: Any Kind, Any Amount

The EFLX cores contain memory. If you require more, it can be synthesized at the edge of the array or between the cores, within the array. The EFLX Compiler software will map your RTL onto the RAM as part of the array. We synthesize RAM from standard compilers with optional MBIST: single port or dual port, whatever size and number of blocks you want, with or without parity/ECC. We can also integrate your special memory like TCAM or custom accelerators.

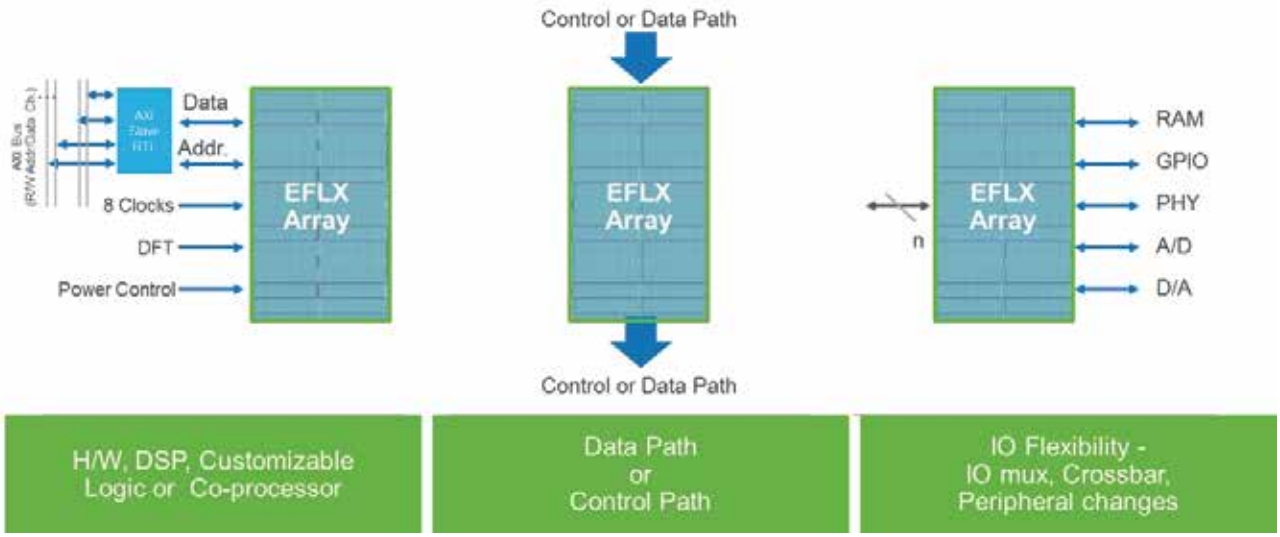


Test and Reliability Features

Test vectors are available with stuck-at fault coverage >>98.5%. Our new Gen 2 Architecture has a special test mode that accelerates test speeds 100x over our first generation. For High Reliability applications we have the ability to read back the configuration bits; and "scrubbing" is also possible to re-write configuration bits periodically.

EFLX Embedded FPGA
Integration & Programming

Flex Logix has interface RTL for AXI, AHB and APB buses as a Slave or Master.



High Density, High Performance Embedded FPGA

EFLX embedded FPGA is implemented as Hard IP: as an array, density is much higher if placement is carefully done. More importantly, Flex Logix™ utilizes an interconnect that gives double the density of traditional mesh FPGA interconnect. Our Gen 2 Architecture increases density using 6-input LUTs which reduces LUT counts typically by 30% -- wider LUTs means fewer LUTs and fewer logic stages which translates to higher speed.

Design Deliverables

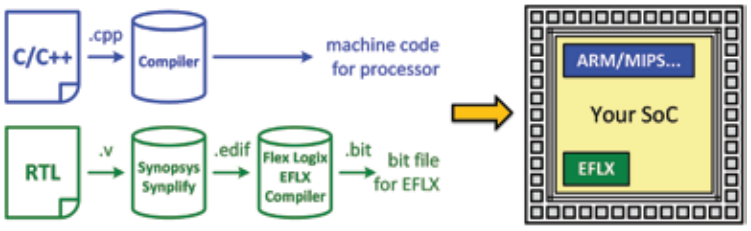
We deliver the exact EFLX array you specify: EFLX100/150 or EFLX4K core, NxM array, your mix of all-LUT and LUT-DSP cores, and RAM if needed.
The design files we deliver are: LEF, LIB, Verilog™ Model, SDF, GDS-II™, CDL/Spice netlist, and DFT test vectors (>>98.5% coverage).
We designed and built a validation chip which is proven in silicon using these same files.
We provide a detailed datasheet including IR drop for static and dynamic, high activity switching.

Power Management Modes & IR Drop Analysis

EFLX cores can be power-gated to reduce static power if not in use; in TSMC 40ULP we added more power management modes and 0.5V state retention.
We use EDA tools to analyze the EFLX array for IR drop in static & high-switching activity dynamic modes to ensure it can operate reliably in your SoC.

EFLX Compiler Programming

To program the EFLX array, use Synopsys® Synplify or another synthesis tool to generate an .edif file which is then input to the EFLX Compiler. You also provide an IO file which shows how the EFLX array is connected to the rest of your chip. EFLX Compiler packs, places, routes and iterates to generate optimum timing performance: if it is acceptable, EFLX Compiler generates the bitstream which when loaded into the EFLX array makes it execute your RTL.



High Utilization

Due to the revolutionary interconnect, the utilization of EFLX arrays is typically higher than in traditional FPGA architecture, often >90%.

Assistance Throughout Your Chip Evaluation and Design

From the start we will assign trained engineers to assist with you with evaluating our technology, presenting the details you need, assisting you with optimizing your RTL for embedded FPGA, and then working weekly through the whole physical design process. We will assist in DFT and chip test as well.

EFLX Embedded FPGA
Applications

flexlogix
EFLX embedded FPGA

Embedded FPGA has High Value in a Very Wide Range of Applications

Microcontroller/IoT
- Reconfigurable accelerators/DSP
- Customer specific RTL
- Reconfigurable Serial I/O
- Battery life extension

Networking
- Reconfigurable protocols
- Programmable parsers
- Programmable NIC

SOCs & ASICs
- Reconfigurable accelerators/DSP
- Deep Learning
- Defense electronics

Data Center
- Processor+FPGA
- Accelerators
- Programmable switch
- Programmable NIC

SSD
- Programmable timing
- Programmable ECC
- Programmable storage protocols for Data Center applications

Wireless Base Station
- Reconfigurable DFE (digital front end)

Growing Series of Application Notes to Help You Get Started

Visit our website for a growing number of App Notes written by our Director of Solutions Architecture (ex-Intel Systems Architect and Sun Architect) and his team of Architects/Applications Engineers.

1. a simple example to get started is our app note on using EFLX as a software reconfigurable I/O Pin Multiplexer

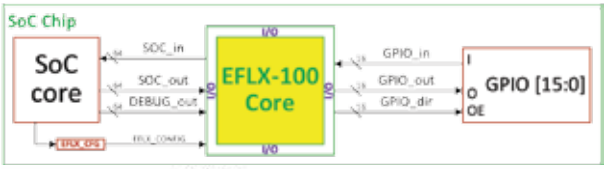
2. Our Accelerators app note shows the detailed verilog for AXI/AHB/APB bus slaves and masters for connecting EFLX to common processor buses. And several accelerator examples (AES, SHA, FFT, JPEG) are shown that demonstrate reconfigurable accelerators can achieve performance 20 - 140 times faster than typical MPUs.

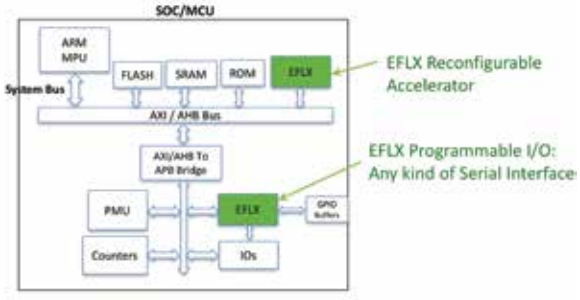
3. Our Flexible I/O app note shows how to implement multiple common serial I/O standards in EFLX arrays: this is particularly useful in MCU and IoT apps.

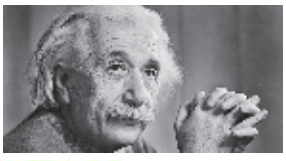
4. Our app note on Battery Life Extension shows how in battery-backed applications the common, repetitive, simple DSP tasks can execute in EFLX using much less energy than code on a processor, primarily because of the memory reference energy required for a processor.

5. Harvard has a Deep Learning chip in fab using EFLX: they will publish a paper in the near future showing how they use EFLX to allow real-time algorithm iteration

6. When cost reducing an FPGA design to ASIC, it is now possible to keep some of it flexible by integrating EFLX in the ASIC or even attaching an EFLX chiplet.







www.flex-logix.com