Gen2 TSMC 28HPC/HPC+ EFLX®4K TARGET Product Brief

The Gen2 EFLX®4K Logic IP core is an embeddable FPGA IP core each containing 2,520 Look-Up-Tables (LUTs: each is 6-input, or dual-5-input, with 2 independent outputs with 2 bypassable flip flops) in Reconfigurable Building Blocks (RBBs) and 21Kb RAM, an improved XFLX™ interconnect network, multiple clocks & scan: fully reconfigurable in-field at any time.

The EFLX4K DSP core has 40 DSP MACs (22x22 multiplier with 48 bit accumulator). In the Gen2 architecture, MACs pipelined to 10 stages without using the interconnect network.

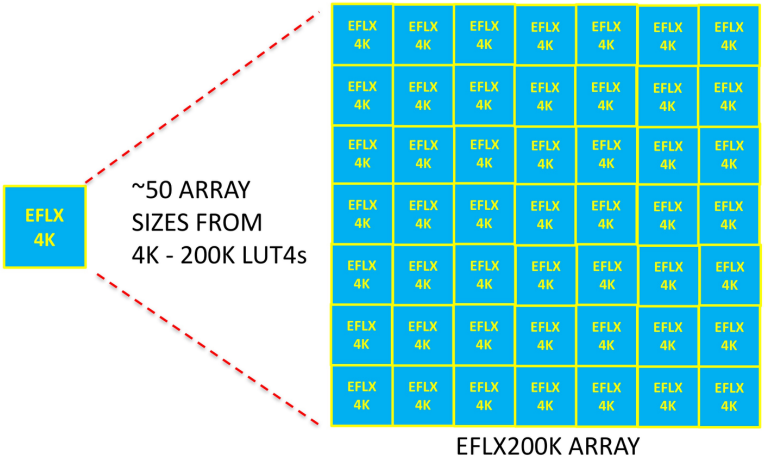
Each EFLX core is a standalone embedded FPGA. Cores can be arrayed up to 7x7 to create arrays of >100K LUTs. Logic and DSP cores can be mixed. And RAM can be integrated as well.

Our improved Gen2 XFLX programmable interconnect has been optimized for higher performance, especially for large arrays. Only 6 metal layers are utilized so this IP is compatible with almost all metal stacks.

Name	EFLX®4K Core Gen2	
Technology	TSMC 28nm HPC/HPC+	
Metal Utilization	6 metal layers	
Metal Stack	M1+5X	
Nominal Supply Voltages (V)	0.8, 0.9	
Junction Temperature (°C)	–40 to 125	
Leakage Power (mW)	3.5mW (HPC+, TT, 0.9Vj, 25°C Tj)	
Performance	Use EFLX Compiler TSMC16FFC frequency times 0.7x for estimate of TSMC28HPC+ performance	
Area (mm^2)	1.6	
Clock inputs	1 to 8	
Input and Output Pins	632 input & 632 output, each with an optional flip-flop	
Look-up Tables (6-input LUT with two independent outputs)	Logic/Mem Core	DSP Core
	2,520 (~4.0K LUT4)	1,880 (~3.0K LUT4)
Total Flip Flops (ex DSP)	6,304	5,024
Distributed Memory (Kb)	21Kb	1Kb
22-bit DSP MACs	0	40
EFLX Array Sizes Possible	1×1 to 7×7	
Design-for-Test Support	Yes, 99% fault coverage	
LUT Utilization	Typically ~90%	

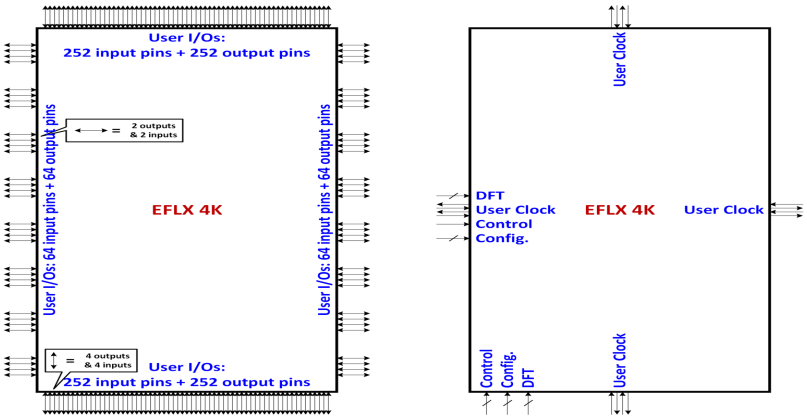
The EFLX4K Core comprises three major blocks: the reconfigurable building blocks (RBBs) of logic/memory types, the XFLX interconnect network, and the user I/Os. In the EFLX4K DSP Core, some of the RBBs are replaced with 40 DSP MACs.

EFLX features full connectivity inside the core, and provides ArrayLinx interconnects at the boundary to concatenate multiple cores via the expandable network I/Os: ~50 array sizes are possible from 4K LUT4s up to 200K LUT4s.



flexlogix Technologies, Inc.

Gen 2 DFT improvements achieve 99% coverage of all faults & a new configuration load mode for test reduces test times about 100 times faster than Gen 1 to lower test costs.



T28HPC/HPC+ EFLX4K dimensions: 1.16mm wide, 1.37mm tall

The EFLX4K Core has 632 input pins and 632 output pins placed as follows: 64 West, 64 East, 252 North, and 252 South. The I/O pins provide user access to the EFLX core. Each I/O has a bypassable flip flop. When multiple cores are concatenated into EFLX arrays, the I/O pins along the abutting edges are disabled (or are used for controlling embedded RAM blocks).

Besides I/O pins, there are clock, configuration, and test/DFT pins. Each Core has an internal power grid (V_{DDH} and V_{SS}) which can be connected to the customer's digital SoC power grid. The Core has 5 power control pins (1 West, 4 South) for power-on and power gating. The Core also has 6 configuration inputs on the West side and 4 configuration inputs on the South side to load the bitstream. An AXI or JTAG interface is available for configuration. On each side of the Core, there are 2 input clocks and 2 output clocks for a total of 8. The ArrayLinx pins are not shown in the diagram above.

Deliverables and EDA Design Views	
Front-end Design view (with NDA)	**Back-end Design Views (with License)**
Encrypted Verilog Netlist	Encrypted Verilog Netlist with Timing Annotation, SDF
LIB	GDS-II
Footprint LEF	CDL/Spice netlist
Detailed datasheet & DSP User's Guide	Integration guidelines
Silicon validation report, when available	Integration assistance as needed
EFLX Compiler evaluation version	EFLX Compiler bitstream generation version
	Test vectors for 99% fault coverage

flexlogix Technologies, Inc.