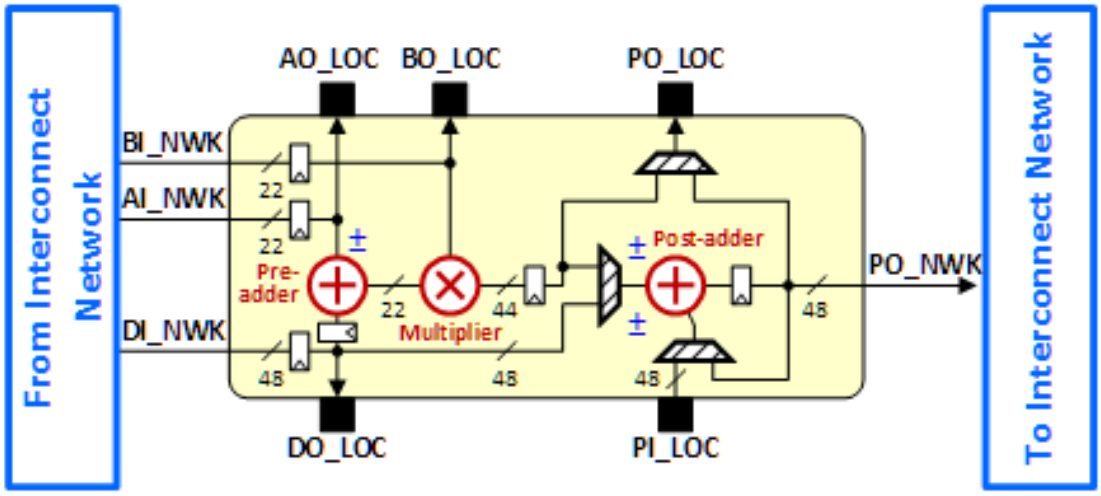
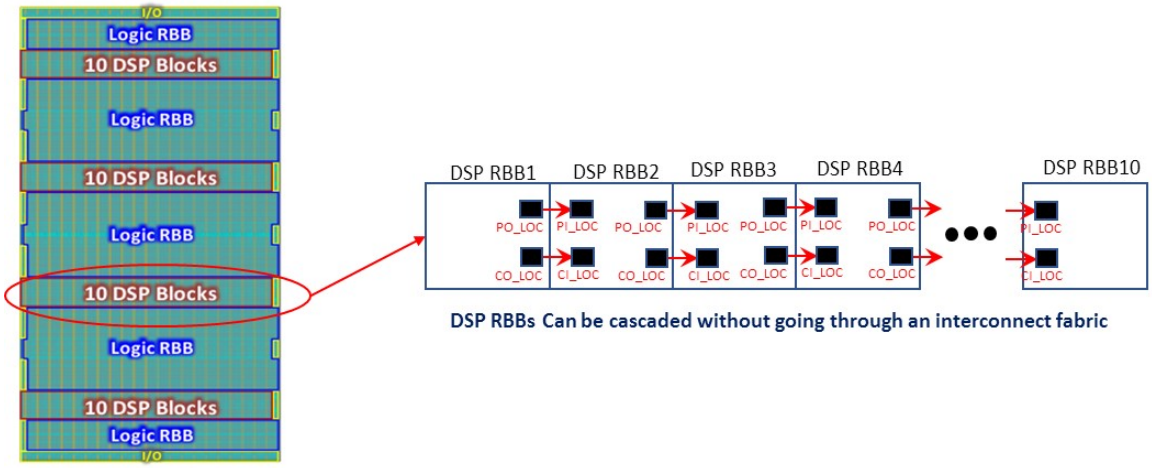
EFLX®4K DSP/AI MACs

EFLX4K cores for reconfigurable RTL are available in versions where ~1/4 of the LUTs are replaced with 40 DSP accelerator blocks. EFLX4K DSP cores can be mixed with EFLX4K Logic cores to make EFLX arrays.

Each DSP accelerator block has a 22x22 multiplier, a pre-adder and 48-bit post-adder (MAC) with muxing. It can also be configured for 11x11 complex multiply/add OR for dual 11x11 multiply (useful for AI). PO_LOC, PI_LOC, AO_LOC, BO_LOC and DO_LOC are used for cascading DSPs and do not go through the interconnect network. PO_NWK output goes to the XFLX interconnect network and BI_NWK, AI_NWK and DI_NWK inputs come from the XFLX interconnect network.



The MACs can be cascaded without going through the XFLX interconnect network as shown below:



The 40 DSPs in an EFLX4K are in rows of 10 DSP RBBs. P_{out} of one DSP pipes to P_{in} of the adjacent DSP. This improves performance for many DSP functions.

The EFLX Compiler maps your RTL, including DSP functions, on to the EFLX array including the DSP accelerator blocks.

Some examples of DSP implementation & performance at worst case conditions

Process Node	TSMC 28HPM[1]	TSMC 16FFC[2]
EFLX Core	EFLX4K	EFLX4K
18x18 signed multiply	722 MHz	1031 MHz
5-Tap Asymmetric FIR Filter	722 MHz	1031 MHz
21-Tap Symmetric FIR Filter	389 MHz	555 MHz
40-Tap Symmetric FIR Filter	351 MHz	501 MHz
FFT 256	114 MHz	171 MHz

1. TSMC 28HPM worst case: 0.81Vj, 125C Tj, Slow/Slow corner
2. TSMC 16FFC worst case: 0.72V, -40/125C Tj, SSGNP (r)cworst_Ccworst_T

The EFLX cores have several voltage range options in addition to the above.

A detailed performance application note is available with more information and RTL code for it can be downloaded, so you may use it to generate hyour own benchmark versions or to benchmark other eFPGA.

flexlogix
Reconfigure your RTL