Headplay Part Number : 3130-10496
Mfg : Brillian
Mfg Part No : 6500007-1002

Z86D-3C

SVGA Microdisplay
Preliminary Data Sheet

Document 6040-0032-01-D7

Overview

The Brillian Z86D-3 SVGA (super video graphics array) microdisplay is a high-resolution, high-refresh-rate, 12 mm-diagonal (0.47") LCoS™ microdisplay designed for color field-sequential operation. The Z86D-3C is a consumer-appearance-graded device functionally identical to the Z86D-3.

The Z86D-3 microdisplay includes many of the controls and functions required to display high-quality images, including a digital-pixel interface and control interface to the host system, look-up tables for custom gray-scale (color-adjustment) curves, DACs (digital-to-analog converters) that convert digital pixel data into pixel gray-scale levels, and row and column controls to apply the signals to the pixels.

Complete system designs can be simplified with standard (CMD8X6DDI) or custom display interface ASICs and the CMD3XLB illumination controller ASIC.

Features

- High 360 color field/second refresh rate (120 frames/second)
- High 800×600-pixel SVGA resolution
- On-chip DAC minimizes external circuity for an all-digital interface
- Integrated look-up tables support 18-bit color depth from a 24-bit color pallet
- Compact BGA package promotes small form factor products and low-cost manufacturing

Typical Applications

- Mobile computing PC headsets
- Entertainment headsets
- Digital camera, videophone, internet appliance, and other viewfinders

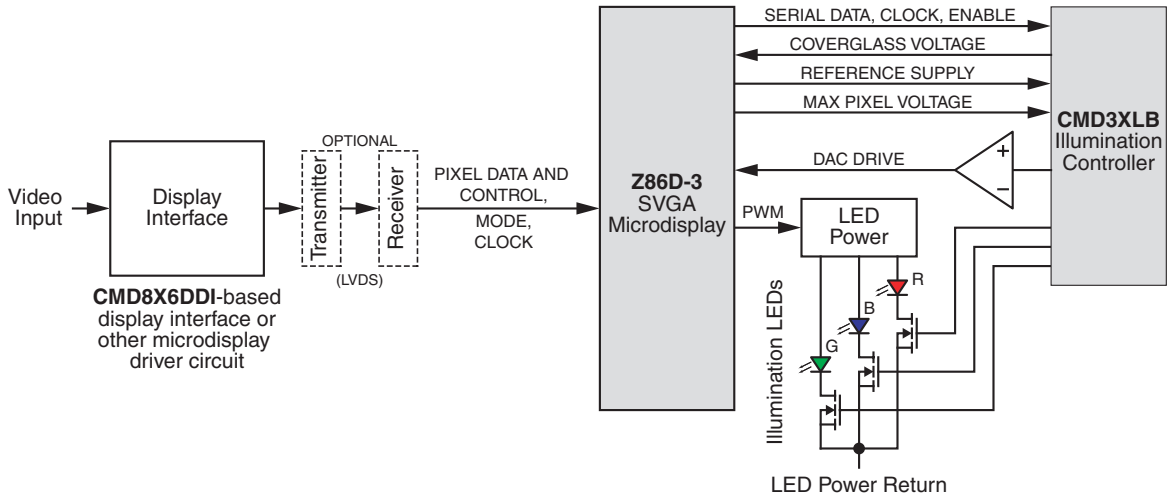

Figure 1. Typical Z86D-3 Microdisplay System

Preliminary Data Sheet Notice

- ***Preliminary data sheets contain target specifications only and are subject to change without notice.***

Handling Precautions

Hot-Plug Susceptibility

- The device is susceptible to hot-plug damage.
  - Turn off power before connecting or disconnecting the microdisplay.

ESD Sensitivity

- The device is ESD sensitive.
  - Use proper ESD handling procedures to protect the device from electrostatic damage.

General Precautions

- Handle and operate only in a clean environment.

Protective Film

- The device is supplied with a protective film on the surface of the display.
  - Handle the device with the protective film in place.
  - Remove film only after device is mounted and secured in place.
  - Remove film in a clean, ESD-controlled environment.

Pick and Place Precautions

- The BGA device is compatible with pick-and-place equipment with appropriate precautions.
  - The protective film must be on the glass when using handling equipment.
  - Ensure that pick-and-place equipment will not scratch or damage the top glass surface of the display.

Cleaning

- The glass surface may be cleaned with isopropyl alcohol.
  - **Do not** clean with other solvents, abrasive cleaners. or metal tools!

Environmental Exposure

- The device is shipped in a tray in an antistatic ESD bag.
  - Do not expose the device to a strong UV source.
  - Store at room temperature.
  - Open and use as soon as possible.
- Store unused devices in the original ESD bag, and in accordance with “Environmental Ratings” on page 5 of this document.

Pinout

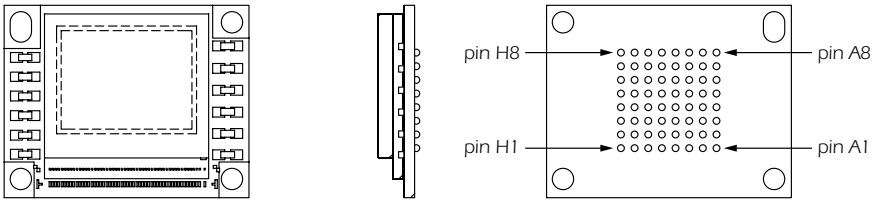

Figure 2. Z86D-3 Microdisplay BGA (Ball Grid Array)

Pin Descriptions

Pin	Signal	Direction	Description
Power Interface			
B5, B6, B7, B8	VDD	input	+5V Digital Supply
A3, A4, A5, A6, H3, H4, H5, H6	VDDA	input	+5V Analog Supply
G8	VDDREF	input	+5V Analog Supply: For internal DAC reference circuits.
B2	VBB	input	+6V Supply
C4, C5, C6, D3, D4, D5, D6, E3, E4, E5, E6, F4, F5	GND	return	Ground
3XL Illumination Control Interface Signals			
A1	3XL_PWM	output	PWM Control: Controls LED intensity in the external illumination circuit.
A2	3XL_EN	output	Enable: Signal for 3-wire synchronous serial interface to illumination controller (CMD3XLB).
A7	3XL_DATA	output	Data: Signal for 3-wire synchronous serial interface to the illumination controller (CMD3XLB).
A8	3XL_CLK	output	Clock: Signal for 3-wire synchronous serial interface to the illumination controller (CMD3XLB).
Miscellaneous Signals			
B1	VMAX	output	Maximum Voltage Reference: Voltage derived from pixel values written to the array. Available for scaling the output of a DAC generating the coverglass voltage. (To CMD3XLB or buffer op amp.)
H8	XGLASS	input	Coverglass Voltage: From illumination controller DAC (CMD3XLB).
H2	VREF	output	Internal Reference Voltage: 1.202V nominal reference output
H1	COMP	output	Internal Compensation: Do not connect this pin.
H7	RSET	input	DAC Drive Set: Current output controlling the pixel DAC.

Table 1. Pin Descriptions (Part 1)

Pin	Signal	Type	Control Mode	Pixel Mode	Description
Pixel Data and Control Interface					
B4	RESET#	input/output	RESET#		Device Reset: Active low resets the Z86D-3. Also driven low if the watchdog timer is triggered. If driven by an external source, a current limiting resistor must be placed in series to protect the source.
B3	DPMODE	input	DPMODE		Mode Select: Selects operating mode of dual-function pins 0 = control mode; 1 = pixel mode
C1	DPCLK	input	DPCLK		Data/Pixel Clock: Clock used to synchronize control-mode write/read and pixel-mode loading operations.
F1	DPCSEL	input	DCSEL		Chip Select: Active-high control signal must be valid to enable control-mode write/read and pixel mode loading operations.
C2	DPD0	input/output	DATA0	PIXEL0_BIT0	Dual-Function Pins: Control-Mode Pin Definitions—Demultiplexed control bus for writing and reading data to/from the control registers and look up tables. ADDR[8:0]: 9-bit address bus DATA[7:0]: 8-bit data bus WRITE: Active high data write control signal READ: Active high data read control signal Pixel-Mode Pin Definitions—Interface for writing four consecutive 6-bit pixel data values per DPCLK during the pixel loading sequence. PIXEL0_BIT[5:0]: 6-bit value for pixel n PIXEL1_BIT[5:0]: 6-bit value for pixel n+1 PIXEL2_BIT[5:0]: 6-bit value for pixel n+2 PIXEL3_BIT[5:0]: 6-bit value for pixel n+3
C3	DPD1	input/output	DATA1	PIXEL0_BIT1	
C7	DPD2	input/output	DATA2	PIXEL0_BIT2	
C8	DPD3	input/output	DATA3	PIXEL0_BIT3	
D1	DPD4	input/output	DATA4	PIXEL0_BIT4	
D2	DPD5	input/output	DATA5	PIXEL0_BIT5	
D7	DPD6	input	not used	PIXEL1_BIT0	
D8	DPD7	input	not used	PIXEL1_BIT1	
E1	DPD8	input	WRITE	PIXEL1_BIT2	
E2	DPD9	input	READ	PIXEL1_BIT3	
E7	DPD10	input/output	DATA6	PIXEL1_BIT4	
E8	DPD11	input/output	DATA7	PIXEL1_BIT5	
F2	DPD12	input	ADDR0	PIXEL2_BIT0	
F3	DPD13	input	ADDR1	PIXEL2_BIT1	
F6	DPD14	input	ADDR2	PIXEL2_BIT2	
F7	DPD15	input	ADDR3	PIXEL2_BIT3	
F8	DPD16	input	ADDR4	PIXEL2_BIT4	
G1	DPD17	input	ADDR5	PIXEL2_BIT5	
G2	DPD18	input	ADDR6	PIXEL3_BIT0	
G3	DPD19	input	ADDR7	PIXEL3_BIT1	
G4	DPD20	input	ADDR8	PIXEL3_BIT2	
G5	DPD21	input	not used	PIXEL3_BIT3	
G6	DPD22	input	not used	PIXEL3_BIT4	
G7	DPD23	input	not used	PIXEL3_BIT5	

Table 2. Pin Descriptions (Part 2)

Physical Characteristics

Parameter	Condition	Typ.	Units
Resolution	horizontal × vertical	800×600	pixels
Pixel Pitch		12×12	µm
Fill Factor		> 93	%
Microdisplay Image Area	horizontal × vertical	9.6×7.2	mm
	diagonal	12	mm
Overall Dimensions	width × height × depth, Note 1	18.0×14.162×3.139	mm
Weight		1.2	g

Table 3. Physical Characteristics

1. Detailed mechanical dimensions of the Z86D-3 are shown in Figure 20 on page 35. Contact Brillian for World Wide Web access to the latest version.

Environmental Ratings

Symbol	Parameter	Min, Limit	Max. Limit	Unit
T_A	Ambient Operating Temperature	0	+60	°C
T_{STG}	Storage Temperature	–20	+70	°C
rh	Relative Humidity, Note 2		85	%
	Vibration, 20Hz to 20kHz	Note 3		
	Shock, 3-Axis		30	g
ESD	Electrostatic Discharge	Class 2		
MSL	Moisture Sensitivity Level, Note 4	Level 1		

Table 4. Environmental Ratings

2. Noncondensing.
3. 0.0001 g^2/Hz to 0.01 g^2/Hz, 20Hz to 2kHz, 30 minutes per axis.
4. Unlimited floor life at ≤30°C, 85%rh. Refer to IPC/J-STD-033A.

Absolute Maximum Ratings

V_{SS} = 0V; Note 5

Symbol	Parameter	Min. Limit	Max. Limit	Unit
V_{DD} V_{DDA} V_{DDREF}	+5V Supplies	–0.5	7.0	V
V_{BB}	+6V Supply	–0.5	7.0	V
V_{CG}	Coverglass Voltage	–6.0	10.0	V
V_I	Logic Input Voltage, Note 6	–0.5V	V_{DD}+0.5	V
I_O	5V Logic Output Current, Note 7		±100	mA

Table 5. Absolute Maximum Ratings

5. Exceeding the absolute maximum ratings may damage the device. Absolute maximum ratings are stress ratings only and are not intended for operation. The device is not guaranteed to function outside its operating range. Attempting operation outside the operating ratings may deteriorate the device.
6. DPCLK, DPMODE, DPCSEL, DPD[23:0], RESET
7. 3XL_PWM, 3XL_CLK, 3XL_EN, 3XL_DATA, RESET, DPD[11:10], DPD[5:0]

Operating Ratings

V_{SS} = 0V

Symbol	Parameter	Min	Nom.	Max.	Unit
V_{DD} V_{DDA} V_{DDREF}	+5V Supply Voltage	4.75	5.0	5.25	V
V_{BB}	+6V Supply Voltage	5.6	6.0	6.5	V

Table 6. Operating Ratings

Power Dissipation

V_{DDA} = V_{DDREF} = V_{DD}. V_{DD}= +5V, V_{BB} = 6V, V_{SS} = 0V; T_A = 25°C; unless noted.

Symbol	Parameters	Min.	Typ.	Max.	Unit
V_{DD}	+5V Digital Supply		167		mW
V_{DDA}	+5V Analog Supply		210		mW
V_{DDREF}	+5V Analog Supply (DAC)		15		mW
V_{BB}	+6V Supply		180		µW

Table 7. Power Dissipation

DC Electrical Characteristics

$V_{DDA} = V_{DDREF} = V_{DD}$. $V_{DD} = 5V$, $V_{BB} = 6V$, $V_{SS} = 0V$; $T_A = +25°C$; **bold** values indicate $4.75V \le V_{DD} \le 5.25V$ and $0°C \le T_A \le +60°C$; unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
+5V Supply						
I_{DD}	VDD-pin Supply Current	f_{DPCLK} = 80MHz, field refresh = 360Hz, Note 8		88	**100**	mA
I_{DDA}	VDDA-pin Supply Current	f_{DPCLK} = 80MHz, field refresh = 360Hz, Note 8		88	**100**	mA
I_{DDREF}	VDDREF-pin Supply Current	f_{DPCLK} = 80MHz, field refresh = 360Hz, Note 8		3	**5**	mA
+6V Supply						
I_{BB}	Supply Current	f_{DPCLK} = 80MHz, field refresh = 360Hz		12	**18**	mA
VMAX-pin Output						
V_{MAX}	Output Voltage		3.7	3.8	4.0	V
I_{MAX}	Output Current				1	nA
VREF-pin Output						
V_{REF}	Reference Output Voltage	no load		1.202		V
Logic						
V_{IH}	Input Voltage, High	Note 9	**2.5**			V
V_{IL}	Input Voltage, Low	Note 9			**0.8**	V
Signals						
V_{OH}	Output Voltage, High	I_{OH} = –2mA, Note 10	2.4			V
V_{OL}	Output Voltage, Low	I_{OL} = 2mA, Note 10			0.4	V
I_{LI}	Input Leakage Current	Note 9			1.0	µA
I_{LO}	Output Leakage Current	Note 10			1.0	µA
C_I	Input Capacitance	Note 9			5	pF

Table 8. DC Electrical Characteristics

8. Typical current values represent the peak current requirements.
9. DPCLK, DPMODE, DPCSEL, DPD[23:0], RESET
10. 3XL_PWM, 3XL_CLK, 3XL_DATA, 3XL_EN, RESET, DPD[11:10], DPD[5:0]

AC Electrical Characteristics

$V_{DDA} = V_{DDREF} = V_{DD}$. V_{DD}= 5V, V_{SS} = 0V; T_A = 25°C; unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DPCLK						
$1/t_C$	DPCLK Frequency		64		80	MHz
t_C	DPCLK Period		12.5		15.6	ns
t_{CJ}	DPCLK Jitter	Note 11			40	ps
t_{CH}	DPCLK High Time		5			ns
t_{CL}	DPCLK Low Time		5			ns
t_{RF}	DPCLK Rise/Fall Time				2	ns
DPMODE, DPCSEL, DPD[23:0]						
t_S	Signal Setup Time Before DPCLK Falling Edge		6			ns
t_H	Signal Hold Time After DPCLK Falling Edge		2			ns
	DPCSEL Valid to DPMODE Valid Phase Delay		0			ns
RESET						
t_{DRI}	RESET Input	(external reset) not shown	60			µs

Table 9. General Display Interface Characteristics

11. Maximum allowable clock-to-clock jitter at 80 MHz.

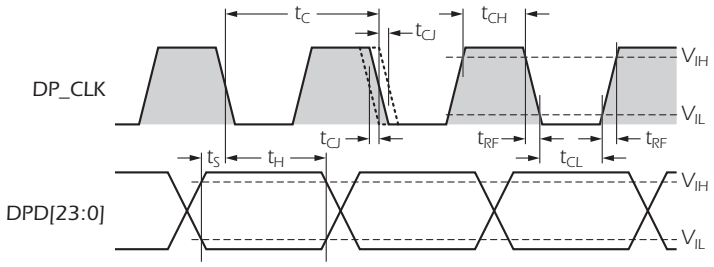

Figure 3. Display Interface Timing Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_C	General	DPCLK period	12.5			ns
t_S		Setup time from DPCSEL, DPMODE, READ, WRITE, ADDR and DATA valid to DPCLK↓	6			ns
t_H		Hold time from DPCLK↓ to change in DPCSEL, DPMODE, READ, WRITE, ADDR and DATA	2			ns
t_{DRS}	Read Cycle	Single read-cycle period	$4t_C$		$4t_C$	ns
t_{DRN}		Sequential (n) write cycle period	$n \cdot 4t_C$		$n \cdot 4t_C$	ns
t_{DCR}	DPCSEL	Delay from chip select becoming active to READ active and DPCLK↓	t_S+t_C			ns
t_{DMR}	DPMODE	Delay from a change to control mode to READ active and DPCLK↓	t_S+t_C			ns
t_{DWR}	WRITE	Delay from the write signal becoming inactive to READ active and DPCLK↓	t_S			ns
t_{HR}	READ	Hold time from first DPCLK↓ of a read cycle to the read signal becoming inactive	$t_{DRN}-t_C+t_H$			ns
t_{SRA}	ADDR	Set-up time from address valid to READ active and the first DPCLK↓ of a read cycle	t_S			ns
t_{HRA}		Hold time from first DPCLK↓ of a read cycle to change in address	$3t_C+t_H$			ns
t_{DZD}	DATA, Note 12	Delay from first DPCLK↓ after READ active to DATA pin change from high-Z to output			2	ns
t_{DRD}		Delay from first DPCLK↓ of a read cycle to read data valid			$2t_C+5$	ns
t_{HRD}		Hold time from DPCLK↓ after ADDR change to read data invalid	2			ns
t_{DDZ}		Delay from first DPCLK↓ after READ inactive to DATA pin change from output to high-Z			4	ns

Table 10. Display Interface Read-Cycle Timing

12. All parameters specified for DATA output pin loading of 5pF.

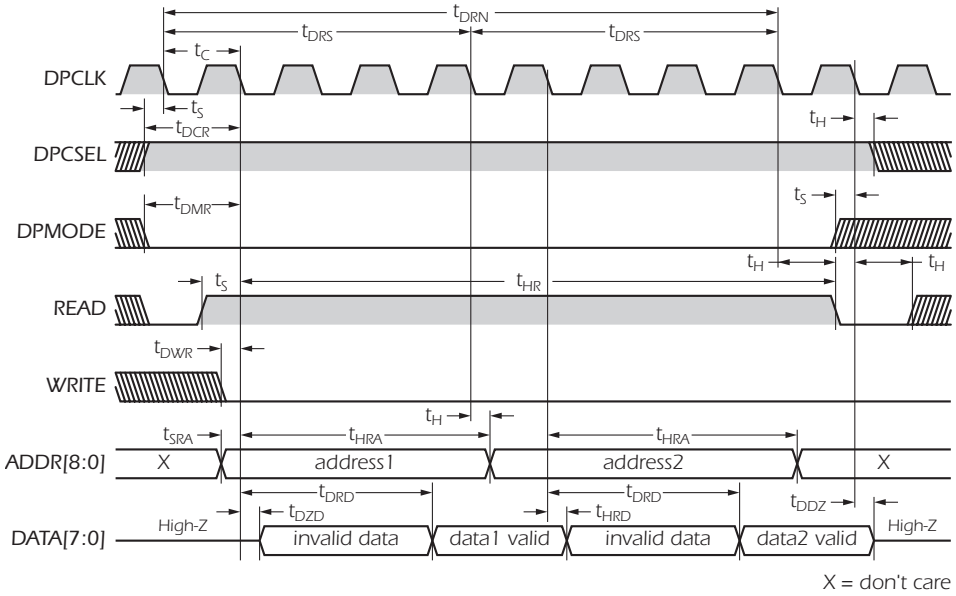

Figure 4. Read-Cycle Timing

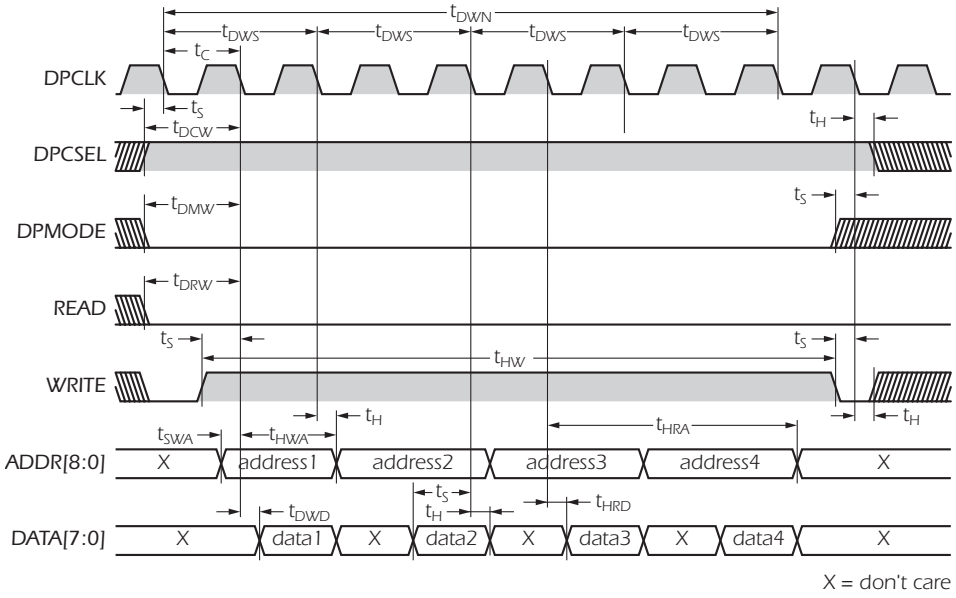

Figure 5. Write-Cycle Timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_C	General	DPCLK period	12.5			ns
t_S		Setup time from DPCSEL, DPMODE, READ, WRITE, ADDR and DATA valid to DPCLK↓	6			ns
t_H		Hold time from DPCLK↓ to change in DPCSEL, DPMODE, READ, WRITE, ADDR and DATA	2			ns
t_{DWS}	Write Cycle	Single Write Cycle Period	$2t_C$		$2t_C$	ns
t_{DWN}		Sequential (n) Write Cycle Period	$n \cdot 2t_C$		$n \cdot 2t_C$	ns
t_{DCW}	DPCSEL	Delay from chip select becoming active to WRITE active and DPCLK↓	t_S+t_C			ns
t_{DMW}	DPMODE	Delay from a change to control mode to WRITE active and DPCLK↓	t_S+t_C			ns
t_{DRW}	READ	Delay from completion of a read cycle to WRITE active and DPCLK↓	t_S+t_C			ns
t_{HW}	WRITE	Hold time from first DPCLK↓ of a write cycle to the write signal becoming inactive	$t_{DWN}-t_C+t_H$		$t_{DWN}-t_S$	ns
t_{SWA}	ADDR	Set-up time from address valid to WRITE active and the first DPCLK↓ of a write cycle	t_S		t_C-t_H	ns
t_{HWA}		Hold time from first DPCLK↓ of a write cycle to change in address	t_C+t_H			ns
t_{DWD}	DATA	Delay from first DPCLK↓ of a write cycle to write data valid			t_C-t_S	ns

Table 11. Display Interface Write-Cycle Timing

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_C	General	DPCLK period	12.5			ns
t_S		Setup time from DPCSEL, DPMODE, PIXEL0, PIXEL1, PIXEL2 and PIXEL3 valid to DPCLK↓	6			ns
t_H		Hold time from DPCLK↓ to change in DPCSEL, DPMODE, PIXEL0, PIXEL1, PIXEL2 and PIXEL3	2			ns
t_{DPR}	Pixel Load Cycle	Row load period (Horizontal)	207 t_C			ns
t_{DPF}		Frame load period	600 t_{DPR}			ns
t_{DCP}	DPCSEL	Delay from chip select becoming active to first DPCLK↓ of a horizontal pixel load sequence	t_S+t_C			ns
t_{DMP}	DPMODE	Delay from a change to pixel mode to first DPCLK↓ of a row load sequence	t_S+t_C			ns
t_{DPD}	PIXEL0 PIXEL1 PIXEL2 PIXEL3	Delay from first DPCLK↓ after DPMODE change to pixel mode to pixel data valid			t_C-t_S	ns

Table 12. Pixel-Mode Timing

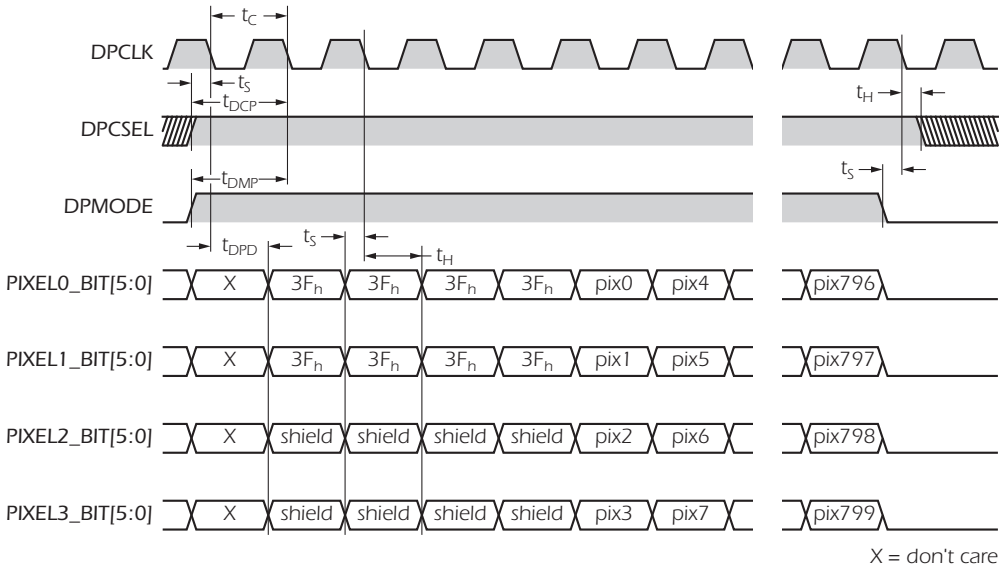

Figure 6. Pixel-Mode Timing

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_C	DPCLK	DPCLK Period	12.5			ns
t_{DSC}	Serial Transfer Cycle	Serial data transfer cycle period	$15t_{CS}$		$15t_{CS}$	ns
t_{CS}	3XL_CLK	Serial clock period	$4t_C$		$256t_C$	ns
t_{SS}	3XL_DATA	Setup time from serial data valid to 3XL_CLK↑	5			ns
t_{HS}		Hold time from 3XL_CLK↑ to a change in serial data	5			ns
t_{DCE}	3XL_EN	Delay from completion of a serial data transfer cycle to serial enable valid		0		ns
t_{DE}		Serial enable valid period		t_{CS}		ns

Table 13. 3XL Interface Serial-Data Timing

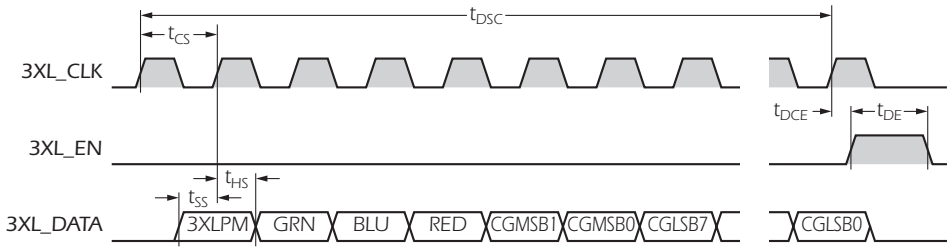

Figure 7. 3XL Serial-Interface Timing

Electro-Optic Characteristics

Timing = color-field sequential, f_{DPCLK} = 80MHz, T_A = 40°C (forced air), rh = noncondensing, ambient illumination < 1lx; measurement per Figure 8; unless noted.

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
f_R	Refresh Rate	(color field rate), Note 13		360		Hz
GL	Gray-Scale Levels	red, green, and blue		256		levels
CR_W	Contrast Ratio	360Hz, white, Note 14, Note 16	75:1			
RE_G	Reflectivity Efficiency	360Hz, green, Note 15, Note 16	35			%

Table 14. Electro-Optic Characteristics

13. Operation above the typical value may degrade image contrast. Operation below the typical value may increase flicker to perceptible levels. Generally flicker is not perceptible from 300Hz–360Hz.

14. $CR_W = \frac{L_{white}}{L_{black}}$

where: L_{white} = luminance at maximum grayscale level; L_{black} = luminance at minimum grayscale level.

15. $RE_G = \frac{L_{green}}{L_{REF(green)}}$

where: L_{green} = luminance at maximum grayscale level with only green LED in operation; $L_{REF(green)}$ = luminance of ideal Q.W.P. mirror, under the same illumination conditions, in place of the microdisplay.

16. Measured using Z86D-3 SVGA Chipset Evaluation Kit with factory-approved configuration file.

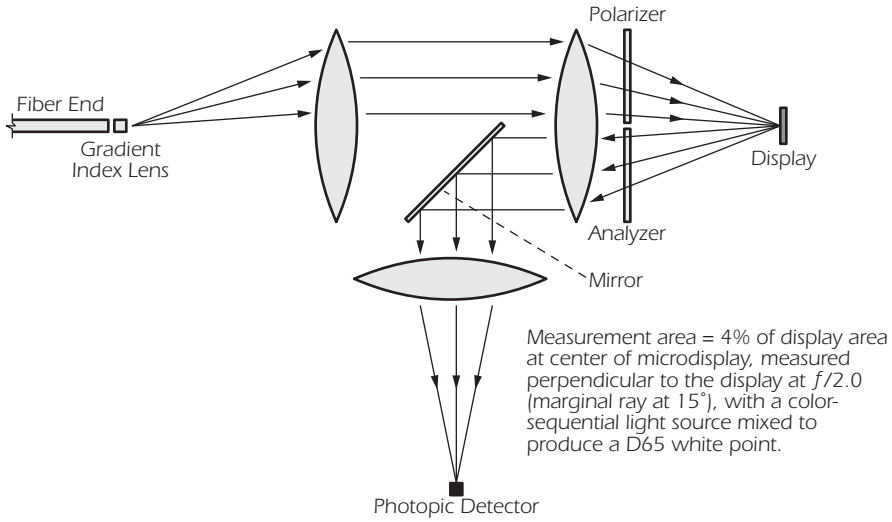

Figure 8. Crossed-Polarizer Measurement Configuration

Electro-Optic Operating Appearance Defects

Dot defects ≥1 pixel in size, visible on a white, black, or gray background:

Parameter	Size	Score	Max.Limit
Bright Dot Defects, Note 17	any		none allowed
Dark Dot Defects, Note 22	small, Note 18	1 point	5 points total
	medium, Note 19	2 points	
	large, Note 20		none allowed
	adjacency, Note 21		2 adjacent dot defects

Table 15. Operating Image Area Dot Defects

17. Bright dot defects are dots that appear bright when a black or gray pattern is displayed.
18. Small dot defects are equal to or larger than 1 pixel, but not more than 2 pixels in size.
19. Medium dot defects are larger than 2 pixels, but not more than 5 pixels in size.
20. Large dot defects are larger than 5 pixels in size
21. Number of dot defects within a distance of 80 pixels (960µm).
22. Dark dot defects are dots that appear dark when a white or gray pattern is displayed.

Parameter	Standard
Vertical Banding	shall not be visible in white image area, Note 23
Frame Color	shall be darker than 32% gray, Note 24
Color Uniformity	shall not exhibit obvious multiple rings of color change on black or white image area, Note 25
Display Flicker	shall not be visible on 50% green image area, Note 26

Table 16. Operating Overall Image Area Appearance

23. red = 255, green = 255, blue = 255
24. red ≤80, green ≤80, blue ≤80
25. red = 0, green = 0, blue = 0; or red = 255, green = 255, blue = 255, respectively
26. red = 0, green = 128, blue = 0

Nonoperating Appearance Defects

Parameter	Condition	Max.	Unit
Surface Foreign Material Diameter, Note 27	$D = \frac{a+b}{2}$, Figure 9	1.0	mm
Surface Foreign Material Occurrences, Note 27		1	dot
Surface Scratch Size, Note 27	width, Figure 10	0.04	mm
	length, Figure 10	0.50	mm
Surface Scratch Occurrences, Note 27		2	scratch

Table 17. Image Area Surface Defects

27. If visible during operating test, refer to dot defect criteria (Table 15).

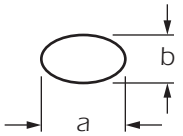

Figure 9. Surface Foreign Material Measurement

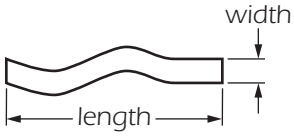

Figure 10. Surface Scratch Measurement

Functional Description

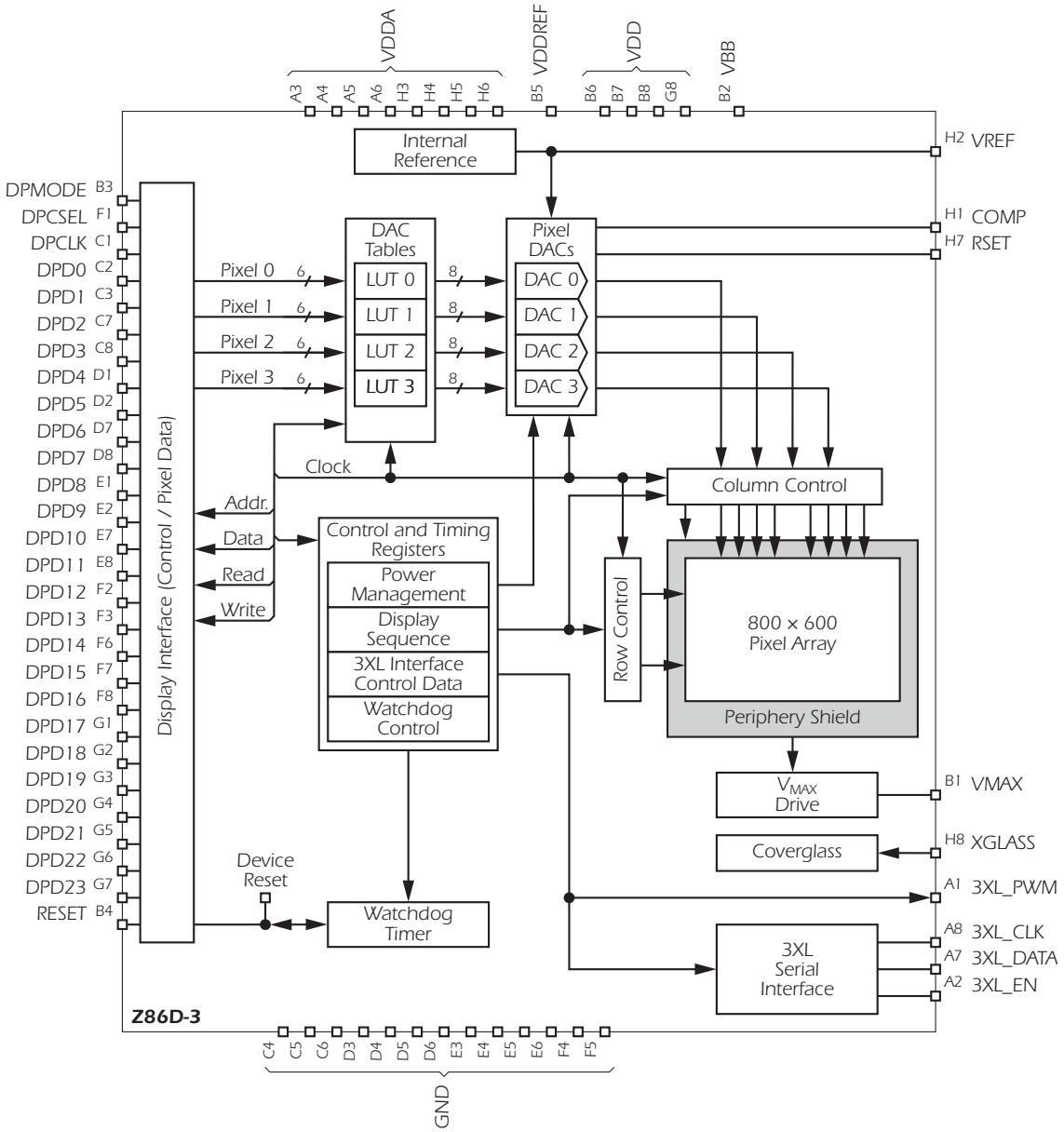

Figure 11. Functional Block Diagram

The Z86D-3 microdisplay is a highly integrated device incorporating a digital pixel and control interface, control registers, look-up tables, DACs (digital-to-analog converters), array control circuits and a pixel array. The interface supports external circuitry, for coverglass voltage generation and illumination LED control (CMD3XLB).

Display Interface

The display interface is a dual-function parallel interface that has two modes of operation: pixel mode and control mode.

Pixel Mode

In pixel mode, the interface accepts four parallel 6-bit (representing 64 grayscale levels) pixel values per pixel-clock cycle. These values are compensated, converted, and sequentially loaded into the array.

Control Mode

In control mode, the interface supports read/write operations to the control register block and look-up tables. The interface accepts 9-bit addresses and transfers 8-bit data and read/write control signals.

Look-Up Tables

Four user-defined look-up tables convert each of the four 6-bit pixel inputs into 8-bit values (inverted or noninverted for each red, green, or blue). This allows color compensation, improved DAC resolution, and the alternating pixel voltage inversion required to drive the pixel array.

Digital-to-Analog Converters

Four identical high-precision DACs (digital-to-analog converters) convert the 8-bit data values output from the look-up tables into the analog grayscale voltages that drive the pixels.

Row and Column Control

The row and column control circuits operate synchronously with the pixel clock to control the routing of the analog signals (four at a time) from the DACs to the columns and rows of the pixel array. These circuits generate the frame and line timing required for correct operation of the microdisplay.

Pixel Array

The image area is an 800×600 pixel array. Additional hidden columns are used for the generation of reference voltages. Pixels consist of a switched metal mirror with an integral capacitor. The capacitance retains the charge (holding a grayscale level) when that pixel is not selected.

Liquid Crystal

The voltage differential across the liquid crystal, between the mirror and a conductive surface on the coverglass, affects the orientation of the liquid crystal. The orientation of the liquid crystal affects light polarization, and when assembled with the proper illumination and polarizing filters, a variation in voltage results in a variation in the gray scale appearance of the pixel. The maximum voltage differential produces black while the minimum voltage differential produces white.

Control Registers

The control registers are accessible from the display interface when in control mode. These registers support various functions and features, such as initiating a pixel data loading sequence, selection of power modes, support of coverglass voltage generation, and control of external illumination LEDs.

Watchdog Timer

A watchdog timer is connected to the reset line on the microdisplay. If the correct signals are not applied within a programmable time, the watchdog may force a reset. The watchdog has its own internal oscillator, and functions regardless of the state of the incoming clock signal.

Illumination Controller Interface

The illumination controller interface is a synchronous 3-wire serial port used to communicate with illumination control circuitry (CMD3XLB) to support the generation of coverglass voltages and control illumination LEDs. Illumination controller data is typically generated by a display interface circuit (CMD8X6DDI or custom ASIC) and is stored in certain Z86D-3 registers for transfer via the illumination controller interface.

Microdisplay Operation

Field-Sequential Color Operation

Z86D-3 microdisplay images are inherently gray scale. To produce a color "frame" (a single full-color image), three separate color "fields", representing the red, green, and blue components of an image, are quickly presented and illuminated individually with corresponding red, green, or blue light.

A practical system configuration actually displays 60 frames per second at 6 fields per frame, in red-green-blue-red-green-blue order, with each color field repeating twice. The field rate in this case is 360 color fields per second. Repeating each color field twice (using the same image) is also useful for averaging the voltage across the liquid crystal.

Voltage Across the Liquid Crystal

Analog pixel signals and coverglass voltages must be inverted on alternate fields. This places a positive voltage across the liquid crystal followed by a negative voltage on the next frame of approximately the same average magnitude. This average coverglass voltage and average analog input voltage must also be approximately the same to produce a time-averaged near-zero voltage across the liquid crystal. This is necessary to prevent deterioration of the liquid crystal.

Color-Field Definition

Each color field consists of three periods: clear, load, and view. For each of these periods, specific timing, pixel data, and polarity-specific and color-specific coverglass voltages are necessary. See Table 18 on page 20.

Color-Field Periods

Each frame, or color field, consists of three distinct periods: clear, hold and view. The significant operations performed during each of these periods are:

Clear Period

- A "frame clear" is applied to set the pixel storage capacitors to a known starting voltage.
- The coverglass voltage is set to the clear value.

Hold Period

- DAC power is enabled.
- Look-up table values for the frame are loaded.
- The coverglass voltage is set to the hold value.
- A "frame start" is applied to initiate the pixel loading sequence.
- A pixel loading sequence is performed by loading the hidden columns and the 800×600-pixel values into the array.

View Period

- DAC power is disabled to minimize power.
- The coverglass voltage is set to the view value.
- The appropriate LED is enabled and the LED power is modulated to establish desired illumination.

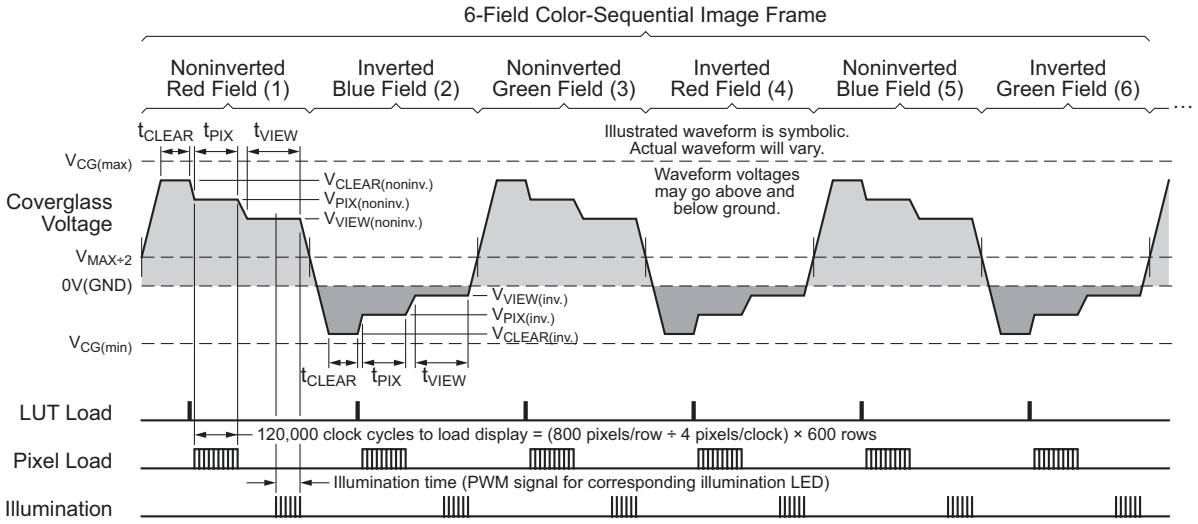

Figure 12. Typical Color Field Sequential Frame Timing

Coverglass voltages are relative to $V_{MAX÷2}$.

Field Color	Noninverted Frame Voltage			Inverted Frame Voltage		
	Clear	Load	View	Clear	Load	View
Red	+2.007V	+2.402V	+2.212V	–2.007V	–2.402 V	–2.212V
Green		+2.007V			–2.007V	
Blue						

Table 18. Sample Coverglass Voltages

Important Table 18 contains sample values only. For the latest coverglass voltages, contact Brillian.

Control Register Programming

Control Mode

The host system uses control mode to read and write the control registers and look-up tables in the Z86D-3. The key functions accessed and performed in control mode include:

- Initialization of the Z86D-3 register values
- Writing of frame specific operating parameters
  - Frame clear operation and writing LUT values for specific color and non-inverted or inverted frames.
- Initiation of the frame pixel loading sequence
  - Frame start write operation
- Dynamic management of frame sequencing and operational parameters
  - Coverglass voltage level settings
  - Selection of red, green or blue LEDs for respective frame data
  - Pulse-width modulation of power to selected LED for control of brightness and color balance
  - 3XL (CMD3XLB) serial data transfers
- Power Management
  - Z86D-3 DAC power control/standby mode
  - 3XL (CMD3XLB) illumination control circuit power control/standby mode

Table 19 on page 21 describes the address space for the control registers and DAC look-up tables accessed in control mode and provides a brief description the functions. Further information on control mode write/read operations, register definitions, and DAC look-up table usage is addressed in the following sections.

Address	Name	Description	Reset Value
000_h–$03F_h$	pixel_0_lut	Look-up-table containing 64 8-bit locations used to map the 6-bit Pixel0_Bit[5:0] input values to 8-bit values delivered to the on-chip DAC.	xx_h
040_h–$07F_h$	pixel_1_lut	Look-up-table containing 64 8-bit locations used to map the 6-bit Pixel1_Bit[5:0] input values to 8-bit values delivered to the on-chip DAC.	xx_h
080_h–$0BF_h$	pixel_2_lut	Look-up-table containing 64 8-bit locations used to map the 6-bit Pixel2_Bit[5:0] input values to 8-bit values delivered to the on-chip DAC.	xx_h
$0C0_h$–$0FF_h$	pixel_3_lut	Look-up-table containing 64 8-bit locations used to map the 6-bit Pixel3_Bit[5:0] input values to 8-bit values delivered to the on-chip DAC.	xx_h
100_h	dac_power_control	Register used to control power mode of the Z86D-3 internal pixel DACs.	00_h
101_h	frame_start	Register used to signal the start of a frame sequence for loading of pixel data.	00_h
102_h	unused_register_102	Unused register.	00_h
103_h	reserved_register_103	Reserved register. Value must be $E1_h$.	$E1_h$
104_h	load_3xl	Register used to trigger the serial transmission of illumination control and coverglass data (to the CMD3XLB).	00_h

Table 19. Control Registers and Look-Up Table Addresses

Address	Name	Description	Reset Value
105_h	watchdog_control	Register used to define the watchdog timer settings.	00_h
106_h	common_voltage_lsbs	Register pair used to define 10-bit value transmitted to the illumination controller (CMD3XLB) for DAC generation of the coverglass voltage.	00_h
107_h	common_voltage_msbs		00_h
108_h	led_enable	Register used to define the red, blue, and green LED Enable values transmitted to the illumination controller (CMD3XL).	00_h
109_h	reserved_register_109	Reserved register. Value must be 80_h.	80_h
$10A_h$	reserved_register_10A	Reserved register. Value must be 03_h.	03_h
$10B_h$	led_pwm_control	Register used to control the state of the 3XL_PWM output pin for pulse-width modulation of power to the LEDs.	00_h
$10C_h$	frame_clear	Register used to clear the pixel array at the start of each frame.	00_h
$10D_h$	3xl_clock_frequency	Register used to set the 3XL_CLK frequency for the synchronous serial interface between the Z86D-3 and the illumination controller (CMD3XLB).	08_h
$10E_h$	3xl_power_control	Register used to define the 3XL power mode value transmitted to the illumination controller (CMD3XLB).	01_h
$10F_h$	reserved_register_10F	Reserved register. Value must be 08_h.	08_h
000_h–$03F_h$	pixel_0_lut	Look-up-table containing 64 8-bit locations used to map the 6-bit Pixel0_Bit[5:0] input values to 8-bit values delivered to the on-chip pixel DAC.	xx_h

Table 19. Control Registers and Look-Up Table Addresses (Continued)

Control-Mode Write/Read Operations

Control mode operations are performed via the display interface when the DPMODE signal is low. In this mode the DPD[23:0] dual function pins are assigned for control mode access: ADDR[8:0], DATA[7:0], WRITE and READ. All operations are synchronized with the falling edge of DPCLK with write or read operations indicated by a high level on the respective WRITE or READ control line. Additionally, the following rules apply when performing write or read operations.

- Control Signals: The WRITE and READ control signals must not be active at the same time and must not remain in an active state when not writing or reading valid address/data information. A minimum of one clock cycle delay must also exist between the READ signal going inactive and the WRITE signal going active.
- DPMODE Transition: A minimum of one clock cycle delay must exist after a transition in DPMODE and the start of a write or read operation.
- Write Cycle: Each write operation requires two clock cycles with sequential write cycles allowed after all other rules are met. The address must be valid and stable for both clocks and the data must be valid during the second clock of the write cycle.
- Read Cycle: Each read operation requires four clock cycles with sequential read cycles allowed after all other rules are met. The address must be valid and stable for all four clocks with the data becoming valid prior to the fourth clock cycle.

Figure 13 shows a typical write cycle, and Figure 14 shows a typical read cycle, for the control-mode operations. See Figure 4 and Figure 5 for detailed ac timing.

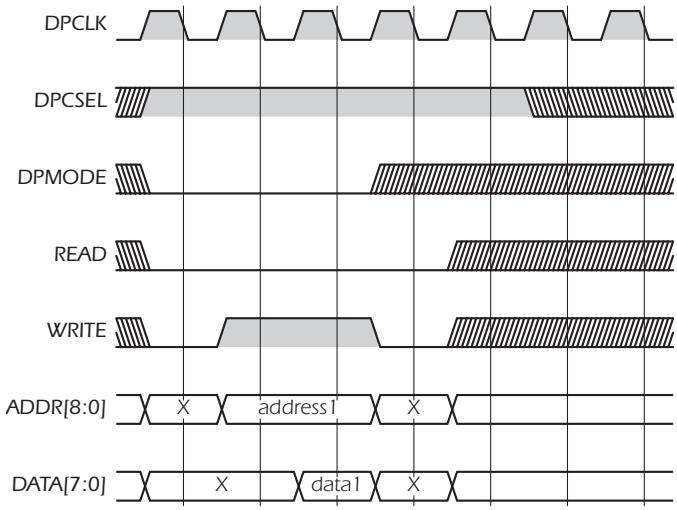

Figure 13. Control-Mode Write Cycle

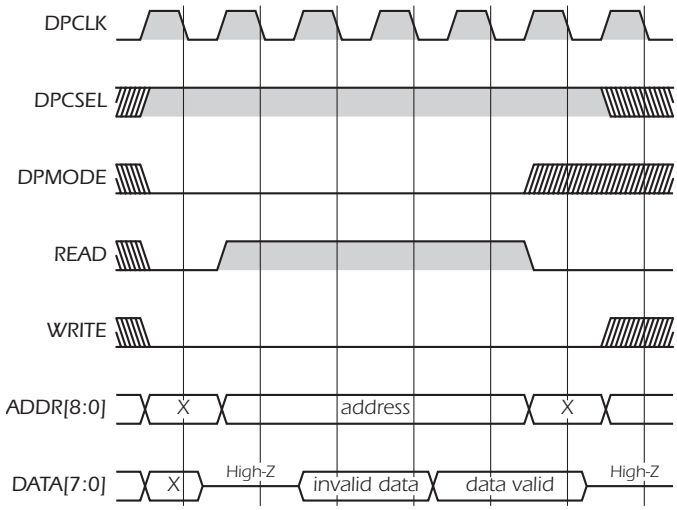

Figure 14. Control-Mode Read Cycle

Control Registers

The following registers are accessible in control mode.

dac_power_control ***Address: 100$_h$***
Type: read/write Reset Value: 00_h

Bit	7	6	5	4	3	2	1	0
Field	X	X	X	X	X	X	X	DACPM

DACPM—DAC Power Mode: “1” = DACs on, “0” = DACs off

frame_start ***Address: 101$_h$***
Type: read/write Reset Value: 00_h

Bit	7	6	5	4	3	2	1	0
Field	X	X	X	X	X	X	X	FS

FS—Frame Start: “1” = start active, “0” = start inactive. Writing a “1” to this field starts the frame loading sequence. This field is automatically cleared after the loading sequence has been initiated.

unused_register_102 **Address: 102_h**
Type: read/write Reset Value: 00_h

Bit	7	6	5	4	3	2	1	0
Field	UNUSED = 00_H							

UNUSED—Unused: Valid Value = 00_h. This register is unused. Writing to this register has no functionality.

reserved_register_103 **Address: 103_h**
Type: read/write Reset Value: $E1_h$

Bit	7	6	5	4	3	2	1	0
Field	RSVD = $E1_H$							

RSVD—Reserved Field: Valid value = $E1_h$. This register is reserved and must remain set to the power up default of $E1_h$.

load_3xl **Address: 104_h**
Type: read/write Reset Value: 00_h

Bit	7	6	5	4	3	2	1	0
Field	X	X	X	X	X	X	X	SD

SD—Send Data: "1" = send/send active, "0" = idle. Writing a "1" to this field causes values contained in the common_voltage_lsbs, common_voltage_msbs, led_enable, and 3xl_power_control registers to be transferred to the illumination controller (CMD3XLB) over the 3XL 3-wire synchronous serial interface. This field is automatically cleared after the loading sequence has been complete. When reading the register, a "1" is returned in this field if a transfer is in process. A "0" is returned after a transfer is complete and/or the interface is idle.

watchdog_control **Address: 105_h**
Type: read/write Reset Value: 00_h

Bit	7	6	5	4	3	2	1	0
Field	DIS	X	X	X	X	X	TO	

DIS—Watchdog Disable: "1" = disable, "0" = enable

TO—Watchdog Timeout: Values written to bits[1:0] define the watchdog timeout period that must expire prior to the device exiting or entering a reset state if evidence of pixel data activity is not been detected.

00_b = 50ms nominal

01_b = 100ms nominal

10_b = 200ms nominal

11_b = 400ms nominal

common_voltage_lsbs **Address: 106_h**
Type: read/write Reset Value: 00_h

Bit	7	6	5	4	3	2	1	0
Field	CGLSB							

CGLSB—Coverglass Voltage LSBs: Defines the lower 8 bits of the 10-bit value transferred to the illumination controller (CMD3XLB) for generation of the coverglass voltage.

common_voltage_msbs **Address: 107_h**
Type: read/write Reset Value: 00_h

Bit	7	6	5	4	3	2	1	0
Field	X	X	X	X	X	X	CGMSB	

CGMSB—Coverglass Voltage MSBs: Defines the upper 2 bits of the 10-bit value transferred to the illumination controller (CMD3XLB) for generation of the common voltage.

led_enable **Address: 108_h**
Type: read/write Reset Value: 00_h

Bit	7	6	5	4	3	2	1	0
Field	X	X	X	X	X	GRN	BLU	RED

RED—Red LED Enable: “1” = enabled; “0” = disabled

BLU—BLU LED Enable: “1” = enabled; “0” = disabled

GRN—GREEN LED Enable: “1” = enabled; “0” = disabled

These fields define the red, green and blue LED enable values transferred to the illumination controller (CMD3XLB). For each red, green or blue color field to be displayed, setting the respective bit to “1” enables pulse width modulation control of the LED brightness via the LED_PWM signal and the illumination controller.

reserved_register_109 **Address: 109_h**
Type: read/write Reset Value: 80_h

Bit	7	6	5	4	3	2	1	0
Field	RSVD = 80_H							

RSVD—Reserved Field: Valid value = 80_h. This register is reserved and must remain set to the power up default of 80_h.

reserved_register_10A **Address: $10A_h$**
Type: read/write Reset Value: 03_h

Bit	7	6	5	4	3	2	1	0
Field	RSVD = 03_H							

RSVD—Reserved Field: Valid value = 03_h. This register is reserved and must remain set to the power up default of 03_h.

led_pwm_control **Address: $10B_h$**
Type: read/write Reset Value: 00_h

Bit	7	6	5	4	3	2	1	0
Field	X	X	X	X	X	X	X	ON/OFF

ON/OFF—LED Power On/Off: “1” = on (LED_PWM pin active); “0” = off (LED_PWM pin inactive). Register used to control the state of the CMOS 3XL_PWM output pin for pulse-width modulation control of power to the LEDs via the illumination controller (CMD3XLB). This register bit maps to the 3XL_PWM output pin.

frame_clear **Address: $10C_h$**
Type: read/write Reset Value: 00_h

Bit	7	6	5	4	3	2	1	0
Field	X	X	X	X	X	X	NEG	POS

POS—Positive Frame Clear: “1” = active (noninverted frame); “0” = inactive

NEG—Negative Frame Clear: “1” = active (inverted frame); “0” = inactive

This register is used to clear the pixel array at the start of each frame. The appropriate POS or NEG bit is selected active to clear the pixel array for the frame polarity (non-inverted or inverted) to be loaded and displayed. The bit must then be cleared prior to starting the loading sequence. Additionally, both the positive and negative frame clear bits should not be set active at the same time.

3xl_clock_frequency **Address: $10D_h$**
Type: read/write Reset Value: 08_h

Bit	7	6	5	4	3	2	1	0
Field	DIV							

DIV—DPCLK Divider: The 8-bit field establishes a DPCLK divider used to generate the serial interface clock frequency for the 3XL_CLK signal used during data transfers to the illumination controller (CMD3XLB). The value defines the number of clocks that are in half the period of the serial interface clock and must be a power of 2. Valid values and the associated 3XL_CLK frequencies are:

DIV field value 3XL_CLK frequency:

02_h = DPCLK÷4

04_h = DPCLK÷8

08_h = DPCLK÷16

10_h = DPCLK÷32

20_h = DPCLK÷64

40_h = DPCLK÷128

3xl_power_control **Address: $10E_h$**
Type: read/write Reset Value: 01_h

Bit	7	6	5	4	3	2	1	0
Field	X	X	X	X	X	X	X	3XLPM

3XLPM—3XL Power Mode: “1” = 3XL power on and DAC bias on; “0” = 3XL power off and DAC bias off. This field defines the value transferred to the illumination controller (CMD3XLB) to control its power mode power state of its on-chip DAC bias circuit.

reserved_register_10F **Address: $10F_h$**
Type: read/write Reset Value: 08_h

Bit	7	6	5	4	3	2	1	0
Field	RSVD = 08_H							

RSVD—Reserved Field: Valid Value = 08_h. This register is reserved and must remain set to the power up default of 08_h.

DAC Look-Up-Tables

The Z86D-3 has four separate look-up tables, one for each of the 6-bit pixel data inputs. These tables permit linearity correction of the grayscale response and allow custom grayscale response curves. They also provide the mechanism to map the pixel data to drive the array for noninverted and inverted frames. Each table has 64 entries, and each entry is 8-bits wide to match the pixel DAC resolution.

The look-up tables must be loaded with the desired color and field polarity data prior to initiating the pixel loading sequence for the frame to be displayed. To minimize the number of write cycles and system overhead required to load these tables, a control mode write to pixel_0_lut address loads the corresponding address of all four tables. In this manner all look-up tables are loaded simultaneously with the same information. When reading data, only data from the specific look-up table defined by the memory map is output to the data bus.

Typical look-up table values, at 80MHz DPCLK and a 360Hz refresh rate, are shown in Table 20.

Table Address		Noninverted Frame Data			Inverted Frame Data		
(6-bit Pixel Value)		Red	Green	Blue	Red	Green	Blue
(Hex)	(Decimal)	(Decimal)	(Decimal)	(Decimal)	(Decimal)	(Decimal)	(Decimal)
00_h	0	0	0	0	255	255	255
01_h	1	37	32	30	218	223	225
02_h	2	47	42	36	208	213	219
03_h	3	55	49	45	200	206	210
04_h	4	61	56	52	194	199	203
05_h	5	67	61	59	188	194	196
06_h	6	72	66	62	183	189	193
07_h	7	77	70	68	178	185	187
08_h	8	80	74	71	175	181	184
09_h	9	84	77	75	171	178	180
$0A_h$	10	87	80	78	168	175	177
$0B_h$	11	90	83	81	165	172	174
$0C_h$	12	93	86	84	162	169	171
$0D_h$	13	96	89	86	159	166	169
$0E_h$	14	99	91	88	156	164	167
$0F_h$	15	101	94	91	154	161	164
10_h	16	104	96	93	151	159	162
11_h	17	106	98	95	149	157	160
12_h	18	108	100	97	147	155	158
13_h	19	111	102	99	144	153	156
14_h	20	113	104	101	142	151	154
15_h	21	115	106	103	140	149	152
16_h	22	117	108	105	138	147	150
17_h	23	119	110	107	136	145	148
18_h	24	121	112	109	134	143	146
19_h	25	124	114	111	131	141	144
$1A_h$	26	126	116	113	129	139	142
$1B_h$	27	128	118	115	127	137	140
$1C_h$	28	130	120	116	125	135	139
$1D_h$	29	132	122	118	123	133	137
$1E_h$	30	134	124	120	121	131	135
$1F_h$	31	136	126	122	119	129	133
20_h	32	138	128	124	117	127	131
21_h	33	141	130	126	114	125	129
22_h	34	143	132	128	112	123	127
23_h	35	145	134	130	110	121	125
24_h	36	147	136	132	108	119	123
25_h	37	149	138	134	106	117	121
26_h	38	152	140	136	103	115	119
27_h	39	154	142	138	101	113	117
28_h	40	156	145	140	99	110	115
29_h	41	159	147	143	96	108	112
$2A_h$	42	161	149	145	94	106	110

Table 20. Sample Look-Up Tables

Table Address		Noninverted Frame Data			Inverted Frame Data		
(6-bit Pixel Value)		Red	Green	Blue	Red	Green	Blue
(Hex)	(Decimal)	(Decimal)	(Decimal)	(Decimal)	(Decimal)	(Decimal)	(Decimal)
$2B_h$	43	163	152	147	92	103	108
$2C_h$	44	166	154	150	89	101	105
$2D_h$	45	168	157	152	87	98	103
$2E_h$	46	171	159	155	84	96	100
$2F_h$	47	173	162	157	82	93	98
30_h	48	176	164	160	79	91	95
31_h	49	179	167	162	76	88	93
32_h	50	181	169	165	74	86	90
33_h	51	184	172	167	71	83	88
34_h	52	187	175	170	68	80	85
35_h	53	190	178	173	65	77	82
36_h	54	194	181	176	61	74	79
37_h	55	197	184	179	58	71	76
38_h	56	201	188	183	54	67	72
39_h	57	205	192	187	50	63	68
$3A_h$	58	209	196	191	46	59	64
$3B_h$	59	214	201	195	41	54	60
$3C_h$	60	221	208	202	34	47	53
$3D_h$	61	228	216	209	27	39	46
$3E_h$	62	239	228	222	16	27	33
$3F_h$	63	255	255	255	0	0	0

Table 20. Sample Look-Up Tables (Continued)

Important *Table 20 contains sample values only. For the latest look-up values, contact Brillian.*

Pixel Mode

Pixel mode operations are performed via the display interface when the DPMODE signal is high. In this mode the DPD[23:0] dual function pins are assigned for pixel mode access: PIXEL0_BIT[5:0], PIXEL1_BIT[5:0], PIXEL2_BIT[5:0], PIXEL3_BIT[5:0]. Pixel loading operations are performed sequentially synchronized with the falling edge of the clock. Once a pixel loading sequence has been initiated, it should not be interrupted, nor should invalid data be provided. The device should also never enter pixel mode when not performing a pixel loading sequence.

The pixels are written into the Z86D-3 sequentially starting at the upper left corner of the pixel array; PIXEL0 being the left pixel and PIXEL3 is the right in a group of four. The rows are sequenced in order with the first row loaded at the top of the pixel array. Figure 15 depicts various signals and their timing when writing a field of pixel data to the pixel array.

The process starts in control mode with a write of a “1” to the frame_start register to reset the internal row and column pointer to “0”. A minimum of one clock cycle must pass before the DPMODE pin can be set high, placing the Z86D-3 into pixel mode. Exactly one clock cycle must pass after the DPMODE pin goes high to allow the Z86D-3 to change modes before writing the first pixel group.

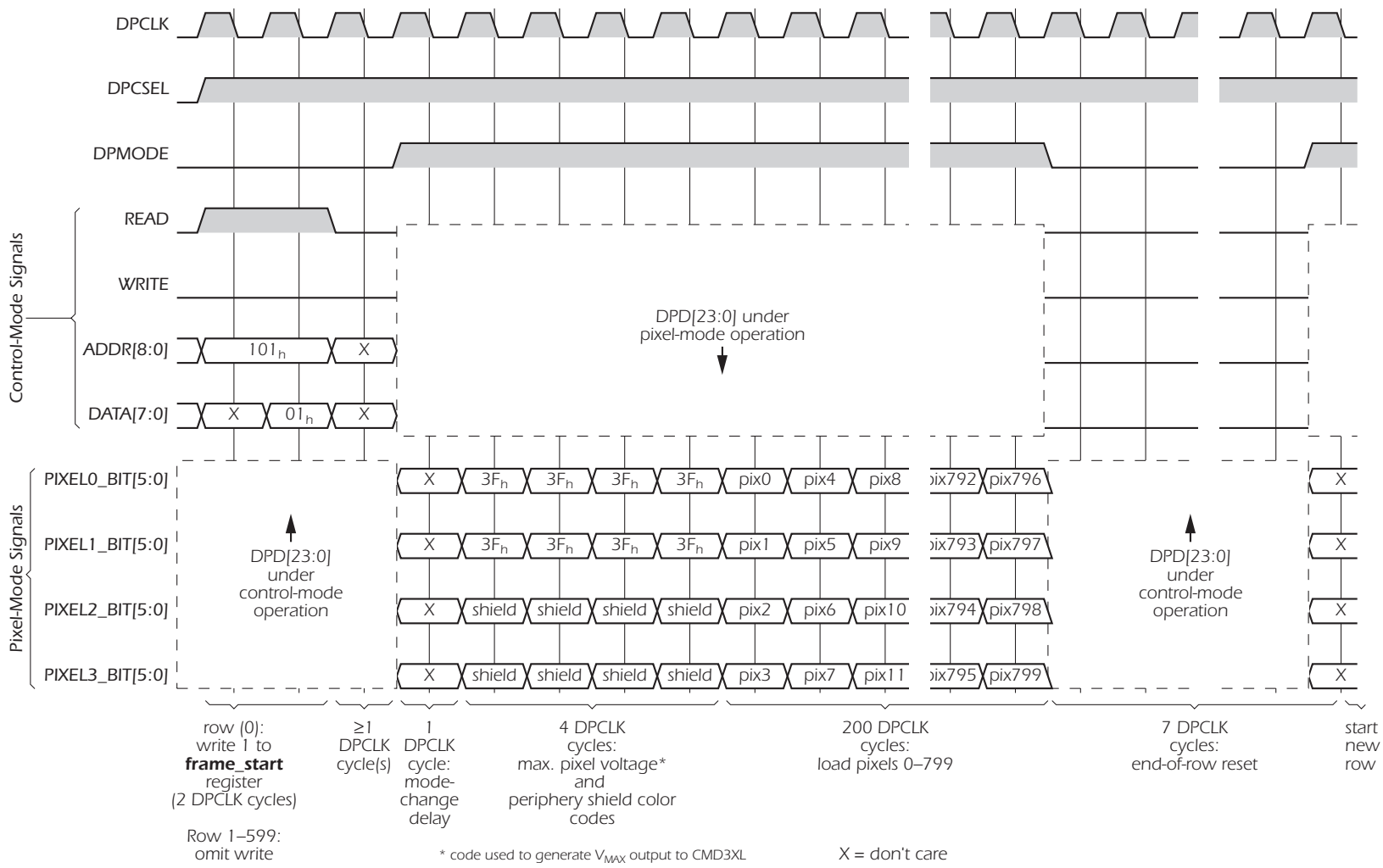

Figure 15. Pixel Loading Sequence

The host then writes pixel data (in groups of four pixels) during the next 204 clock cycles using DPD[23:0] as the pixel data lines. The first four groups contain values to be driven to the hidden columns. These provide the voltage data for the VMAX pin and the periphery shield intensity. The following 200 groups contain the pixel data for the first row of the image. If the DPMODE pin remains high after the 204 groups are written, the following data is ignored. The DPMODE pin must be set low for at least seven clock cycles before it is set high for the next row.

Loading of each of the remaining 599 subsequent rows proceed as described above, with the omission of the write to the frame_start register.

Watchdog Timer and Reset Pin

The watchdog timer is connected to the reset line on the microdisplay. If pixel data is not correctly written to the display within a certain time, the watchdog may force the RESET pin low and reset the Z86D-3 and illumination controller (CMD3XLB) which share the reset pin. The watchdog time period may be configured from 50ms to 400ms nominal as determined by the value contained in the watchdog_control register. The watchdog has its own internal oscillator, giving protection even if the DPCLK pin is inactive.

All of the following events must occur within each watchdog period to allow normal system operation:

- Write an 01_h to the dac_power_control register, address 100_h.
- Write an 01_h to the frame_start register, address 101_h.
- Write an 01_h to the load_3xl register, address 104_h.

Upon a watchdog reset, all registers will be set to their defined reset value. This will cause the watchdog timer to be enabled for a nominal watchdog time period of 50ms. Until such time as all the above watchdog events occur within a 50ms period, the device will remain in a reset state causing any write/read operations or pixel loading operations to be ignored. To gain access to the registers for initialization of the device, the watchdog events must be written to the device within the watchdog period in order to release the device from the reset state.

Note that there are occasions where writing the watchdog events within a 50ms period will not release the device from the reset state. This would occur if the asynchronous watchdog timeout occurs in the middle of the event sequence and therefore all events are not performed within a single watchdog period. To ensure that the watchdog events occur synchronized to a single 50ms timeout period and the device is released from the reset state, the following sequence is recommended:

1. Write an 01_h to the dac_power_control register, address 100_h.
2. Write an 01_h to the frame_start register, address 101_h.
3. Write an 01_h to the load_3xl register, address 104_h.
4. Write an 83_h to the watchdog_control register, address 105_h to disable the watchdog timer.
5. Read the watchdog_control register, address 105_h.
6. If the return value is equal to 83_h proceed to register initialization.
7. If the return value is not equal to 83_h, repeat the sequence.

After initialization of the device registers, the watchdog can remain disabled, or it may be enabled for normal operation via bit 7 of the watchdog_control register. The microdisplay does not require the watchdog timer be enabled for normal operation, but the watchdog must be deactivated and disabled prior to direct writing and reading of the microdisplay. In some cases the watchdog may fail to activate even if the proper sequence is not provided.

The Z86D-3 Reset signal (pin B4) is a bidirectional pin as shown in Figure 16. As an input, this active low signal is intended to be driven from an external source at power-up to ensure that the control registers contain their predefined reset values. As a watchdog reset output, it is intended to be connected to the reset input pin of the illumination controller (CMD3XLB). If the Reset pin is driven from an external source, a current limiting resistor (R1) should be used to protect the source driver as shown in Figure 16. A 1kΩ resistor for R1 should be sufficient for most applications.

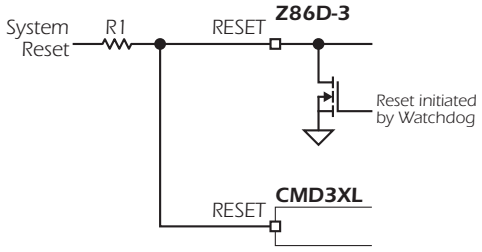

Figure 16. Z86D-3 Reset Pin Circuit

3XL Interface

The 3XL interface is a 3-wire synchronous serial interface that supports communication between the Z86D-3 and illumination controller (CMD3XLB). The signals consist of clock, enable, and data.

Data is transferred from the microdisplay to the external circuitry in the format of a 14-bit control word containing data from the 3xl_power_control, common_voltage_msbs, common_voltage_lsbs, and led_enable registers within the Z86D-3. Transfers are initiated by writing a "1" to the send data bit in the load_3xl register. They occur synchronous to the rising edge of the clock at a rate determined by the value in the 3xl_clock_frequency register. Upon completion of a transfer, the send data bit in the load_3xl register is automatically cleared to zero.

A typical transfer cycle is shown in Figure 17. Notice that there are 15 clock cycles used to transfer 14 bits. The first rising clock edge sets up the transfer, the second rising clock edge gates the first of 14 data bits, etc.

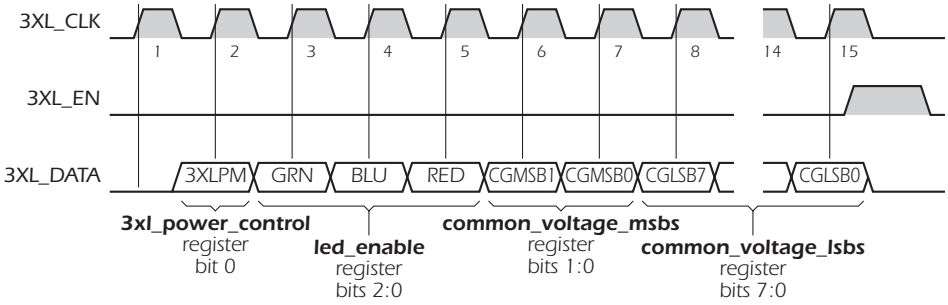

Figure 17. 3XL Serial Interface Transfer Cycle

VMAX Output

The V_{MAX} output voltage (pin B1) is the maximum voltage that can be applied to any pixel from the internal DAC. This output is designed to be used as a reference voltage from which to balance and center the coverglass waveform (pin H8). Voltage balancing of the coverglass waveform is required to ensure that a dc voltage does not develop across the liquid crystal. If a dc voltage offset is allowed to remain across the liquid crystal, it will cause degradation to the liquid crystal material over time. This degradation will appear as image retention and/or flicker.

The VMAX output is basically a high-impedance sample-and-hold circuit. A 0.1µF capacitor on the Z86D-3's BGA substrate holds the voltage between samples. As such, this pin needs to be externally buffered through the VMAX (input) and VMAX_OUT pins of the CMD3XLB illumination controller ASIC or with a low-offset, high-input-impedance buffer op-amp such as a Burr Brown OP340.

RSET Output

The RSET output (pin H7) is a current output that sets the Z86D-3's internal DAC strength for a given DPCLK frequency; that is, the RSET pin controls V_{MAX}. DAC drive, which controls V_{MAX}, affects the perceived image brightness and contrast.

Note *Two circuit configurations are described below. For most applications, the RSET servo circuit (see "RSET Servo Circuit (Preferred)" below) is recommended over the resistor configuration. The RSET servo provides consistent brightness and contrast from one microdisplay to the next. This is especially important in dual-microdisplay applications.*

The RSET servo circuit is mandatory for any application that must support multiple clock frequencies.

Resistor Configuration

In a fixed DPCLK frequency application, a resistor can be connected between the RSET pin and ground to set the DAC drive. The resistor value is a function of the desired V_{MAX} voltage (3.8V nominal) and the DPCLK frequency (f_{DPCLK}):

$$R_{SET} = \frac{1.33 \times 10^{12}}{V_{MAX} \cdot f_{DPCLK}}$$

Example: for V_{MAX} = 3.85V and f_{DPCLK} = 80MHz, R_{SET} = 4.318kΩ

RSET Servo Circuit (Preferred)

The circuit shown in Figure 18 adjusts the RSET pin current, using V_{REF} = 1.202V nominal, to maintain a V_{MAX} output of approximately 3.8V.

$$V_{MAX} = V_{REF} \times \frac{R1 + R2}{R2}$$

U1 in Figure 18 is the buffer described under "VMAX Output" above and can be either the buffer in the CMD3XLB or an external op amp.

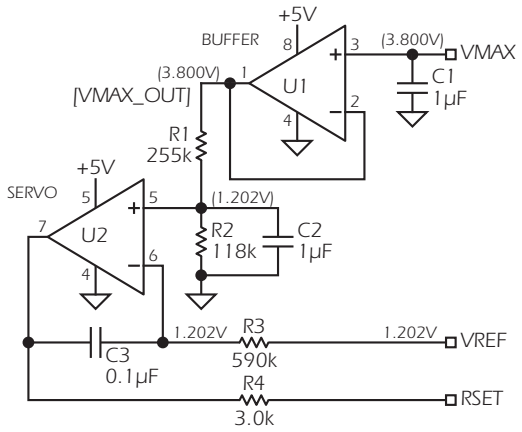

Figure 18. Z86D-3 RSET Pin Servo Circuit

In dual-microdisplay systems, two servo circuits must be used, one for each microdisplay. However, V_{REF} for both circuits should be supplied by only one of the microdisplays to avoid differences in V_{MAX} caused by variations in V_{REF}.

Related Documents

The following data sheets are referenced by this document:

- D00677—*CMD3XLB Microdisplay Illumination Controller ASIC Data Sheet*
- D00170—*CMD8X6DDI Digital Display Interface ASIC Data Sheet*

The CMD3XLB illumination controller, with associated circuitry generate accurate voltages required by the microdisplay and can enable the illumination LEDs. It communicates with the Z86D-3 microdisplay via a 3-wire synchronous serial interface (Refer to Figure 1 on page 1.)

The CMD8X6DDI digital display interface ASIC converts spatial color information to the field-sequential color format required by the Z86D-3, executes all specific timing required to maintain an image without host intervention, and offers several interfacing options for use in both computer graphics and full-speed video applications.

Receiving and Opening Packaged Microdisplays

Microdisplays should be protected against corrosion, deterioration, and physical damage at all times.

Shipment Packaging

- Microdisplays are shipped with an orange protective cover tape, capable of withstanding solder reflow. For proper display operation, the protective tape must be removed after soldering. The protective tape covers the active area as well as the clear aperture area (10.3mm × 7.9mm). See Figure 20 on page 35.
- Microdisplays are shipped in black JEDEC trays.
- A maximum of 5 populated trays is allowed in one sealed bag.
- Each stack is shipped with empty trays on top and bottom of the stack for protection.
- ESD compliant rubber bands are used to secure the stack, one on each end and one in the middle.
- The stacked trays are shipped in a vacuum-sealed ESD bag.
- The purchase order number, part number, and quantity are visible on the sealed bag.

Figure 19 shows Brillian's JEDEC tray population sequence. Brillian recommends that its customers follow this sequence in future handling.

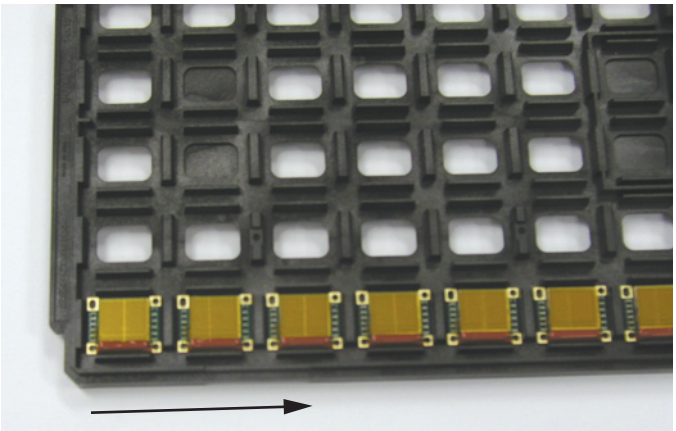

Figure 19. Tray Population Sequence

Package Opening Procedure

Brillian recommends that packages be opened, and tray stacks be removed at a laminar flow bench, using the following sequence:

1. Wipe down the ESD bag with isopropyl alcohol and blow dry with clean compressed air prior to opening the bag.
2. With the vacuum-sealed end of the bag facing a constant stream of clean air, use a razor blade to break the bag seal.
3. Blow off the tray stack, remove the ESD rubber bands and remove the cover tray.
4. Prior to optical assembly, remove the protective tape with tweezers, taking care not to contact the glass or the encapsulant protecting the bond wires.

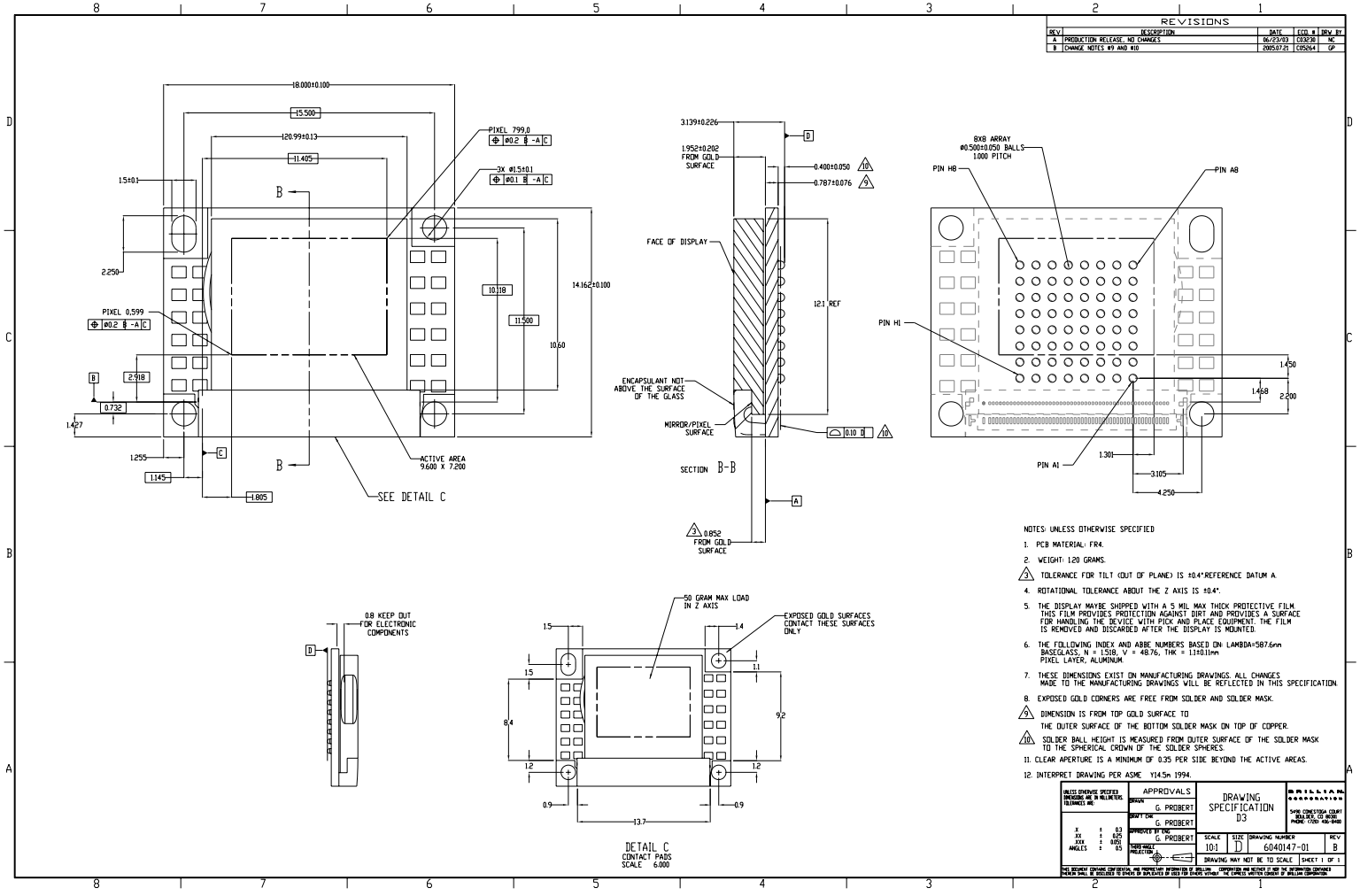

Figure 20. Z86D-3/Z86D-3C Mechanical Dimensions

SYNTAX-BRILLIAN CORP.
1600 North Desert Drive
Tempe, AZ 85281
USA
tel: + 1-602-389-8888 | fax: + 1-602-389-8801
http://www.brilliancorp.com

© 2006 Syntax-Brillian Corporation
Brillian and LCoS are trademarks of Syntax-Brillian Corp.

Syntax-Brillian Corp. advises its customers to obtain the latest version of relevant information before placing orders. Syntax-Brillian reserves the right to make changes to, or discontinue, any product, specification, or service without notice.

Unless otherwise stated in writing by Syntax-Brillian, Syntax-Brillian assumes no liability for Syntax-Brillian applications assistance, customer product design, or software performance. No license, either express or implied, is granted under any patent right, copyright mask work right, or other intellectual property right of Syntax-Brillian, covering or related to any combination, machine, or process in which such microdisplay, optics, interface electronics, or services might be, or are, used.

Evaluation boards or reference designs provided by Syntax-Brillian have not been approved or certified by the FCC (Federal Communications Commission). Evaluation boards and products based on reference designs may not be offered for sale or lease until approval of the FCC and/or other applicable agency has been obtained.

Application Note 06-001

Z86D-3 Lead-Free Soldering Recommendations

Document TD-00101-01-E1

Featured Device

- Z86D-3 SVGA Microdisplay, part #6500007-02

References

- 6065635-01 rev. F; *Production Manufacturing Specification for Syntax-Brillian D3 Personal Display Imagers*
- Spec. No. PDTP0001; *Solder Ball Product Specification Sn42/Bi57*, Accurus Scientific Co., Ltd.

Overview

Introduction

The Syntax-Brillian Z86D-3 microdisplay BGA package is now available with Sn42/Bi58 tin-bismuth solder balls featuring a 0.01% maximum Pb (lead) content for lead-free attachment. For details regarding the solder balls, contact Accurus Scientific directly. See Table 1.

Manufacturer	Accurus Scientific Co. Ltd. 508-51, Wen-Sen Road Section 1, Jen-Der Tainan Country Taiwan 717 tel: +886-6-266-1288 fax: +886-6-366-1276 e-mail: sales@accurus.com.tw
Alloy Composition	42% Sn 58% Bi
Liquidus Temperature	138°C
Solidus Temperature	138°C
Part Number	Sn42/Bi58

Table 1. Solder-Ball Supplier Contact Summary

Note

- **This application note provides a starting point for attachment process development for Z86D-3 microdisplays with Sn42/Bi58 solder balls. This is document not a procedure or specification.**

  The customer is responsible for selecting soldering media (solder past, flux, etc.) that is compatible with their materials, equipment, and processes.

Z86D-3 Handling

- **The Z86D-3 microdisplay is susceptible to hot-plug damage.**

  Turn off power before connecting or disconnecting the microdisplay.
- **The Z86D-3 microdisplay is ESD sensitive (Class 1).**

  Use proper ESD handling procedures to protect the microdisplay from damage.
- **The top of the Z86D-3 microdisplay is glass and is pressure sensitive.**
- **Z86D-3 microdisplays are shipped in a tray in a sealed bag.**

  Do not expose the microdisplays to a strong UV source.

  Do not exceed the published storage temperature.

  Storage of unused microdisplays in N_2 purge is encouraged but not required.
- **The BGA microdisplay is compatible with pick-and-place equipment with appropriate precautions.**

Dos and Don'ts of Lead-Free Soldering of Syntax-Brillian Microdisplays

The following are emphasized in order of importance:

- Do use pad sizes of ≥ 0.020".
- Do use HASL (hot-air solder leveled) finish on the PCB.
- Do inspect solder printed boards for proper alignment and print repeatability before placing parts.
- DO NOT place the part more than 20% off of the pad center as the resulting solder joint will be significantly weaker.
- Do use X-raying as a process development and process check tool to assure no solder bridging or offset issues exist with the reflowed part.
- DO NOT use solder paste after its expiration date.
- Do put a good date tracking system in place to assure the paste is not used after expiration. Discard all expired material.
- Do use all proper handling precautions for microdisplays.
- Do verify all alignment requirements are met.
- Do verify thermal profile.
- Do test attached displays to appropriate environmental requirements.
- DO NOT use water cleaning or any solvent cleaning after assembly.

PCB Surface Finish Requirements

A proper surface finish on the rigid or flexible PCB will help achieve proper adhesion of the Z86D-3 microdisplay to the pads.

Recommended

- Hot-air leveled solder.
- Solder mask opening 3mils larger than pad size.

Acceptable

- LPI (liquid photoimagable) and dry film solder mask.

Solder Paste Application to PCB

- A stencil is recommended for solder paste application if the paste will be applied to one entire side at a time.
- Solder should be at room temperature before application.

Z86D-3 SVGA Microdisplay Placement

Placement methods and procedures should be in accordance with IPC specification IPC-A-610C (Class 2). The following items are especially important:

- Baking is not required prior to assembly.
- Do not remove the protective tape on the microdisplay during the manufacturing process.
- Use light force when placing the display.
- Alignment must be within 4 mils of the pad center (±20% of 20 mil pad).

Reflow

The customer is responsible for developing their reflow process for attaching the Z86D-3 microdisplay. The reflow profile must accommodate the specific thermal characteristics of the board design, component locations, and thermal masses.

Test Boards

The test boards provide a serial connection through all interconnects to allow easier monitoring during the qualification process. A BGA package, thermally similar to the Z86D-3, is also available for profile tests which allows for thermal profile development without risking functional microdisplays.

Thermal Profile

Figure 1 shows the basic features of the solder-ball manufacturer's recommended reflow profile and can be used as a starting point for profile development.

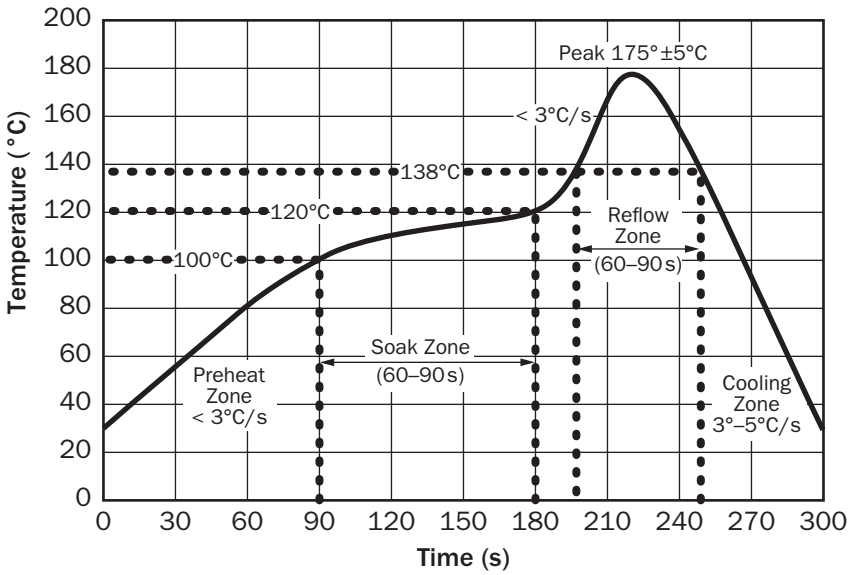

Figure 1. Example Reflow Profile

Profile Development Procedure

The following are some considerations for developing the solder profile.

Preheat Zone

The heating rate in the preheat zone should be less than 3°C/s and the temperature should be approximately 100°C. During preheat, if the temperature ramp is too fast, the solder paste may explode resulting in undesired solder balls. To avoid thermal shock to sensitive components, the maximum heating rate should be controlled.

Soak Zone

The soak zone is intended to bring the temperature of the entire board up to a uniform temperature. The ramp rate in this zone is very low. The temperature is raised to 120°C at the bottom (the melting point of solder is 137°–139°C). The recommended time duration in this zone is 60s to 90s.

Reflow Zone

The peak temperature in this zone should be 175° ±5°C measured by a thermocouple under the BGA solder balls.

The recommended time duration in the reflow zone is 60s to 90s. A longer duration will make the solder joint brittle and reduce resistance to solder joint fatigue.

Cooling Zone

The cooling rate of the solder joint after reflow is also important. The faster the cooling rate, the smaller the grain sizes of the solder and hence the higher the fatigue resistance of the solder joint. The cooling rate should be 3° to 5°C/s.

Profile Development Suggestion

1. Check the surface finishing of the PCBs (or flex).
2. Apply solder paste using a stencil.

   Always inspect the paste profile and appearance for volume variation and paste bridging.

   After finishing the PCB preparation, inspect the board with microscope for uniform level and good flow.
3. Use one PCB as a test board to measure the temperature of the solder joints. Place the tip of a thermal couple between PCB and the microdisplay. A small hole through the PCB, beneath the center of the microdisplay, may accommodate the thermocouple tip. See Figure 2.

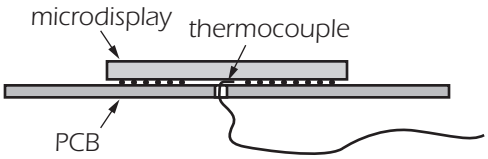

Figure 2. Solder-Joint Temperature Monitoring

4. Create a trial profile. Check the thermocouple readings in each zone, comparing the reading to the sample profile. Modify the temperature settings as needed and perform another trial until the profile almost duplicates the sample profile.

Inspection Guidelines

Perform an inspection of the final assembly. Specifically check for the following problems:

- Occurrence of undesired solder balls or solder microballs.

  In the context of inspection, solder balls or solder microballs are undesired, small spheres of solder, typically in clusters between the device leads and solder mask. Solder balls can violate electrical clearances, result in short-circuits, and are an indication of soldering issues. There are a many articles and resources discussing a variety of causes (such as an incorrect quantity of flux, incorrect preheat settings, incompatible materials, etc.) and solutions. Some of this information is available on the World Wide Web.

- Part misalignment.
- Solder bridging.
- Weak adhesion or poor mechanical connection. After reflow, significant force should be required to separate the microdisplay from the target.

Reflowed solder should have a smooth appearance and a normal fillet should exist.

Printed circuit board inspection information and standards, such as IPC-A-610, available from IPC—Association Connecting Electronic Industries (www.ipc.org), is available from professional and industry associations.

SYNTAX-BRILLIAN CORP.
1600 North Desert Drive
Tempe, AZ 85281
USA
tel: +1-602-389-8888 | +1-602-389-8801
http://www.syntaxbrillian.com

©2006 Syntax-Brillian Corp.
Brillian and LCoS are trademarks or registered trademarks of Syntax-Brillian Corp.

Syntax-Brillian Corp. advises its customers to obtain the latest version of relevant information before placing orders. Syntax-Brillian reserves the right to make changes to, or discontinue any product, specification, or service without notice.

Unless otherwise stated in writing by Syntax-Brillian, Syntax-Brillian assumes no liability for Syntax-Brillian applications assistance, customer product design, or software performance. No license, either express or implied, is granted under any patent right, copyright mask work right, or other intellectual property right of Syntax-Brillian, covering or related to any combination, machine, or process in which such microdisplay, optics, interface electronics, or services might be, or are used.

Evaluation boards or reference designs provided by Syntax-Brillian have not been approved or certified by the FCC (Federal Communications Commission). Evaluation boards and products based on reference designs may not be offered for sales or lease until approval of the FCC and/or other applicable agency has been obtained.