



Features

eIMAG-I is a 24.5 Mpixel pipeline global shutter CMOS Imager for environmental monitoring and machine vision applications.

Pixel

- 5T $6.4\mu\text{m} \times 6.4\mu\text{m}$ Pixel
- 6144×4000 active pixels (2D stitched from an array of 1536×2000)
- Monochrome/color
- Bayer Pattern Color Filter

Readout Channel

- Pipeline Readout
- 3-bit Programmable Gain Amplifier
- Programmable 12-bit SAR ADC
- Delta Sampling
- 48 CMOS IO @ 100Mbps
- Serial Interface

Imager

- Front-side Illuminated
- Global Shutter Mode
- $0.18\mu\text{m}$ CMOS
- 20fps at Full Resolution
- Programmable Region of Interest (down to 8×8 pixels)
- On-chip Regulator and Bias Generation
- Operating range: -40 to $+85$ °C

Power

- 1.8V Digital Supply
 - 0.3W @ 20fps
- 3.3V Analog Supply
 - 0.5W @ 20fps

Status

- Under Development (available early 2017)

Applications

- Environmental monitoring
- Machine vision
- Traffic systems
- Motion monitoring

Description

eIMAG-I functional block diagram is shown in Fig. 1. The Image sensor has an array of 6144×4000 that is divided to a top and bottom sections with independent read-out channels. This allows for simultaneous read-out of the sub-arrays. 2D stitching technique is utilized to achieve resolution of 24.5 Mpixels. The highly sensitive 5T $6.4\mu\text{m} \times 6.4\mu\text{m}$ pixels support both global shutter mode and low-noise rolling shutter mode. The read-out channel consists of column parallel column driver and programmable gain amplifier (PGA) with 3-bit gain setting. Each eight PGA is interfaced with a low-power 12-bit pipeline SAR ADC. The image sensor achieves a maximum frame rate of up-to 20fps at full resolution. It can be programmed to allow read-out from a specific section achieving a higher-frame rate. The image sensor data interface consists of 48 CMOS drivers running at 100Mbps. All the required clock signals and on-chip regulators and bias generation circuits provide all the bias voltages and currents. The Imager consumes 0.3W from a digital 1.8V supply and 0.5W from a 3.3V analog supply at maximum frame rate and resolution. The image sensor is available in monochromatic and color versions.



Clk/Biasing	I/O Pads	I/O Pads	I/O Pads	I/O Pads	Clk/Biasing
	CMOS Driver (6)	CMOS Driver (6)	CMOS Driver (6)	CMOS Driver (6)	
	12-bit SAR ADC (192)	12-bit SAR ADC (192)	12-bit SAR ADC (192)	12-bit SAR ADC (192)	
	COL DRIVER &PGA (1536)	COL DRIVER &PGA (1536)	COL DRIVER &PGA (1536)	COL DRIVER &PGA (1536)	
Row Driver	Pixel Array 1536×2000	Pixel Array 1536×2000	Pixel Array 1536×2000	Pixel Array 1536×2000	Row Driver
Row Driver	Pixel Array 1536×2000	Pixel Array 1536×2000	Pixel Array 1536×2000	Pixel Array 1536×2000	Row Driver
Clk/Biasing	COL DRIVER &PGA (1536)	COL DRIVER &PGA (1536)	COL DRIVER &PGA (1536)	COL DRIVER &PGA (1536)	Clk/Biasing
	12-bit SAR ADC (192)	12-bit SAR ADC (192)	12-bit SAR ADC (192)	12-bit SAR ADC (192)	
	CMOS Driver (6)	CMOS Driver (6)	CMOS Driver (6)	CMOS Driver (6)	
	I/O Pads	I/O Pads	I/O Pads	I/O Pads	

Fig. 1, eIMGA-I block diagram