Monolithic Integration of Telecommunications Wavelength Quantum Dot Lasers on Silicon Substrates

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Outline

• Why integration on Si substrates?
• State of the art
• 1300-nm InAs/GaAs QD lasers on Ge/Si substrates
• 1300-nm InAs/GaAs QD lasers on Si substrates
• Future Work & Markets
• Summary
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Photonic Integration on Si - Advantages

Si offers

- **Cheap substrates** - < 10% cost of GaAs < 3% cost of InP;
- **Large substrates** - up to 450mm dia. compared with 150 mm dia for GaAs and 100 mm dia for InP - economies of processing scale;
- **Advanced processing** - steppers, foundries, small feature sizes;
- **Advanced optical waveguide technology**;
- **Potential for integration with Si electronics** - low cost, reduced parasitics, complex circuits;
- **Large available markets for interconnect, from chip-chip to continent-continent**, achievable if manufacturing cost reduction is realised

ABB/Ericsson
Why Lasers on Si?

Challenge for Si photonics

Various Waveguides

25G Modulator (NEC)

340G APD (Intel)

8 channel WDM (IBM)

-0.8dB Vertical Coupler (Helios)

What is missing in silicon photonics?

Electrically-pumped Lasers
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Challenges for Si photonics

- Although high-performance photonics components, such as modulators, detectors have been developed, SiGe system is not suitable for emitters because of their nature of indirect bandgap;
- Only optically pumped lasers have been demonstrated so far for Si lasers. Electrically pumped lasers are required
- Recently, an electrically pumped Ge laser was demonstrated, though with extremely high threshold current density (~250kA/cm²)

Heterogeneous (hybrid) integration on silicon- UCSB, Aurrion, Intel

- Optical gain from III-V Material
- Efficient coupling to silicon passive photonic devices
- No bonding **alignment** necessary: suitable for high volume CMOS
- All back end processing low temperature (<350 C)

Excellent reported results for 1300-nm III-V QDs from QD Laser Inc.

- High slope-efficiency and temperature-insensitive operation with almost constant threshold-current and slope efficiency between -40 and 100 °C.
- The realization of a *10 Gbit s⁻¹* QD laser that can operate in environments of up to 100 °C.
- Lasing operation up to 200 °C.

Resilience to defects

- Less sensitive to defects than quantum well (QW) lasers
- Stronger mechanical properties to prevent the growth of defects during lasing operation, leading to much longer lifetime for QD laser diodes with higher defect density.

Best reported results of III-V QDs on Si and Ge before UCL work

- III-V QD lasing on Si only achieved ~1 µm with threshold current density of ~900 A/cm² by using MOCVD and MBE systems. A laser with wavelength longer than 1100 nm is required for Si waveguide.
- No room-temperature emission from III-V QD grown Ge substrate reported.
- 1300 nm and 1550 nm are required for telecom applications.

InAs/GaAs QD laser on Si


InAs/GaAs QDs on Ge

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III-V QDs on Ge/Si substrate at UCL

- The Ge/Si substrate is 2 µm Ge epitaxially grown on Si by CVD, with defect density of $5 \times 10^6$/cm$^2$
- Based on TEM results, this approach is the best method to deal with defect generation between GaAs and Si
III-V QDs on Ge/Si substrate at UCL

• Reference 1300-nm InAs/GaAs QDs on Ge substrate were grown under the optimized conditions;
• The PL intensity of QDs on Ge/Si substrate is greater than 85% of that of QDs grown on Ge substrates.
1300-nm QD laser on Germanium on Silicon

- Broad-area laser with 20 µm ridge-waveguide and as-cleaved facets;
- Ti/Pt/Au on the bottom p+ III-V layer;
- Ni/Ge/Au on the top N+ GaAs contact layer;
- Devices of 3-mm and 3.5-mm length were bar-tested.
1300-nm InAs/GaAs QD lasers on Ge/Si

RT 1300-nm QD lasers with 3.5-mm cavity

• First room-temperature CW QD laser on silicon;
• Series resistance: \( \sim 5.0 \Omega \);
• Threshold current densities: 64.3 A/cm\(^2\) (pulsed) & 163 A/cm\(^2\) (CW);
• Output power: 93 mW (pulsed) & 3.7 mW (CW)
• The previously best reported threshold current density for a silicon-based laser is 210 A/cm\(^2\) by direct fusion bonding.

High temperature performance

• Lasing up to **84 °C** (pulsed) and **30 °C** (CW);
• The lower CW operation temperature due to metallisation issues and non-soldered heat-sinking.
High CW Output Power - UCSB

• CW powers over 100 mW routinely achieved.
• Nearly 180 mW maximum CW single side output power at 20 °C from HR coated 1130x10 µm² intrinsic active region (undoped) device.
  • 33% differential efficiency and 18% WPE (at 150 mA)

![Graph showing single side output power vs. drive current for different facet lengths]
Encouraging Reliability Results - UCSB

- Lifetimes up to 2,700 hours already demonstrated

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Challenge for direct GaAs growth on Si

- Native SiO$_x$ within III-V MBE
  - HF etch, difficult to control;
  - Heat to over 850 °C; special design for UCL MBE system.
- AlAs or GaAs prelayer?
- Quantum well filter layers are very useful to filter the defects.
- QW defect filter layers are more effective than QD defect filter layers
1300-nm InAs/GaAs QD lasers on Si

AlAs nucleation layer on silicon substrate:

(a) 5nm GaAs nucleation layer + GaAs buffer

(b) 5nm AlAs nucleation layer + GaAs buffer

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Effect of defect filter layers – InAlAs/GaAs strained superlattice

- High density (~$5 \times 10^9$ cm$^{-2}$) of dislocations is generated at the GaAs/Si interface.
- After the last set of InAlAs/GaAs SLFs, the dislocation density has been remarkably reduced to ~3-5$ \times 10^6$ cm$^{-2}$.
1300-nm QDs on Silicon

- Si (100) substrate with 4° offcut towards the [110] planes;
- InAs/InGaAs dot-in-a-well structure on Si substrate was grown at the optimized conditions as on GaAs substrate
- QD density of $4.3 \times 10^{10}$ cm$^{-2}$;
- Wavelength at 1.3 µm at RT;
- RT PL linewidth of 30 meV, very similar to GaAs-based sample;
- PL intensity is greater than 50% of that for growth on GaAs substrate;
- No defects observed in the QD active region.

TEM image of QD active region.

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Layer structure and device fabrication with contacts on III-V region

- The ridges were etched down to 200 nm below the active region for improved carrier confinement.
- Ti/Pt/Au and InGe/Au were deposited on the p-GaAs contacting layer and the exposed n-GaAs buffer layer, respectively.
- As-cleaved devices of 3 mm length and 50 µm width were mounted and wire bonded on ceramic tiles to enable testing. No facet coating was used.

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InAs/GaAs QD Lasers using InAlAs DFLs and N-Doped Buffer Layer

- 25 µm x 3 mm devices
- Pulsed operation; 1 µs, 1% duty cycle

Threshold current density of 200 A/cm² and an output power exceeding 100 mW at room temperature

Lasing operation up to 111 °C

Electrical Input Power: 300 x 25 x 10⁻⁴ x 0.3 x 1.2 = 270 mW

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Demonstrated continuous-wave InAs/GaAs quantum-dot lasers directly grown on silicon substrates with a low room temperature threshold current density of 62.5 A cm\(^{-2}\), a room-temperature output power exceeding 105 mW, and operation up to 120 °C (pulsed), 75 °C (CW)
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The markets available for this technology are extensive, ranging from core to core interconnects on Si integrated circuits, through chip-to-chip, board-to-board and rack-to-rack interconnects to long-haul optical fibre communications.

An early win for the technology could be reduced cost datacomms. transceivers, through the integration of all optical functions on a single silicon chip with passive optical alignment.

This market opportunity is itself huge, by 2019 > $1.5b for active optical cables in data centres alone (CIR). The initial technology could also be used in WAN and access markets- > $7b by 2019 (Ovum).

Later markets to be addressed would include board-to-board and on-chip interconnects, together with photonic switching.
Integration of photonics on a Si platform is highly attractive for integration with silicon electronics and to reduce substrate cost. Previously, no practical on-chip electrically pumped laser has been available.

We have developed the first successful lasers on Si substrates by direct epitaxy, with threshold current densities as low as 64 A/cm² and output powers of over 100 mW. The practicality of this approach has been confirmed by other groups, who have already achieved excellent reproducibility and encouraging device lifetimes.

In recent work we have demonstrated an extrapolated room temperature CW lifetime of > 100,000 hours.

The markets available for this technology are extensive, ranging from core to core connections on Si integrated circuits, through chip-to-chip, board-to-board and rack-to-rack interconnects to long-haul optical fibre communications - a total market of $200b pa.
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