AIM Photonics
Silicon Photonics PDK Overview

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Silicon Photonics Process Design Kits (PDK)

- PDK– 3 technologies, 2 major releases/year
  - Full (active)- v1.0 available now
  - Passive- v1.0 available now
  - Interposer- v1.0 available now
  - Next: v1.5 (Aug’17), v2.0 (Jan’18)
  - Incremental releases add components & maturity leading to guaranteed specs based on full statistical corner validation

- Extensive Component Library
  - Passive, Active and Interposer components
  - Support for simulation, layout, schematics, DRC, documentation
  - Developed by Analog Photonics LLC (Boston)

- EDA/PDA Design Software Supported

- Download the PDK from MOSIS
  - AIM Membership or license required

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### PDK Passive Components

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Qty</th>
<th>Selected Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Waveguides (Si &amp; SiN), curves, etc.</td>
<td>16+</td>
<td>Si:&lt;2.2dB/cm, SiN:&lt;1dB/cm</td>
</tr>
<tr>
<td>Edge Couplers (Si &amp; SiN)</td>
<td>2</td>
<td>&lt;2.5dB/facet loss</td>
</tr>
<tr>
<td>Vertical Couplers (Si &amp; SiN)</td>
<td>2</td>
<td>&lt;3dB loss</td>
</tr>
<tr>
<td>3dB 4-Port Couplers (Si &amp; SiN)</td>
<td>2</td>
<td>loss &lt;0.5dB, deviation &lt;1%</td>
</tr>
<tr>
<td>Y-Junctions (Si &amp; SiN)</td>
<td>2</td>
<td>loss &lt;0.25dB, deviation &lt;1%</td>
</tr>
<tr>
<td>Directional Coupler (Si &amp; SiN)</td>
<td>2</td>
<td>loss &lt;0.5dB, deviation &lt;1% % @ 1550nm</td>
</tr>
<tr>
<td>Si-to-SiN Coupler (escalator)</td>
<td>1</td>
<td>loss &lt;0.1dB</td>
</tr>
<tr>
<td>Crossing (Si)</td>
<td>1</td>
<td>loss &lt;0.25dB, crosstalk &lt; -60dB</td>
</tr>
</tbody>
</table>

### PDK Active Devices

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Qty</th>
<th>Selected Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Ge Photodetector</td>
<td>1</td>
<td>&gt;30GHz, &lt;20nA dark</td>
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<tr>
<td>Analog Ge Photodetector</td>
<td>1</td>
<td>&gt;25GHz, &lt;80nA dark</td>
</tr>
<tr>
<td>Digital Mach-Zehnder Modulator</td>
<td>1</td>
<td>&gt;15GHz, &gt;25Gb/s, push-pull &lt;2Vpp per arm, &gt;5dB extinction, &lt;5dB loss</td>
</tr>
<tr>
<td>Analog Mach-Zehnder Modulator</td>
<td>1</td>
<td>&gt;15GHz, -10V&lt; Vs &lt;0V, 25dB lin., 1500–1600 nm</td>
</tr>
<tr>
<td>Thermo-Optic Phase Shifter (Si)</td>
<td>1</td>
<td>0.25dB loss, &lt;50mW, range 0&lt;Δθ&lt;2π</td>
</tr>
<tr>
<td>Thermo-Optic Switch (Si)</td>
<td>1</td>
<td>&lt;1dB loss, 25mW</td>
</tr>
<tr>
<td>Tunable Filter (Si)</td>
<td>4</td>
<td>&lt;0.5dB loss, 26nm FSR, &gt;1nm/mW tuning efficiency</td>
</tr>
<tr>
<td>Microdisk Switch (tunable)</td>
<td>4</td>
<td>&lt;2ns switch time, &gt;200GHz EO tuning @ 1.2V</td>
</tr>
<tr>
<td>Microdisk Modulator (tunable)</td>
<td>4</td>
<td>15GHz, 25Gb/s, 1.2Vpp, 1dB Loss, 8dB extinction</td>
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</tbody>
</table>
Silicon Photonics Multi Project Wafer (MPW)

- **2017 MPW Fab Runs**
  - SUNY Poly 300mm fab line
  - 3 MPW offerings
    - Full-Active- 2 runs in 2017
    - Passive Only- 2 runs in 2017
    - Interposer- 1 run in 2017
  - Reservations to be a rider can be started at [http://www.aimphotonics.com/pdk-mpw-sign-up/](http://www.aimphotonics.com/pdk-mpw-sign-up/)
    - Generates quote with terms
    - 20% down to hold slot; balance invoiced at design submission

- **MOSIS is the MPW Aggregator**
  - DRC clean designs (Mentor Calibre) are submitted to MOSIS
  - MOSIS also distributes the PDK

- **MPW Pricing**
  - **FULL**
    - 50mm² chips
      - $100K AIM members
      - $120K non-members
    - 8mm² chips
      - $25K AIM members
      - $30K non-members
  - **PASSIVE**
    - 50mm² chips
      - $30K AIM members
      - $36K non-members
  - **INTERPOSER**
    - 156mm²
      - $93.6K AIM members
      - $112.3K non-members
## 2017-18 Silicon Photonics MPW Schedule

<table>
<thead>
<tr>
<th></th>
<th>2017</th>
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<th>2018</th>
<th></th>
<th>2019</th>
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<tr>
<td></td>
<td>Mar</td>
<td>Apr</td>
<td>May</td>
<td>Jun</td>
<td>Jul</td>
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<tr>
<td>PDK Releases</td>
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<tr>
<td>Run #1</td>
<td>Due</td>
<td>Apr</td>
<td>10</td>
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<td></td>
<td>Full</td>
<td>17-01: MPW Fab</td>
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<td>Run #2</td>
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<td>Due</td>
<td>Sep</td>
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<td>On-Demand</td>
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<tr>
<td>Int 17-01: MPW Fab</td>
<td>Due</td>
<td>Jun</td>
<td>5</td>
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<tr>
<td>On-Demand</td>
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### Notes/Assumptions:

1. DRC clean designs uploaded to MOSIS by the due date for each run
2. Must follow Design Guide in the applicable PDK version
3. MPW Reservations confirmed with 20% down payment; balance invoiced at submission
4. On-Demand runs will only start if economically feasible
This PDK and library enables:

- **Less complex** design
- **Hierarchical** design
- **Design re-use → IP market**
- Large design community
- Latest EPDA methodologies
- **System-level E-O co-design**
- Layout & schematic based flows
- **Photonic schematic capture**
  - drag & drop components
  - *auto waveguide routing
- **Integrated photonic circuit simulation**
- Integrated E-O IC floor-planning
- **2.5D/3D & monolithic** integration
- *Parameter extraction
- DRC & *LVS

(* coming soon)
EPDA Methodologies

Contact these EPDA companies for more info...
...multiple partnerships & integrated solutions
Interesting 2017 Design Enablement Projects

- **Reference Design Project**
  - System level integrated transceiver with PIC and CMOS designs
  - Open and sharable—useful for EPDA methodology development
  - Focus area on E-O co-simulation with verilog-A modeling methodologies

- **Standardized Parameters for Photonic Modeling Project**
  - Collaborate with industry/academia/EPDA
  - Ease PDK creation; define common functions & parameters