An Example Design using the Analog Photonics Component Library

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# Component Library Elements

## Passive Library Elements:

<table>
<thead>
<tr>
<th>Component</th>
<th>Current specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Edge Couplers (Si)</td>
<td>&lt;3dB Loss (1500-1600nm)</td>
</tr>
<tr>
<td>2 Edge Coupler (SiN)</td>
<td>&lt;3dB Loss (1500-1600nm)</td>
</tr>
<tr>
<td>3 Vertical Coupler (Si)</td>
<td>&lt;4dB Loss (C-Band)</td>
</tr>
<tr>
<td>4 Vertical Coupler (SiN)</td>
<td>&lt;4dB Loss (C-Band)</td>
</tr>
<tr>
<td>5 3dB 4-Port Coupler (Si)</td>
<td>&lt;2% Split Ratio Deviation (target 1%)</td>
</tr>
<tr>
<td></td>
<td>&lt;0.5dB Loss (C-Band)</td>
</tr>
<tr>
<td>6 3dB 4-Port Coupler (SiN)</td>
<td>&lt;2% Split Ratio Deviation (target 1%)</td>
</tr>
<tr>
<td></td>
<td>&lt;0.5dB Loss (C-Band)</td>
</tr>
<tr>
<td>7 Y-Junction (Si)</td>
<td>&lt;1% Split Ratio Deviation</td>
</tr>
<tr>
<td></td>
<td>&lt;1dB Loss (C-Band)</td>
</tr>
<tr>
<td>8 Y-Junction (SiN)</td>
<td>&lt;1% Split Ratio Deviation</td>
</tr>
<tr>
<td></td>
<td>&lt;1dB Loss (C-Band)</td>
</tr>
<tr>
<td>9 Directional Coupler (Si)</td>
<td>&lt;4% Split Ratio Deviation (1550nm)</td>
</tr>
<tr>
<td></td>
<td>&lt;0.5dB Loss</td>
</tr>
<tr>
<td>10 Directional Coupler (SiN)</td>
<td>&lt;4% Split Ratio Deviation (1550nm)</td>
</tr>
<tr>
<td></td>
<td>&lt;0.5dB Loss</td>
</tr>
<tr>
<td>11 Si-to-SiN Coupler</td>
<td>&lt;0.25dB Loss</td>
</tr>
<tr>
<td></td>
<td>(TE-Only, 1500-1600nm)</td>
</tr>
<tr>
<td>12 Crossing (Si)</td>
<td>&lt;0.25dB Loss, &lt;-50dB Crosstalk</td>
</tr>
</tbody>
</table>

## Active Library Elements:

<table>
<thead>
<tr>
<th>Component</th>
<th>Specs</th>
</tr>
</thead>
<tbody>
<tr>
<td>13 Microdisk Modulator</td>
<td>&lt;2ns switching time (10-90), &gt;200GHz electro-optic tuning, 1.2V applied; 4 lambdas</td>
</tr>
<tr>
<td>14 Digital Mach-Zehnder Modulator</td>
<td>&gt;10GHz capable, &lt;4Vpp, &gt;6dB extinction</td>
</tr>
<tr>
<td>15 Ge Photodetector</td>
<td>&gt;25GHz, &lt;100nA dark current</td>
</tr>
<tr>
<td>16 Thermo-Optic Phase Shifter (Si)</td>
<td>&lt;25mW/π-phase shift</td>
</tr>
<tr>
<td>17 Analog Mach-Zehnder Modulator</td>
<td>P_{1dB}&gt;20mW, SFDR&gt;100dB/Hz^{2/3}</td>
</tr>
<tr>
<td>18 Analog Ge Photodetector</td>
<td>P_{1dB}&gt;20mW, SFDR&gt;100dB/Hz^{2/3}</td>
</tr>
<tr>
<td>19 Thermo-Optic Switch (Si)</td>
<td>&lt;25mW/π-phase shift, &gt;10dB extinction, 4 lambdas</td>
</tr>
<tr>
<td>20 Tunable Filter (Si)</td>
<td>35nm tuning range, &lt;25mW power, 4 lambdas</td>
</tr>
</tbody>
</table>

## Library Elements

Include:
- Compact model
- Thorough documentation
- Layout abstract
- Schematic and symbol representation
Supported Software Environments

cadence

Synopsys

Mentor Graphics

Phoenix Software
Solutions for Micro and Nano Technologies

Lumerical
Getting The Process Design Kit

Create MOSIS Account & Download

Set Up Software CAD Environment
- Determine a software flow
- Install tech files & display files
- Install simulation models
- Check out documentation
Component Library Documentation

Documentation includes:
- Performance Specifications
- Port names
- Port sizes and types
- Design layer usage
- Thorough placement instructions
- Footprint size and description
How We Create a Library Component

• Design using 3D FDTD/EME with losses and dispersion

• Define universal specs and models

• Create the true geometry and the abstract (for MPW users)

• Verify using wafer scale characterization
Implementing a model: Detector example

- Empirical calibration and complex 3D FDTD simulation

- Symbol and Port Definition

- Geometry/Abstract Definition

![Graph a](image_a)
![Graph b](image_b)
Implementing a model: Detector example

- Use built-in functions for preserving time and frequency domain info

- Aggregate into compact/compound models

- Verify in time and frequency domain

- Finally: Measure!
Hello-World Design Example: Layout & Sim

- 15 Gb/s end-to-end photonic link using a Mach-Zehnder modulator

- This simple design example exclusively uses Component Library elements

- Simple design examples like this will be part of next PDK release
Designer Environment (Cadence Virtuoso)
Example Chip Layout (Cadence Virtuoso)
Example Chip Layout (Cadence Virtuoso)

Chip Frame (Provided)

Simple Design Example

6mm

8.5mm
Simple Example Design: Layout
Simple Example Design: Layout

- Chip Frame (Provided)
- Transmit Block
- Receive Block
- Fiber Array
Transmitter Layout

- Pads for probe/wirebond; Heaters, MZM arms
- MZM Termination Resistor Library Component
- Digital Mach-Zehnder Component
- Edge Couplers
- Silicon Waveguides
Receiver Layout

- Chipframe
- Cleaved Fiber Input
- Edge Coupler Component
- Photodiode Component
- Silicon Waveguide
- Pads for probe/wirebond; Photodiode connections

200um
Modeling the End-to-End Link (Lumerical)

Designer’s view of simulation testbench:

External Electrical Drive
Transmit
Receive
External Drive Electronics Simulation Testbench

PRBS-Driven Push-Pull Electrical Driver

**Top Arm Drive:**
DATA: 15Gb/s, 1Vpp

**Bottom Arm Drive:**
DATA: 15Gb/s, 1Vpp

**Electrical Eye Diagram:**
10-to-90%: ~4ps
Transmitter Simulation Schematic

MZM Specifications:
- Drive voltage: 1 Vpp push-pull
- 10-to-90% transition: ~4 ps
- Datarate shown: 15Gb/s
- Modulator bandwidth: ~15GHz
- Power: 60mW
Photodiode Simulation Schematic

Photodiode Specifications:

- Responsivity: 0.8 A/W
- Footprint:
- Datarate shown: 15Gb/s
- Modulator bandwidth: ~15GHz
- Power: 60mW

Link Optical Eye @ 15 Gbps
Conclusion

• State-of-the-art performance from the first release onward

• The roadmap introduces new components and significantly improves existing components with each subsequent release

• Measured results at a wafer-scale will be fed back into compact models for manufacturing readiness and high yield.

• Many software flows are possible; as industry support for photonics improves, we will take advantage.