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**Report on SRU testing to validate the stack design modification**

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Author(s): Karine Couturier, Stéphane Di Iorio (CEA), Valtteri Pulkkinen, Olivier Thomann, Mikko Kotisaari (VTT)

Summary

One objective of the BALANCE project, addressed in WP3, consists of the development and testing of electrochemical cells, stacks and systems with high performance and durability under reversible SOFC/SOEC operation. At stack level, two designs are considered, one developed at VTT for SOFC operation and one developed at CEA mainly for SOEC operation, both being optimised for reversible SOFC/SOEC operation in WT3.5 during the first year of the BALANCE project.

The present document gathers the available test results obtained at VTT and CEA for the stack design optimisation (WT3.5) and its validation (WT3.6) as well. The optimisation task was finished on time with the assessment of milestone MS2 and the validation step initially planned at Single Repeat Unit (SRU) level is in progress.

About WT3.5, both VTT and CEA partners finalised the development work needed for adaptation of their stack design to reversible SOFC/SOEC operation in the corresponding period. This task is now finished as planned. The main modifications aimed to decrease the pressure drop on both H₂ and air sides and enhance electrical contact by increasing the stack compression level, decreasing the seal thickness and modifying the interconnect design for improved stack electrochemical performance and durability. Preliminary tests carried out in both operating modes validated most of the modifications made both at VTT and CEA.

In regard to WT3.6, as planned, tests in reversible SOFC/SOEC operation have been considered for the two stack designs validation. At CEA, a first test was carried out on a 5-cell short stack (not only a SRU) in order to prepare a next step of the project when 5-cell short stacks are delivered to different partners for testing of G2 cells in reversible SOFC/SOEC operation. It shows that, on the basis of the electrochemical results, no specific issue was encountered with the integration of the G1 cells from DTU (good tightness all along the test, no cell breakage ...). Moreover, performances and durability similar to those of single cells were experienced in similar operating conditions, including the reversible SOFC/SOEC operation. Then CEA stack design can be considered as validated for this kind of operation. Results of a similar test ongoing at VTT will be analysed as soon as available for a fair comparison of both designs.

Key words: SRU testing, stack design modifications, performance and durability, reversible SOFC/SOEC operation
## TABLE OF CONTENTS

1. Introduction ......................................................................................................................................... 4  
   1.1. Description of the deliverable content and purpose ................................................................. 4  
   1.2. Deviation from objectives ............................................................................................................. 4  
   1.3. If relevant: correction actions ....................................................................................................... 4  
   1.4. If relevant: internal property rights ............................................................................................... 4  

2. Stack design and testing ....................................................................................................................... 5  
   2.1. VTT development work ............................................................................................................... 5  
      2.1.1. VTT new stack design description .......................................................................................... 5  
      2.1.2. Stack modelling .................................................................................................................... 5  
      2.1.3. Seal thermomechanical analysis ............................................................................................ 7  
      2.1.4. Stack mechanical design ....................................................................................................... 8  
      2.1.5. Short-stack tests ................................................................................................................... 9  
   2.2. CEA development work ...............................................................................................................13  
      2.2.1. CEA stack description ...........................................................................................................13  
      2.2.2. CEA stack improvement .......................................................................................................14  

2.3. Stack design validation ..................................................................................................................15  

3. Conclusions .........................................................................................................................................20
1. INTRODUCTION

The BALANCE project focuses on the reversible SOFC/SOEC operation of high temperature solid oxide electrochemical systems for an efficient management of the electricity grid when electricity is produced by intermittent renewable energy sources.

In this context, one objective of the BALANCE project, addressed in WP3, consists of the development and testing of electrochemical cells, stacks and systems with high performance and durability under reversible SOFC/SOEC operation. At component level, cells of Generation 1 (G1) are studied in WT3.1, produced in WT3.2 and electrochemically tested in WT3.3 of the project. At stack level, two designs are considered, one developed at VTT for SOFC operation and one developed at CEA mainly for SOEC operation, both being optimised for reversible SOFC/SOEC operation in WT3.5 during the first year of the BALANCE project (see milestone MS2 of WP3). Those stack designs are validated in WT3.6.

1.1. Description of the deliverable content and purpose

The present document gathers the available test results obtained at VTT and CEA for the stack design optimisation (WT3.5) and its validation (WT3.6) as well. The optimisation task was finished on time with the assessment of milestone MS2 and the validation step initially planned at Single Repeat Unit (SRU) level is in progress. A test is ongoing at VTT and will be analysed as soon as measurements completed. At CEA a 5-cell short stack test (not only a SRU) was carried out in order to prepare a next step of the project when 5-cell short stacks are delivered to different partners for testing of G2 cells in reversible SOFC/SOEC operation. Results are presented in this report and compared to those obtained during single cell tests of WT3.3 and the technical targets initially defined at stack level in the project document of work.

1.2. Deviation from objectives

The stack design optimisation phase (WT3.5) was realised on time. CEA focussed its work on the search for pressure loss reduction mainly on air side in SOFC mode. VTT undertook extensive study to achieve the performance requirements in both operating modes with its own stack design.

Due to delay in the G1 cells delivery (end of January 2018) and also in other components supply in each stack design, validation tests (WT3.6) have been postponed and delivery of the present deliverable D3.1 as well. Thanks to each involved partner’s efforts (DTU for cells production, VTT and CEA for stack design validation), a test is now finished at CEA and ongoing at VTT. Moreover, no impact on the other tasks of the project is expected so far.

1.3. If relevant: correction actions

At CEA the first test of WT3.6 has been performed on a 5-cell stack (instead of the planned 1-cell SRU) in order to anticipate solutions for their delivery to other testing partners later in the project (G2 cells characterisation), give an idea of the stack performance and durability with a higher number of integrated cells earlier in the project and allow a precise/proper comparison between G1 and G2 cells in stack environment when available.

1.4. If relevant: internal property rights

Each VTT and CEA stack design is of course subject to internal property and confidential. Exchanges of stack data and drawings are strictly restricted to the BALANCE project consortium and must respect the rules agreed in the project Consortium Agreement.
2. STACK DESIGN AND TESTING

2.1. VTT development work

VTT has done stack design and development work for SOFC stacks. In older version of VTT in-house stack, the interconnect sheets and stack design were dimensioned for stack power up to 500 W in SOFC (about 20 cells) (Figure 1).

The older version achieved good performance levels but some mechanical aspects could be improved i.e. stack assembling was found hard and sealing was inadequate at certain spots. The experience from the older design was a start point for the new stack generation which is used in BALANCE project. Additional motivation to modify the VTT stack design is the creation of new IP.

The primary starting points for the VTT's next generation SOFC-stack design were:

a) as few different components for stack as possible, which contributes to the following point b),

b) easiness of stack assembling, easy and fast, i.e. align-problem-free,

c) output power of 2 kW in SOFC could be reached,

b) state-of-the-art (SotA) performance maintained.

2.1.1. VTT new stack design description

The new stack, like the old one, has been designed for 10x10 cm$^2$ cells, which size is commercially available from several suppliers. The new stack design has been elaborated to include more cells, up to 75 cells for about 2 kW output in fuel cell mode, with internal features improving the stack assembling and reducing issue with alignment for example. The distribution of the inlet gas has been redesigned. The interconnects have also been redesigned. Crofer 22 H (DIN 1.4755 grade) ferritic stainless steel is used as the interconnect sheet material and the design is a laser welded sandwich structure. One of the interconnect sheets is stamped to create the flow channels form. This manufacturing method is highly suitable for upscaling. The stack uses hybrid seals with glass and mica-type compressible materials. A SRU only consists of one type of each three components (cell, interconnect and seal) and is repeated when assembling the stack.

2.1.2. Stack modelling

To achieve SotA performance level of 2 kW output power, the manifold of the fuel and air was optimized to reach three main objectives: minimize the footprint of the stack, minimize the pressure losses inside the stack and homogenize the volume flow between the interconnect channels. Several iterative rounds for flow channel design were made together with CFD-calculations using input/output parameters given in Table 1 below:
Table 1. Operating parameters for fuel and air channel design optimization calculations.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>FUEL COMPOSITION</td>
<td>50% H₂, 50% N₂</td>
</tr>
<tr>
<td>FUEL UTILIZATION</td>
<td>60%</td>
</tr>
<tr>
<td>FUEL INLET TEMPERATURE</td>
<td>600°C</td>
</tr>
<tr>
<td>FUEL OUTLET TEMPERATURE</td>
<td>680°C</td>
</tr>
<tr>
<td>CURRENT DENSITY</td>
<td>0.4 A/cm²</td>
</tr>
<tr>
<td>AIR UTILIZATION</td>
<td>20%</td>
</tr>
<tr>
<td>STACK OUTPUT POWER</td>
<td>2 kW</td>
</tr>
</tbody>
</table>

For air side manifold and channels, the initial calculation from the first design was satisfactory, giving the maximum flow difference between the channels of around 3% (Figure 2). Pressure loss across the stack was higher than wanted but after increasing the manifold size the calculation showed a satisfactory value of ~13 mbar.

![Figure 2. Air volume flow distribution between interconnect channels. The y-axis represents the normalised flow of each channel to the maximum channel flow, which is channel 19.](image)

On fuel side, the initial design proved to be unsatisfactory showing a volume flow difference of 20% between the channels (Figure 3).
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Figure 3. Fuel volume flow distribution between interconnect channels in the initial design. The y-axis represents the normalised flow of each channel to the maximum channel flow, which is channel 19.

With geometrical parameter mapping, the fuel side flow distribution got to acceptable level (about 5% maximum) and the overall pressure drop over the stack by calculations was around 5 mbar (Figure 4).

Figure 4. Left. Fuel volume flow distribution after optimisation by iterations. The y-axis represents the normalised flow of each channel to the maximum channel flow, which is channel 1. Right. Mapping of flow distribution by varying two geometrical parameters of seal geometry. The optimal and chosen values is highlighted with a star.

2.1.3. Seal thermomechanical analysis

The hybrid seals were tested with an in-house built thermomechanical analyser to find the required nominal thickness for the seals to a) achieve a satisfying stack tightness and b) satisfying electrical contacts between the cells and interconnects after heating-up and application of the compression force (Figure 5). As it can be seen, the seal is compressed to 92% of its initial thickness when load is applied after 3 min of recording. The temperature is then increased from room temperature to 700°C, which affects the seal thickness. The seal thickness is decreasing from 92% to 72% of its initial value due to the heat treatment. This measurement is
essential to assess the suitability of the chosen seal material and its initial thickness. Generally, if the seal is thicker than its design value after compression and heating-up, this will lead to lack of electrical contact, and if it is thinner than its design value, the seal performance will be compromised. Leakage tests of the seals had been done in previous project.

![Thermomechanical analysis of the hybrid seal material (first heating-up). The load is applied after 3 min of recording. The normalised thickness of the seal start at 100% at the beginning of the recording (0 min).](image)

**Figure 5.** Thermomechanical analysis of the hybrid seal material (first heating-up). The load is applied after 3 min of recording. The normalised thickness of the seal start at 100% at the beginning of the recording (0 min).

2.1.4. Stack mechanical design

With all the dimensions for stack manifold and channels, seals and interconnect plates, the new stack mechanical design was finalized (Figure 6). The details of the improvement are confidential and are therefore not represented. A separate manifold plate was designed on top of which the stack will be mounted in the test station. This allows for quick change of the stack and separate stack assembly without any need of pipe welding or reconnection between each stack replacement. Small 90-degree corner plates are used during installation to align the seal and stack properly on the top of the manifold. They are removed before heating-up.
2.1.5. Short-stack tests
First in-situ tests were done with 2-cell stacks. Simplified test setup piping and instrumentation diagram can be seen in Figure 7.

![Simplified piping and instrumentation diagram of test set-up.](image)

Figure 7. Simplified piping and instrumentation diagram of test set-up.

Five stack tests were conducted consecutively. Since the first five stack tests were meant to evaluate some stack modifications and the number of DTU cells is limited, it was decided to use commercial cells for the first five stacks. The output power in the first stack test was close to zero. Measurements of seals thickness and interconnects (IC) dimensions showed that the batch of components was not inside the manufacturing tolerances. The seals were too thick and interconnectors too thin, widening the gap between contact layers (IC and cell). The problem had two possible solutions: increasing the compression or using thinner seal...
material. A second stack test was done with same seal thickness, but with increased compression. Poor electrical contact was achieved, thus giving a stack output power of max 25 W. To enhance the electrical contact and output power, thinner seals were ordered. Use of thinner seals improved the performance level which was recorded in the 3rd and 4th stack tests. In the 4th test, output power of 40 W was achieved. However, this was still behind the targeted performance level. Electrical contact issues were still experienced as the main problem. Compensating it further with compression increase led to formation of micro cracks on the cells. Then in order to improve the contact issue, the interconnect design was altered and new interconnects were ordered. The aim of the alteration was to reduce mechanical stress on the cell and thus allow to increase the mechanical load on the stack without cracking the cells. The fifth stack test included the newly designed interconnects and exhibited performance with up to 71 W achieved. Stack test voltages, current and output power are presented in Table 2.

Table 2. SOFC performance at 700°C overview of five stack tests with changes in seal thickness, IC design and stack compression.

<table>
<thead>
<tr>
<th>STACK TEST</th>
<th>#1</th>
<th>#2</th>
<th>#3</th>
<th>#4</th>
<th>#5</th>
</tr>
</thead>
<tbody>
<tr>
<td>OCV Cell #1</td>
<td>1223 mV</td>
<td>1222 mV</td>
<td>1224 mV</td>
<td>1218 mV</td>
<td>1214 mV</td>
</tr>
<tr>
<td>OCV Cell #2</td>
<td>1048 mV</td>
<td>1217 mV</td>
<td>1207 mV</td>
<td>1209 mV</td>
<td>1209 mV</td>
</tr>
<tr>
<td>Maximum continuous current</td>
<td>0.2 A</td>
<td>12 A</td>
<td>15 A</td>
<td>20 A</td>
<td>20 A</td>
</tr>
<tr>
<td>Voltage at maximum continuous current</td>
<td>1000 mV</td>
<td>817 mV</td>
<td>813 mV</td>
<td>815 mV</td>
<td>878 mV</td>
</tr>
<tr>
<td>Seal nominal thickness</td>
<td>100%</td>
<td>100%</td>
<td>94%</td>
<td>94%</td>
<td>94%</td>
</tr>
<tr>
<td>Stack compression</td>
<td>100%</td>
<td>133%</td>
<td>143%</td>
<td>166%</td>
<td>166%</td>
</tr>
</tbody>
</table>

Overview of power output from stack tests 1-5 can be seen in Figure 8 with arrows indicating nominal stack currents for few sections of the tests. In addition, a polarisation curve is illustrated in Figure 9 for the fifth stack where 700 mV is reached at about 0.62 A/cm² at 700°C in SOFC mode, which is a value close to the state-of-the-art. This validates the modifications made to the stack. The scope of these tests is to investigate the initial performance of the stack, mainly to observe issue with electrical contact. The commercial cells used are known to exhibit issue regarding durability and therefore their durability behaviour is not commented here.
After finding the performance of the stack 5 satisfactory, it was transferred from a fuel cell stack test station to a reversible stack test station in order to study the performance in electrolysis mode as well. During the transfer, the stack suffered some inevitable performance loss because of cooling down to room temperature, removal of the operation compression, new compression and heating-up to operation temperature as it can be seen in Figure 9. At 0.24 A/cm² (20 A), the voltage is about 90 mV lower in the rSOC test station compared to the fuel cell test station. Out of this 90 mV, 50 mV are attributed to the degradation during the approximately 100-hour hold in fuel cell mode (Figure 8), therefore it is estimated that the station transfer has caused 40 mV loss, which is low considering that the compression had to be removed during transport. As already mentioned, the commercial cells used are known to have a durability issue and are not representative of the state-of-the-art durability.

Figure 8. Power output of stack tests 1-5 with nominal stack currents at 700°C for few test sections.
Figure 9. Fuel cell iV curves of stack 5 at 700°C before and after the transfer from a fuel cell stack test station to a reversible stack test station. Cell active area 81 cm$^2$, hydrogen electrode flows 1.39 NLPM H$_2$ and 1.39 NLPM N$_2$, air flow 4.98 NLPM.

The performance in electrolysis mode was then tested with two steam-to-hydrogen ratios (Figure 10):

1. 80/20 as set in WT3.3 Test procedure for the reversible SOFC/SOEC operation for single cells,
2. 90/10 for a more application oriented condition.

The current density reached at 1300 mV is 0.37 A/cm$^2$, which is below the state-of-the-art for SOEC stack. This can be explained by the degradation during the hold in fuel cell mode and the transfer to the reversible test station. This performance in electrolysis mode will be more relevant for the BALANCE project when G1 cells from DTU will be used, which is planned for the next stack. This will allow direct comparison between single cell results and stack results using the same type of cells.
Figure 10. Electrolyser IV curves of stack 5 at 700°C. Cell active area 81 cm$^2$. Hydrogen electrode flows were 1.05 NLPM H$_2$O and 0.26 NLPM H$_2$ for the 80/20 ratio and 1.19 NLPM H$_2$O and 0.13 NLPM H$_2$ for the 90/10 ratio. Air flow was 1.98 NLPM.

2.2. CEA development work

2.2.1. CEA stack description

The CEA stack design is planar and cross-flow. The stack is composed of (Figure 11):

- thin interconnects using 0.2 mm AISI441 ferritic stainless steel sheets with in-plane interconnect dimensions of 205 x 205 mm$^2$ and 2 thick endplates,
- H$_2$ electrode supported cells with a 100 x 100 mm$^2$ active surface area,
- contact elements added between the interconnects and the cells with the same size as the electrodes: a nickel-mesh (100 meshes·cm$^{-2}$) on the hydrogen side and a LSM contact element on the oxygen side,
- ceramic glass Schott G018-311 seal. A mica foil is used to ensure the electrical insulation between two adjacent interconnects, but also to complete the sealing and to position the cell precisely.
2.2.2. CEA stack improvement

At CEA, stack design modifications have been carried out to decrease the pressure drop by a factor higher than 2 on the air side, which was considered to be necessary for an optimum use in SOFC mode (Figure 12). It can been seen that the modifications were efficient, the pressure drop was decreased by a factor higher than 2 for a given air flow rate.

![Figure 12. Pressure drop evolution as a function of the inlet air flow rate before and after stack modification.](image)

It was then checked at SRU level that those modifications did not degrade the performance for instance in SOEC mode. Indeed similar iV curves and ASR evolution as a function of the inlet gas flow were demonstrated before and after modification in this operating mode (Figure 13).
2.3. Stack design validation
As mentioned previously, the CEA stack design was validated on a 5-cell short stack with G1 cells from DTU following a full testing protocol (electrochemical characterization of performance and durability at different temperatures and testing conditions) similarly to what was defined in WT3.3 at single cell level. This validation test aims to allow comparison with single cell performances, try to de-convolute the stack design effect from the cell effect and evaluate durability in more realistic operating conditions (700°C and 90%H2O/10%H2 gas composition at the H2 electrode). Figure 14 shows the overall 1080-h test including performance measurements (iV curves and EIS diagrams), short initial steady-state periods at ±0.5 A/cm² and 700°C in SOFC and SOEC modes and 23 cycles (about 625-h duration) at same electrical current and temperature in reversible SOFC/SOEC operation as well. The reversible SOFC/SOEC operation was a little bit shortened due to schedule constraints of the test station used at CEA. Nevertheless, as demonstrated below, the present test allows to conclude on stack design validation assessment as required in BALANCE project.

At 700, 750 and 800°C, it is shown that initial cells performance is homogeneous within the stack in both operating modes, cell n°5 being the best one and cell n°4 the worst one due to cell manufacturing reproducibility or gas distribution/electrical contact in the short stack (see Figure 15 for 750°C which is the temperature mostly studied at single cell level). Moreover, stack tightness appears very good and stable all along the test as OCV values higher than 1.2 V are achieved under 50%H2/50%N2 when a full stabilisation time is applied. In particular, it means that DTU G1 cells have been successfully integrated in the stack even if it was the first time that this type of cell (dimensions and thicknesses of the different layers) was integrated into CEA stack design. Thanks to EIS measurements, the initial ohmic resistance Rs can be evaluated for each cell. It appears that Rs values are globally at the top of the range given at single cell level. For example, they are comprised between 0.22 and 0.27 W cm² at 750°C in the stack instead of 0.14 W cm² obtained for the best single cell. This difference of electrical contact highly contributes to the global ASR values which also belong to the upper range measured for single cell.

Finally, the best cell presents very similar performances to the G1 single cell in identical testing conditions with current density at 750°C higher than 0.6 A/cm² at 0.77 V in SOFC mode and lower than -0.75 A/cm² at 1.23 V in SOEC mode. At this stage, it is quite difficult to separate the stack design effect from the cell effect: for sure, both are involved but evaluation of their respective contribution is not obvious. On the one hand, cell manufacturing reproducibility is not perfect. On the other hand, cell n°5 is very often the best one in CEA 5-cell stack which is probably due to a more efficient gas distribution for this top cell and/or a thermal effect coming from the stack design/mounting configuration in the test station (higher temperature on the top of stack).
the stack compared to the bottom, in particular in SOFC mode, for a good thermal homogeneity of the furnace and a good tightness of each RU). In any case, a difference lower than 20% is measured on current density at a given voltage between the single cell and the five short stack cells as defined in stack performance targets of the BALANCE project.

Figure 16 below summarises the initial performances of cell n°5 at the three different temperatures (700, 750 and 800°C) and in the three different fuel gas compositions (H₂/N₂ – 50/50; H₂O/H₂ – 80/20 and 90/10).

Figure 14. Cells voltage evolution as a function of time, test performed on a 5-cell stack with G1 cells at CEA.
Figure 15. Initial iV curves at 750°C obtained in SOFC and SOEC modes on a 5-cell stack with G1 cells at CEA.
Figure 16. Initial iV curves of cell n°5 at 700, 750 and 800°C obtained in SOFC and SOEC modes on a 5-cell stack with G1 cells at CEA.

In regard to durability at ±0.5 A/cm², trends similar to the single cell (750°C) are observed at 700°C with the short stack (see Figure 14). **Low degradation is experienced in steady-state SOFC operation** with a maximum voltage degradation rate of -7 mV/kh (-0.9%/kh) for cell n°4 and a voltage degradation rate close to 0 for cell n°2 (small performance improvement). **A higher voltage degradation rate is also calculated in steady-state SOEC mode** with an average voltage degradation rate of 97 mV/kh (8%/kh) for cells n°2 to 5 and a maximum voltage degradation rate of 200 mV/kh (16%/kh) for cell n°1 (Figure 17). Except for cell n°1 which shows an exceptionally high degradation in steady-state SOEC operation, **those voltage degradation values are in the range which is observed at single cell level** (0.2 to 3.5%/kh in SOFC mode and 3.3 to 7%/kh in SOEC mode). Nevertheless the values in SOEC mode are still higher than the stack degradation targets of the BALANCE project (below 2%/kh).
In reversible SOFC/SOEC operation, as for single cell, a higher degradation is observed in SOEC mode than SOFC one and degradation slowly decreases all along the test in both modes for all cells (see in Figure 14 and Figure 18). Indeed, for example at 700°C, ASR increase at intermediate IV curves recorded after 13 reversible cycles is higher than the one measured after 23 cycles in particular in SOEC mode. On the four last cycles, voltage degradation rate in SOEC mode is divided by more than 2 for cells n°1 and 5 (7.2 and 3.2%/kh respectively). It must be noticed that those values include a small thermal effect as stack temperature increased a little bit with stack voltage (no more than few degrees) during operation (stack behaviour being less and less endothermal and even a little exothermal at the end). After 23 reversible SOFC/SOEC cycles, those values are closer but still higher than the stack degradation targets of the BALANCE project.

Figure 18. ASR evolution all along the test, at 700°C in both SOFC and SOEC gas conditions on a 5-cell stack with G1 cells at CEA.

Thanks to EIS measurements, it is also demonstrated that the ohmic resistance Rs is almost constant during the overall test for all cells while ASR, consequently the polarisation resistance Rp, is increasing (see Figure...
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19 and Figure 20 at 700°C for RU2 and 4 as examples). Moreover it seems that the great part of the degradation occurs in the same frequency region than the one mentioned at single cell level. A more accurate comparative analysis of single cell and stack EIS results has to be done before conclusion on that point.

Figure 19. EIS diagrams of RU2 and 4 all along the test, at 700°C in SOEC gas conditions on a 5-cell stack with G1 cells at CEA.

Figure 20. Rs evolution of RU2 and 4 all along the test, at 700°C in both SOFC and SOEC gas conditions on a 5-cell stack with G1 cells at CEA.

3. Conclusions

About WT3.5, both VTT and CEA partners finalised the development work needed for adaptation of their stack design to reversible SOFC/SOEC operation in the corresponding period. This task is now finished as planned.

At CEA, design modifications were made in order to successfully decrease the pressure drop mainly on the air side for SOFC operation, without any degradation of the stack electrochemical performances.

At VTT, stack design was modified with new interconnects (better manufacturability and reduce mechanical stress), optimised seal design to homogenise pressure drop across the different channels and features to improve the ease of large stack assembly. These modifications were assessed with five stack tests.

The results from four first stack tests were not satisfying. The stack performance level was lower than initial targets. Post-mortem analyses of first two stacks showed that the most probable reason is an electrical contact issue between interconnector plates and fuel cells. To overcome this problem, an increase in initial stack compression of more than 65% and decreasing the thickness of the seal material by more than 5% were experimented. The enhancement of the electrical contact was experienced but increasing the compression even further led to formation of micro cracks in the cells. During the test, this was observed as degradation level increased. Post-mortem analysis showed oxidized nickel on the H₂ electrode side, which indicates oxygen leaks through micro cracks from the O₂ electrode.
Then additional geometrical design changes were made to interconnect plates to prevent the formation of micro cracks with the increased stack compression level. A decrease in mechanical stresses induced to the fuel cell was analysed with simulations. The new interconnect led to significantly improved performances. These tests validate most of the modifications made to the VTT stack, since these modifications are expected to be independent of the cell used in the stack.

The stack has been characterised in fuel cell and electrolysis modes with commercial cells. The next step is the assembling of a new short stack including the DTU G1 cells and its test in reversible SOFC/SOEC operation to verify the good integration of DTU cells and compare performance with single cells.

In regard to WT3.6, as planned, tests in reversible SOFC/SOEC operation have been considered for the stack designs validation. The first test of a CEA short stack shows that, on the basis of the electrochemical results, no specific issue was encountered with the integration of the G1 cells from DTU (good tightness all along the test, no cell breakage ...). Moreover, performances and durability similar to those of single cells were experienced in similar operating conditions, including the reversible SOFC/SOEC operation. Then CEA stack design can be considered as validated for this kind of operation. Results of the test ongoing at VTT will be analysed as soon as available for a fair comparison of both designs.