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Ferroelectric transistors with monolayer molybdenum disulfide and ultra-thin aluminum-doped hafnium oxide

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In this letter, we demonstrate ferroelectric memory devices with monolayer molybdenum disulfide (MoS2) as the channel material and aluminum (Al)-doped hafnium oxide (HfO2) as the ferroelectric gate dielectric. Metal-ferroelectric-metal capacitors with 16 nm thick Al-doped HfO2 are fabricated, and a remnant polarization of 3 μC/cm2 under a program/erase voltage of 5 V is observed. The capability of potential 10 years data retention was estimated using extrapolation of the experimental data. Ferroelectric transistors based on embedded ferroelectric HfO2 and MoS2 grown by chemical vapor deposition are fabricated. Clockwise hysteresis is observed at low program/erase voltages due to slow bulk traps located near the 2D/dielectric interface, while counterclockwise hysteresis is observed at high program/erase voltages due to ferroelectric polarization. In addition, the endurances of the devices are tested, and the effects associated with ferroelectric materials, such as the wake-up effect and polarization fatigue, are observed. Reliable writing/reading in MoS2/Al-doped HfO2 ferroelectric transistors over $2 \times 10^7$ cycles is achieved. This research can potentially lead to advances of two-dimensional (2D) materials in low-power logic and memory applications. Published by AIP Publishing. [http://dx.doi.org/10.1063/1.4991877]

A ferroelectric dielectric is a polar dielectric in which the polarization can be switched between two or more stable states by the application of an electric field. Ferroelectric random access memory (FRAM) utilizes ferroelectric polarization switching for data storage. In a FRAM cell, the dipoles tend to align themselves with the field direction when an external electric field is applied to the dielectric structure. The dipoles retain their polarization state after the electric field is removed. Therefore, FRAM is ideally non-volatile. Among non-volatile memories, FRAM consumes much less read/write power than magnetoresistive RAM (MRAM) and phase-change RAM (PCRAM),1 and has better endurance than resistive RAM (RRAM).2–4 While spin-transfer torque magnetic random-access memory (STT-RAM or STT-MRAM) has the advantage of lower power consumption, the amount of current needed to reorient the magnetization is at present too high for most commercial applications.5

Traditional ferroelectric materials are primarily complex perovskites, such as lead zirconate titanate (PZT), strontium bismuth tantalate (SBT), and lead magnesium niobate-lead titanate (PMN-PT).6,7 FRAMs based on complex perovskites have demonstrated superior energy efficiency and endurance.8,9 However, these traditional ferroelectric materials have limited thickness scaling and are not compatible with CMOS processes, making them difficult to be adopted in the semiconductor industry. In the last few years, doped metal oxides, including hafnium oxide (HfO2) and zirconium oxide (ZrO2), were found to possess a ferroelectric phase.10–19 Ferroelectric HfO2 has the advantages of a high coercive field, excellent scalability (down to 2.5 nm), and good compatibility with CMOS processing.16,18,20,21

HfO2 and ZrO2 doped with silicon (Si),10,22–24 yttrium (Y),12 aluminum (Al),13 gadolinium (Gd),14 strontium (Sr),15 and lanthanum (La)16 have been confirmed to possess a ferroelectric phase. The phase transitions in these metal oxides were found to be very sensitive to capping layers and substrates, which determine the internal stresses of the film and crystalline phases. The phase transition is also very sensitive to film composition and annealing temperature. For Al-doped HfO2, a high annealing temperature (ranging between 650 and 1000°C) is required to realize the phase transition.13 FRAMs based on Al-doped HfO2 on silicon have shown excellent endurance and retention.16 However, to further scale down the ferroelectric transistors, an ultrathin body in the semiconductor channel is needed. Two-dimensional materials can address this issue—the atomically thin body of 2D materials can effectively suppress the so-called short-channel effect. Graphene, transition metal dichalcogenides (TMDCs), and black phosphorus (BP) have been investigated intensively over the past few years. Particularly, graphene and MoS2 based on traditional ferroelectric materials, including PZT, SBT, and PMN-PT, have been shown to possess promising memory windows.25–30 However, memories based on 2D materials and ferroelectric HfO2 hybrid stacks are still unrealized.

In this paper, we demonstrate ferroelectric transistors based on Al-doped HfO2 and monolayer MoS2. To characterize the ferroelectricity of the Al-doped HfO2, we fabricated ferroelectric capacitors with TiN electrodes and 16 nm HfO2 doped with Al. A remnant polarization of 3 μC/cm2 is observed at a 5 V programming voltage. 10-year retention of the ferroelectric Al-doped HfO2 is demonstrated. Consequently, ferroelectric transistors with embedded Al-doped HfO2 and monolayer MoS2 channel are fabricated, followed by the systematic characterization of the hysteresis effect and endurance of the transistors. Additionally, wake-up and fatigue effects were observed during the endurance test.
The structure of the ferroelectric capacitors with Al-doped HfO₂ is shown in Fig. 1(a). The 16 nm HfO₂ with 5.9 mol. % Al was deposited via atomic layer deposition (ALD) and annealed at 1000 °C for 1 s to induce ferroelectricity in the insulator material. The details of the capacitor fabrication are in the supplementary material.

The polarization of the capacitors was measured using the positive-up–negative-down (PUND) method. The capacitors are subjected to a series of five pulses consisting of a preset pulse, a positive switching pulse, a positive non-switching pulse, a negative switching pulse and a negative non-switching pulse, as illustrated in Fig. 1(a). The preset pulse sets the ferroelectric HfO₂ in negative spontaneous polarization $-P_s$ state. The first positive pulse applied (P) will switch the polarization vector into the $+P_s$ state and the displacement current for this “non-switching” pulse is

$$i_n(t) = \frac{\partial D}{\partial t} = \frac{\partial(\epsilon E + P)}{\partial t}, \quad (1)$$

where $P$ is the polarization due to the ferroelectric dipoles, $E$ is the electric field, and $\epsilon$ is the dielectric constant of the dielectric. Since the film has already been polarized positively $+P_s$, applying the second positive pulse (U) will not switch the polarization, and the displacement current for this “non-switching” pulse is

$$i_{ns}(t) = \frac{\partial(\epsilon E)}{\partial t}. \quad (2)$$

The difference between the two currents is therefore given by

$$\Delta i(t) = i_s(t) - i_{ns}(t) = \frac{\partial P(i)}{\partial t}. \quad (3)$$

The polarization can then be extracted from $P(t) = \int_0^t \Delta i(i) \, dt$. The change in current as a function of time was measured using a Keithley semiconductor parameter analyzer (model 4200-SCS) equipped with a 4225-PMU ultra-fast I-V module. Figure 1(b) shows the extracted polarization as a function of electric field in various voltage ranges for a capacitor annealed at 1000 °C for 1 s. A clear hysteresis loop is observed, indicating the formation of the ferroelectric phase in this Al-doped HfO₂. The remnant polarization was seen to increase monotonically with the program/erase voltage. At 5 V program/erase voltages, the remnant polarizations reach 3 μC/cm², indicating ferroelectricity in these Al-doped HfO₂ dielectrics.

The retention characteristics of the ferroelectric capacitors were also measured. Figure 1(d) shows the polarization as a function of retention time for a capacitor with an area of $8.1 \times 10^{-5}$ cm². The program/erase pulses are ±5 V and ±4 V, with a 1 μs rise/fall time and a 0.1 μs pulse width. The polarization was measured using the PUND method. We can see that the polarization is nearly unchanged with time for the range we have tested (up to 4600 s). The solid lines are the fitting of the experimental results. From the results, we can extrapolate that more than 89% of the original polarization still remains after 10 years.

Ferroelectric transistors with monolayer MoS₂ and Al-doped HfO₂ were fabricated. The device structure is shown in Fig. 2(a), and an optical image of the device is shown in the inset of Fig. 2(b). The channel width is 3 μm, and the channel length is 7.8 μm. These transistors have an inverted gate structure, i.e., the gate and ferroelectric gate dielectrics are embedded under the MoS₂ channel. Since the high temperature annealing of the HfO₂ film is needed to convert the film into the ferroelectric phase, forming the ferroelectric gate dielectric prior to transferring the MoS₂ can minimize the thermal budget and the potential damage to the MoS₂. The device fabrication is detailed in the supplementary material. The DC characteristics of these devices were systematically measured. Here, we use degenerated p⁺ silicon and the Ti layer as the bottom gate.
The hysteresis effects of the MoS₂ ferroelectric transistors are shown in Figs. 3(a) and 3(b). A clockwise hysteresis is observed when the gate voltage sweep is in the small voltage range (7 V), and counterclockwise when the gate voltage sweep is in the large voltage range (10 V). A similar trend is also observed in the \( I_D \sim V_G \) characteristics after program and erase pulses, shown in Figs. 3(c) and 3(d). Here, the pulse width is 5 \( \mu s \), and the pulse amplitudes are ±7 V [Fig. 3(c)] and ±10 V [Fig. 3(d)]. At low program/erase voltages (e.g., 7 V), the \( I_DV_G \) shifts in the positive direction after a positive gate pulse, corresponding to a clockwise hysteresis loop, while at high program/erase voltages (10 V), the \( I_DV_G \) shifts in the negative direction instead after a positive gate pulse, corresponding to a counterclockwise hysteresis loop in the double gate voltage sweep measurements. These phenomena can be explained by the two competing mechanisms that influence the threshold voltages: charge trapping and ferroelectric polarization switching. At low program/erase voltages, if the electric field in the Al-doped HfO₂ is lower than the coercive field, then the program/erase voltage is not high enough to switch the polarization of the dipoles, so charge trapping phenomenon dominates. Figures 4(a) and 4(b) illustrates the impact of the slow bulk traps on the threshold voltage shift. A positive pulse will cause the energy band of the semiconductor at the gate dielectric/semiconductor interface to bend downward, resulting in more bulk traps located close to the interface to move below the Fermi-level, which tend to capture electrons. A negative gate pulse will bend the band upward and cause more slow traps to move above the Fermi-level and release electrons. This will increase the threshold voltage after the positive gate pulse and decrease it after the negative gate pulse, which is consistent with the experimental observation at low program/erase voltages as shown in Fig. 3(c). At high program/erase voltages, if the electric field in HfO₂ is higher than the coercive field, the program and erase voltage will switch the polarization in HfO₂ film. Figures 4(c) and 4(d) illustrate the impact of ferroelectric switching on the threshold voltage shift. A negative pulse will switch the polarization vector to a \(-P_s \) state, which will induce positive charges in the MoS₂ channel and increase the threshold voltage. A positive pulse will switch the polarization vector in HfO₂ to a \(+P_s \) state, which will induce negative charges in the MoS₂ channel and result in a decrease in the threshold voltage. This is
The coercive electric field (PE) measured in the capacitors, we would expect the minimum gate voltage required to change the polarization in HfO$_2$ to be 9.3 V. This is consistent with our experimental observation that the ferroelectric hafnium oxide and molybdenum disulfides grown by chemical vapor deposition ferroelectric HfO$_2$. The “wake-up effect” corresponds to the initial increase in the number of switchable polarization domains, resulting in the widening of the ferroelectric memory window. Explanations such as domain wall de-pinning have been offered to account for this effect. The second effect, “Polarization fatigue,” corresponds to degradation in the polarization states after a high number of switching cycles. All of the devices demonstrated counterclockwise cycle loops, indicating that they are ferroelectric.

In summary, we have demonstrated ferroelectric transistors based on monolayer MoS$_2$ and ultra-thin ferroelectric Al-doped HfO$_2$. Ferroelectric capacitors with 16 nm HfO$_2$ doped with Al show a remnant polarization of 3 $\mu$C/cm$^2$ under a program/erase voltage of 5 V. The retention measurements of the ferroelectric HfO$_2$ capacitors show that more than 89% of the original polarization remains after 10 years. Ferroelectric transistors based on embedded ferroelectric hafnium oxide and molybdenum disulfides grown by chemical vapor deposition monitored to ensure that there is no significant current tunneling of charge carriers into the floating gate.

An important criterion for nonvolatile memory devices is the long-term endurance, i.e., how many program/erase cycles it can sustain before it becomes unreliable. For ferroelectric memory devices, this translates to the long-term stability of the switchable polarization states. The endurance of the MoS$_2$ ferroelectric transistors were tested with program/erase voltages of $\pm$10 V and pulse width of 5 $\mu$s. Figure 5(a) shows the drain current as a function of gate voltage for a MoS$_2$ ferroelectric transistor after 10000 cycles of program/erase operations. The threshold voltages of the MoS$_2$ ferroelectric transistors after the positive and negative gate pulses, $V_{TP}$ and $V_{TN}$, were extracted by the linear fitting of the $I_D-V_G$ curves at high fields. The threshold voltage difference between these two states, $\Delta V_T = V_{TN} - V_{TP}$, was plotted as a function of program/erase cycles, shown in Fig. 5(b). As the number of program/erase operation increases, $\Delta V_T$ first increases (up to 1000 cycles) and then starts to decrease. The widening of the memory window at the early stage is due to the “wake-up” effect, while the shrinking of the memory window after 1000 cycles is attributed to the fatigue effect of the ferroelectric materials. Two stages of polarization change have been reported not only in conventional lead zirconate titanate (PZT) materials but also ferroelectric HfO$_2$. The “wake-up effect” corresponds to the initial increase in the number of switchable polarization domains, resulting in the widening of the ferroelectric memory window. Explanations such as domain wall de-pinning have been offered to account for this effect. The second effect, “Polarization fatigue,” corresponds to degradation in the polarization states after a high number of switching states. All of the devices demonstrated counterclockwise cycle loops, indicating that they are ferroelectric.

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were then fabricated, and the hysteresis and endurance of the ferroelectric transistors were studied. At low program/erase voltages, a clockwise hysteresis was observed due to charge trapping of slow interface states, while at high program/erase voltages, a clockwise hysteresis was observed due to ferroelectric polarization switching. We demonstrate reliable writing/reading in MoS2/Al-doped HfO2 ferroelectric transistors over 2 × 104 cycles. In the endurance test, the wake-up effect was detected at an early stage of the program/erase cycles and fatigue effect was observed in the late stages of the cycles, which is a characteristic behavior of ferroelectric materials. These ferroelectric transistors can open up a path to extend the scaling of ferroelectric memory.

See supplementary material for the fabrication of ferroelectric Al-doped HfO2 capacitors and ferroelectric MoS2 transistors.

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