RMT® MACHINE VISION

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T-COR-31

FPGA IP-CORE FOR AUTOMATIC TRACKING OBJECTS IN VIDEO

The T-COR-31 FPGA IP core implements the algorithm of automatic tracking of objects in video and calculation of their parameters for solving guidance and target designation tasks. The IP core is a stand-alone module easily integrable into projects based on field-programmable gate arrays (FPGA) and application-specific integrated circuits (ASIC). The core interfaces are universalized for connection to IP cores of other manufacturers. The use of the T-COR-31 IP core will allows you to create your own effective machine vision systems for solving problems in fire control, weapons guidance and perimeter control with a significant reduction of the development time.

FIELD OF APPLICATION

The IP core can be used in smart sights, portable and stationary target acquisition systems, unmanned aerial vehicles, weapon stations, fire control systems, anti-aircraft complexes and homing heads.

HOSTING PLATFORMS AND COMPATIBILITY

The FPGA IP core can make use of any computer modules based on microcircuits manufactured by Xilinx® and Altera® companies. Besides, the core can be adapted for use in application-specific integrated circuits (ASIC). Owing to easy integration, fast prototyping is possible for evaluation of the IP core performance characteristics. The device is compatible with Xilinx® Vivado and Altera® Quartus IDE systems.

DELIVERY AND REQUIRED RESOURCES

The T-COR-31 IP core is supplied as file archives to be included into Xilinx® Vivado IDE projects or as a QSP file and VERILOG file with description of input/output ports for Altera® Quartus IDE system. Below is the list of resources required for FPGA Xilinx® 7 series ICs.

Parameter	Utilization of resources
LUT	38685
FF (Registers)	45146
BRAM	82
DSP	116

PROCESSING TIME FOR A SINGLE FRAME

Results for 150 MHz project frequency

Size of tracking strobe (WxH)	Time, ms
128x128	25
128x64	13
64x64	6.5
64x32	3.5

MAIN CHARACTERISTICS

- Tracking up to 80 fps at core clock frequency 300 MHz and object size of 128x128 pixels.
- The library implements 1 tracking channel. If several channels are required, several cores need to be used.
- Tracking of objects is possible in the size range from 8x8 to 128x128. Channel parameters can be changed in times of tracking.
- Tracking is possible for all types of objects of any shape. There is no tracking collapse if up to 50% of object area changes over no less than 50 frames.
- Tracking when an occluder overlaps up to 50% of object area. Tracking collapse is automatically detected and the object is re-captured after detection.
- Discreteness of coordinate calculation is not less than 1/256 pixels. Discreteness of motion speed calculations is no less than 1/256 pixels/frame.
- Tracking of dynamic objects. Possible translation of object over 1 frame is by 52 pixels in any direction.
- Tracking of low-contrast objects against a complex background. Tracking of objects with a contrast from 10% is possible.
- Calculation of the position and size of object in the tracking rectangle. It is possible to resize the strobe without tracking collapse and object re-capture.
- Adaptation is possible to your conditions of use (changing of operation modes, control logic, algorithm modification).
- Easy integration. The core is supplied in a form convenient for use in Xilinx® Vivado and Altera® Quartus IDE systems.

COMPLEMENTARY OPTIONS

IP cores of interfaces for video data input/output, telemetery transmission can be supplied for fast development of projects based on the T-COR-31 IP core. For the use in projects featuring extremely high frame rate, processing time for a single frame can be reduced 4 fold without significantly increasing the required resources.