Modeling Edge Placement Error Performance of EUV and DSA Multipatterning Processes

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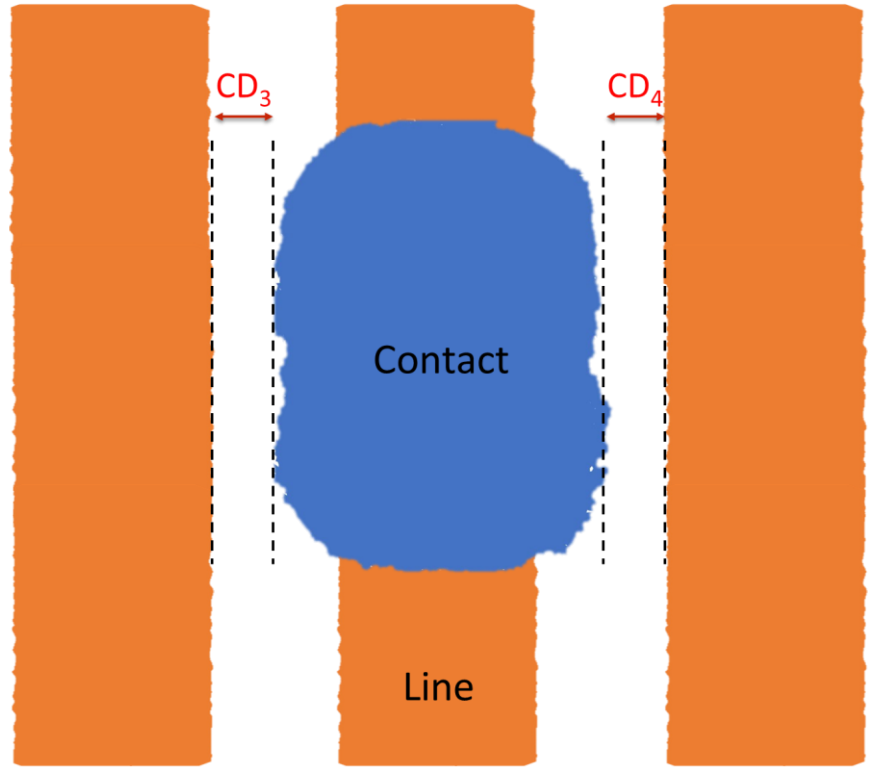
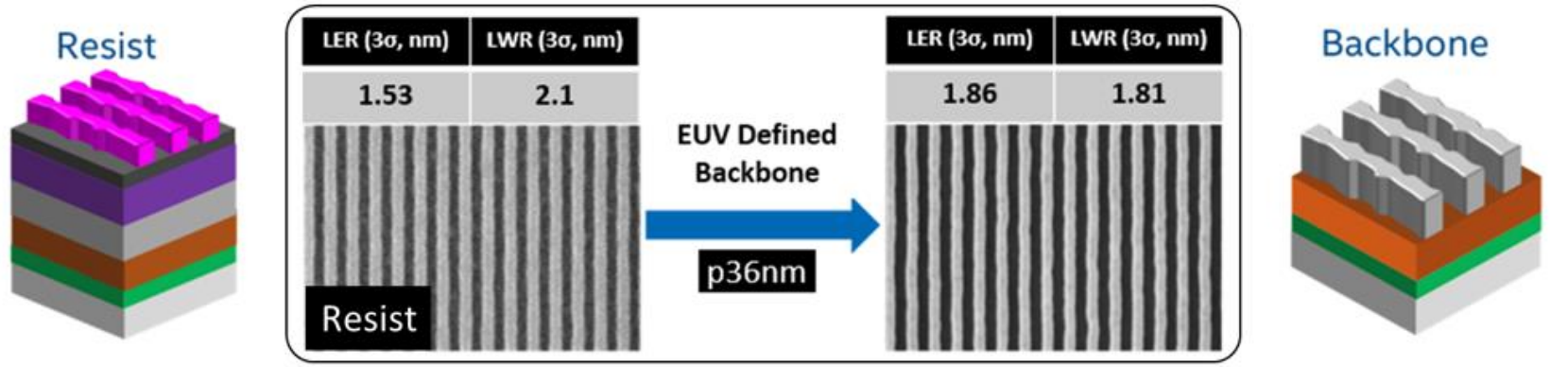
Study Goals

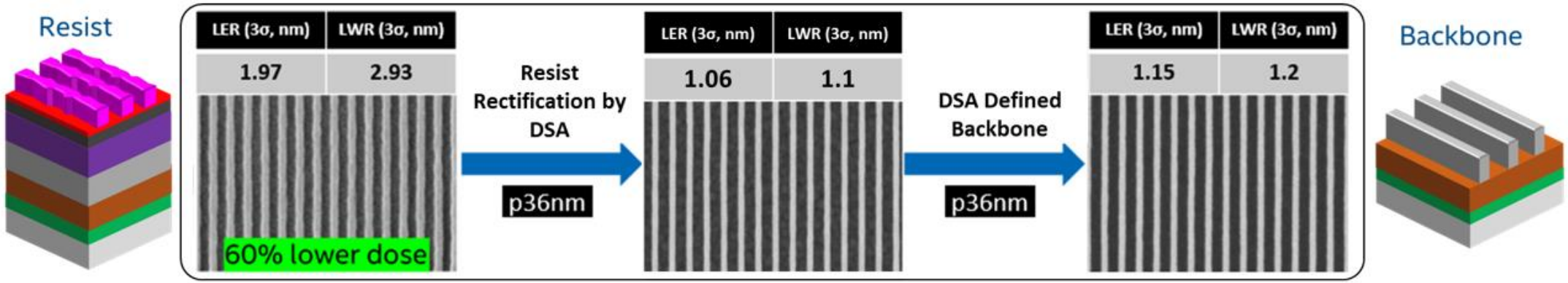
- Consider via landing on a dense array of lines
  - Misaligned via touching a neighboring line results in device failure
- Grating patterns with 18/21 nm pitch can be fabricated with two process flows:
  - A) EUV printed 36/42 nm pitch + SADP
  - B) DSA rectified 36/42 nm pitch + SADP
- Goal: By measuring stochastic variability of each process layer, predict the yield impact of EUV versus DSA rectification



Process Flows



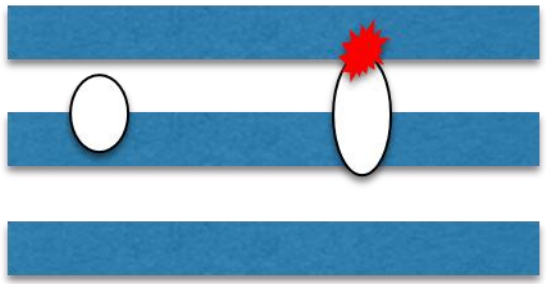
Conventional Flow



DSA based EUV Rectification Flow

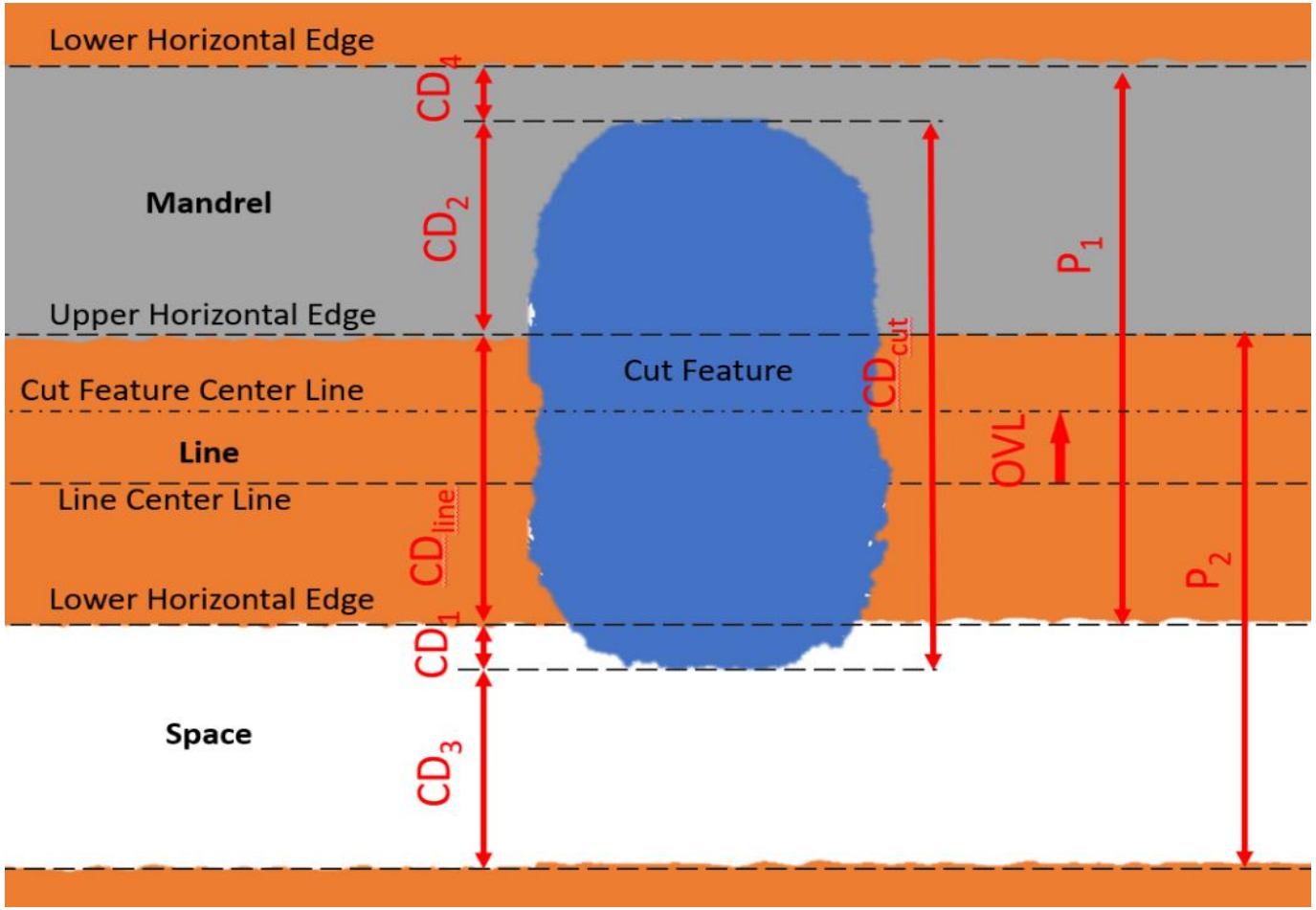
Gurpreet Singh, “Continuing Moore's Law with next-gen DSA”, Proc. SPIE PC12497, *Novel Patterning Technologies 2023*, PC124970D (2023).

Prior Work: EPE Model for Complementary Lithography



Two failure mechanisms:

- An incomplete cut
- Cutting a neighbor feature

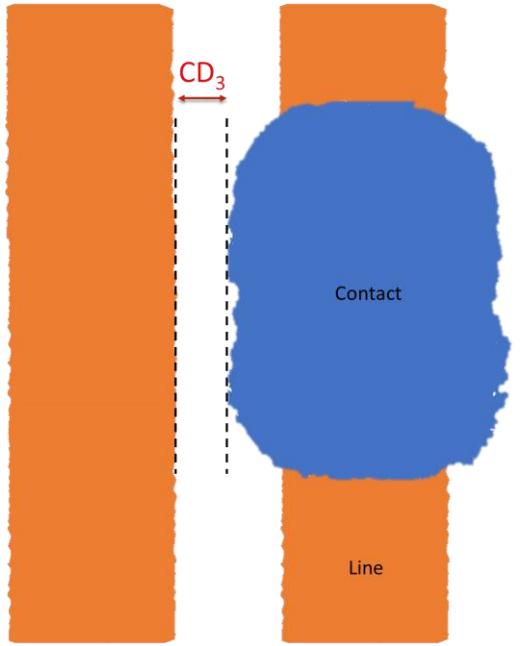


Chris A. Mack and Michael E. Adel "Overlay and edge placement error metrology in the era of stochastics", Proc. SPIE 12496, *Metrology, Inspection, and Process Control XXXVII*, 1249609 (2023).

Applying New Stochastic EPE Modeling Approach

1. Write down Geometric equations for EPE (traditional way)

$$CD_3 = Pitch - \frac{CD_{via}}{2} - \frac{CD_{line}}{2} + OVL$$



2. Take the Variance of this equation

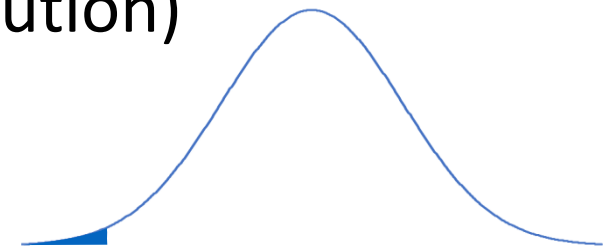
$$\sigma^2_{CD_3} = \frac{1}{4}\left(\sigma^2_{CD_{via}} + \sigma^2_{CD_{line}}\right) + \sigma^2_{OVL}$$

3. Find the stochastic contributors to each term

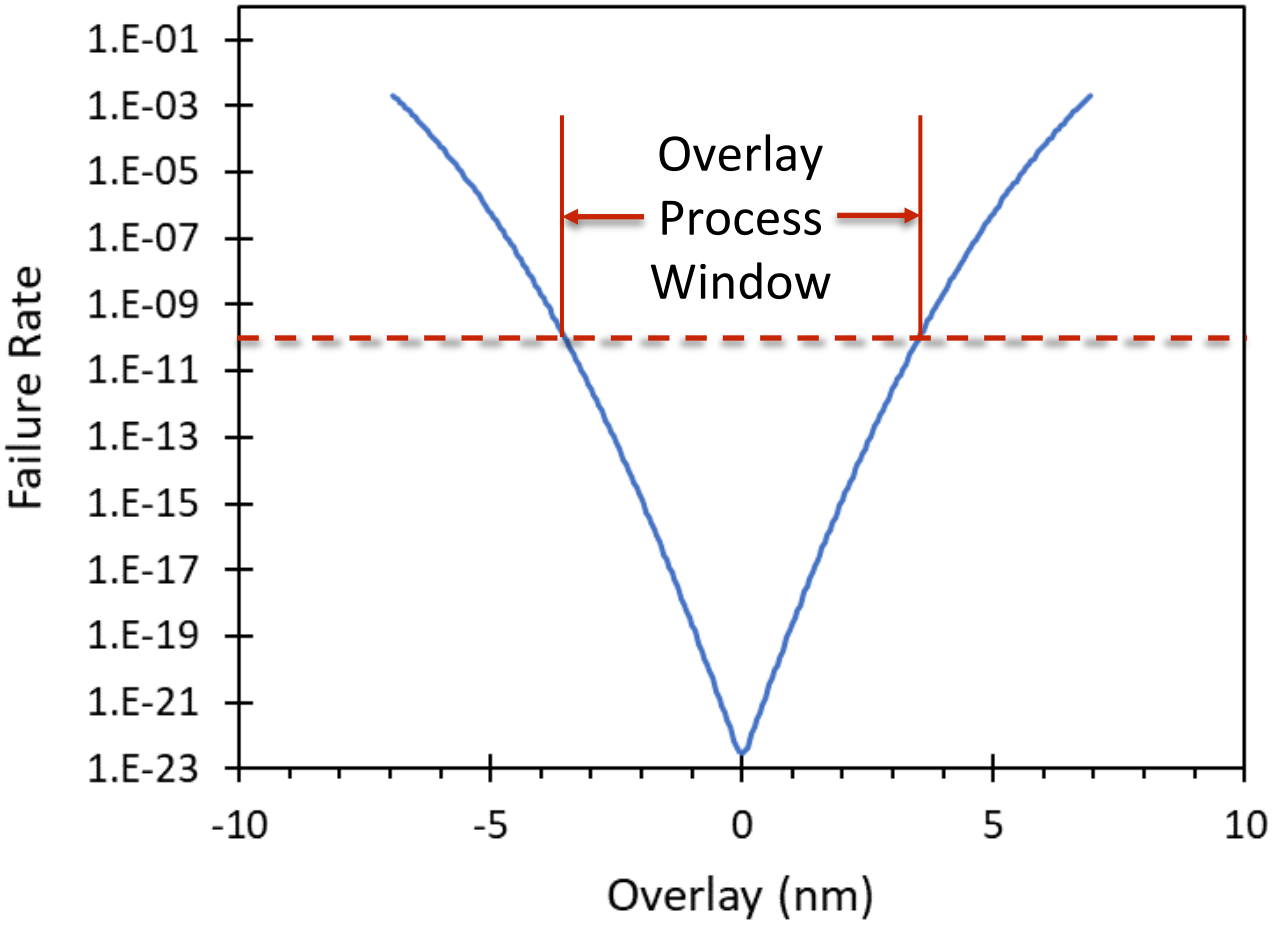
$$\sigma^2_{OVL} = \sigma^2_{Res} + \sigma^2_{LPPE_{via}} + \sigma^2_{LPPE_{line}}$$

4. Define the failure probability (assume Gaussian distribution)

$$\text{Probability}(CD_3 < 0) \approx \frac{\sigma}{\sqrt{2\pi}\mu} e^{-\frac{\mu^2}{2\sigma^2}}$$



The Overlay Process Window



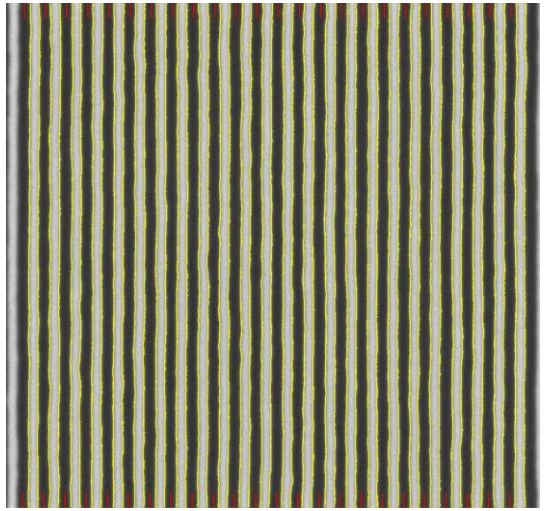
- "Failure rate" = fraction of instances where either $CD_3 \; or \; CD_4 \leq 0$
- Assign a maximum allowed excursion rate (e.g., 0.1 ppb)
- The Overlay Process Window is the range of overlay that keeps the excursion rate below this threshold

Metrology with MetroLER

EUV + SADP

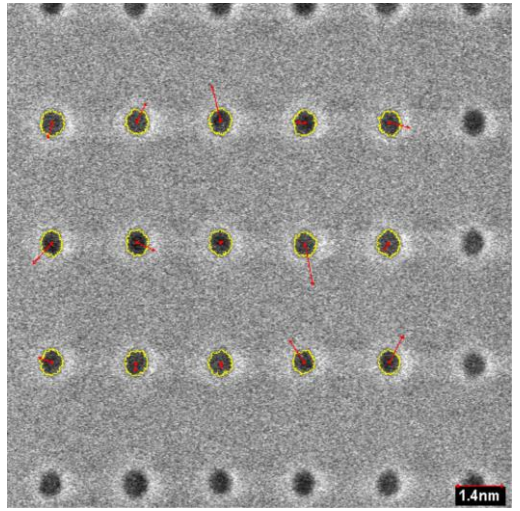
1024x1024
Pixel size = 0.329 nm
Voltage = 1600 V
Frames = 64
64 images across the wafer

DSA + SADP



1024x1024
Pixel size = 0.527 nm
Voltage = 1600 V
Frames = 64
64 images across the wafer

EUV Single Patterning

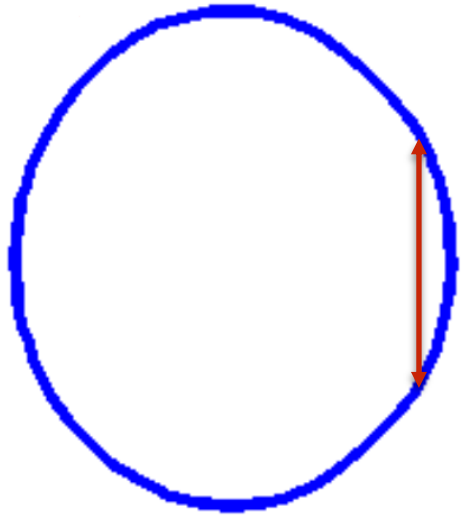


512x512
Pixel size = 0.754 nm
Voltage = 800 V
Frames = 12
320 images across the wafer and across the field

(Note: no across-field variations were measured for line/space patterns)

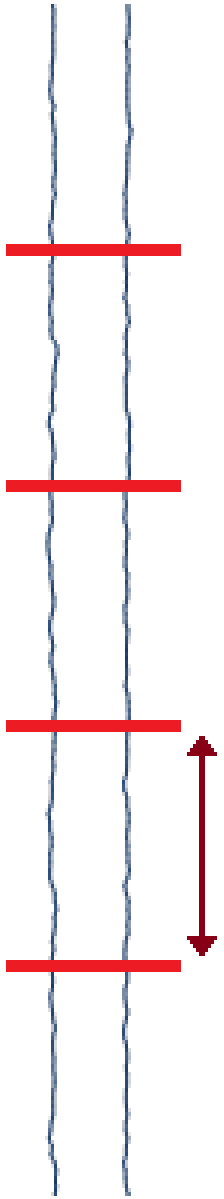
Choosing Segment Length

- The statistical variations of the lines and spaces are measured over the appropriate segment length
  - Here, we care about the overlap of the via with the neighboring space



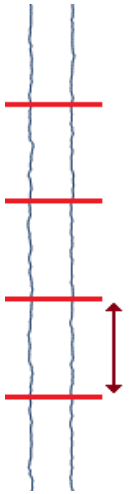
Measured Mean Contour

- Due to designed sidewall taper, the via height at the bottom ≈ 16 nm
- We will choose half this amount as the segment length (8 nm)



Metrology Results: Pitch = 21 nm

Parameter	Mean (nm)	GCDU (nm)	LCDU (nm)	LPPE (nm)	LEPE (nm)
EUV Space Segment CD	11.7	0.33 ± 0.06	2.09 ± 0.02	1.161 ± 0.008	1.58 ± 0.01
DSA Space Segment CD	11.6	0.67 ± 0.12	1.157 ± 0.007	1.071 ± 0.005	1.272 ± 0.006
Via X CD	13	2.1 ± 0.15	2.03 ± 0.04	1.46 ± 0.03	1.76 ± 0.02

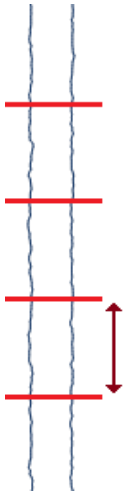


Segment Length = Via Y CD/2 = 8 nm

- Vias land on the measured space features
- Line population is spacer defined (ALD Process), and the space population is EUV/DSA defined
- Uncertainty estimates are ± 2*Standard Error
- For LEPE, the worst of right/left edge is used
- GCDU, LCDU, LPPE, and LEPE are 3σ

Metrology Results: Pitch = 18 nm

Parameter	Mean (nm)	GCDU (nm)	LCDU (nm)	LPPE (nm)	LEPE (nm)
EUV Space Segment CD	9.5	0.38 ± 0.06	2.89 ± 0.02	1.260 ± 0.009	1.91 ± 0.013
DSA Space Segment CD	10.4	0.55 ± 0.05	1.43 ± 0.01	0.911 ± 0.006	1.207 ± 0.008
Via X CD	12	2.1 ± 0.15	2.03 ± 0.04	1.46 ± 0.03	1.76 ± 0.02



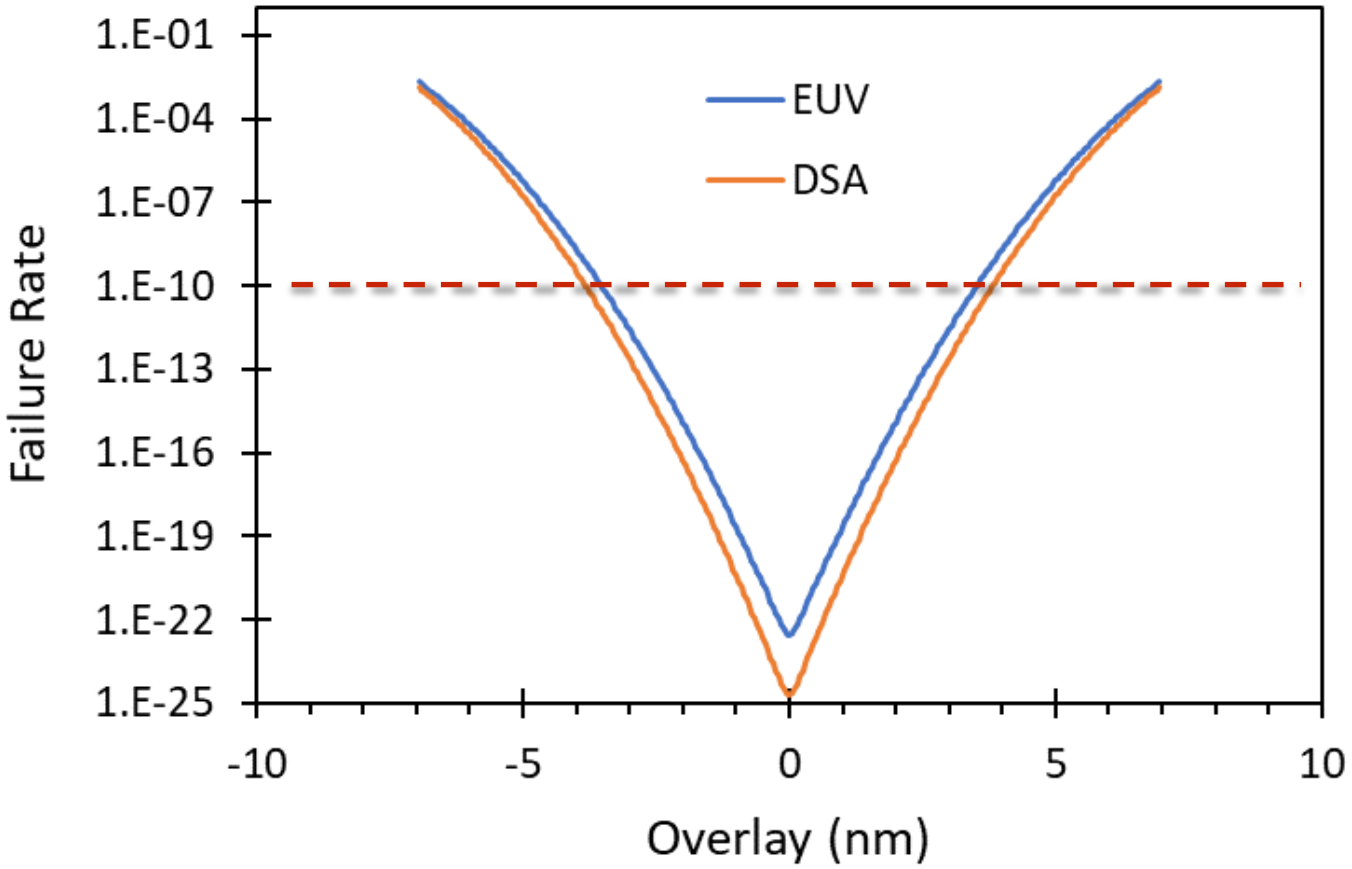
Segment Length = Via Y CD/2 = 8 nm

- Vias land on the measured space features
- Line population is spacer defined (ALD Process), and the space population is EUV/DSA defined
- For subsequent modeling, a space CD = 10 nm is used for both EUV and DSA
- Uncertainty estimates are ± 2*Standard Error
- For LEPE, the worst of right/left edge is used
- GCDU, LCDU, LPPE, and LEPE are 3σ

Bridging was a Problem with EUV Pitch = 18 nm

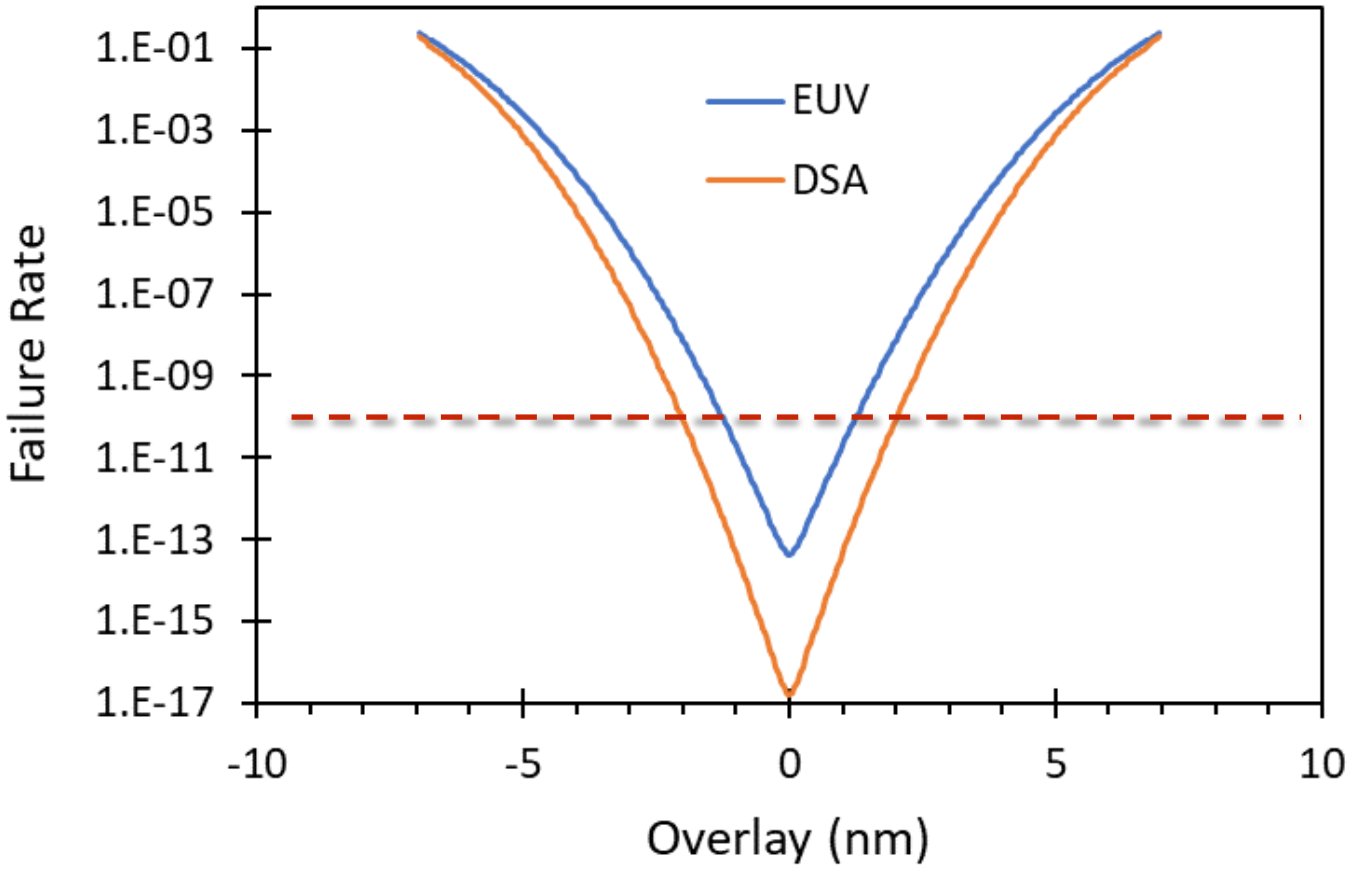
- 3 out of 64 images exhibited bridging for EUV flow
  - Regularly observed for this flow at this pitch
- DSA rectification flow did not show any bridging

The Overlay Process Window: Pitch = 21 nm



- For a 0.1 ppb failure rate threshold, the Overlay Process Window (OPW) is
  - EUV = 6.9 nm
  - DSA = 7.5 nm

The Overlay Process Window: Pitch = 18 nm



- For a 0.1 ppb failure rate threshold, the Overlay Process Window (OPW) is
  - EUV = 2.5 nm
  - DSA = 4.0 nm

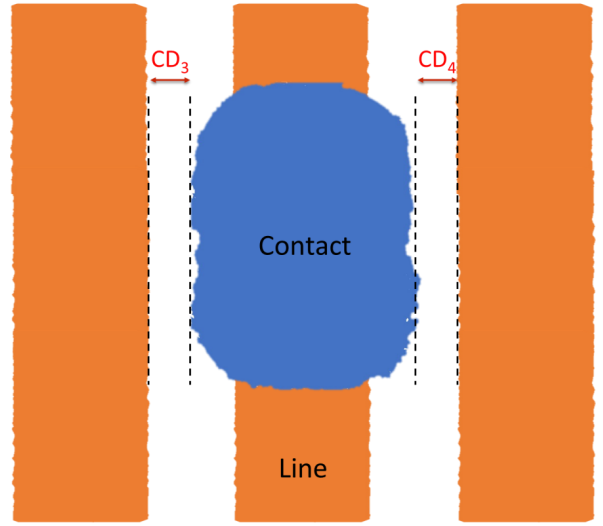
Propagation of Uncertainty to the OPW

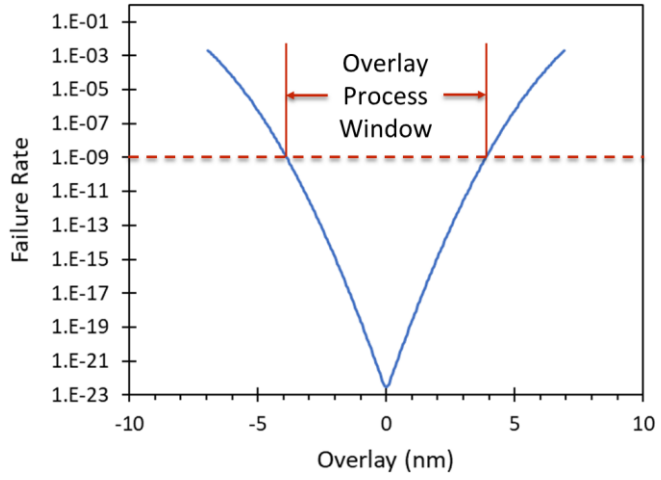
- All individual terms propagate to an uncertainty in σ_{CD_3} and σ_{CD_4} : SE(σ_{CD_3}) ≈ 0.008 nm
- Uncertainty in σ_{CD_3} and σ_{CD_4} propagates to uncertainty in the Overlay Process Window based on the slope of the OPW at the failure threshold

$$\Delta\mathrm{OPW} = 2 * \left(\mu_{CD_3}/\sigma_{CD_3}\right) * \mathrm{SE}\left(\sigma_{CD_3}\right)$$

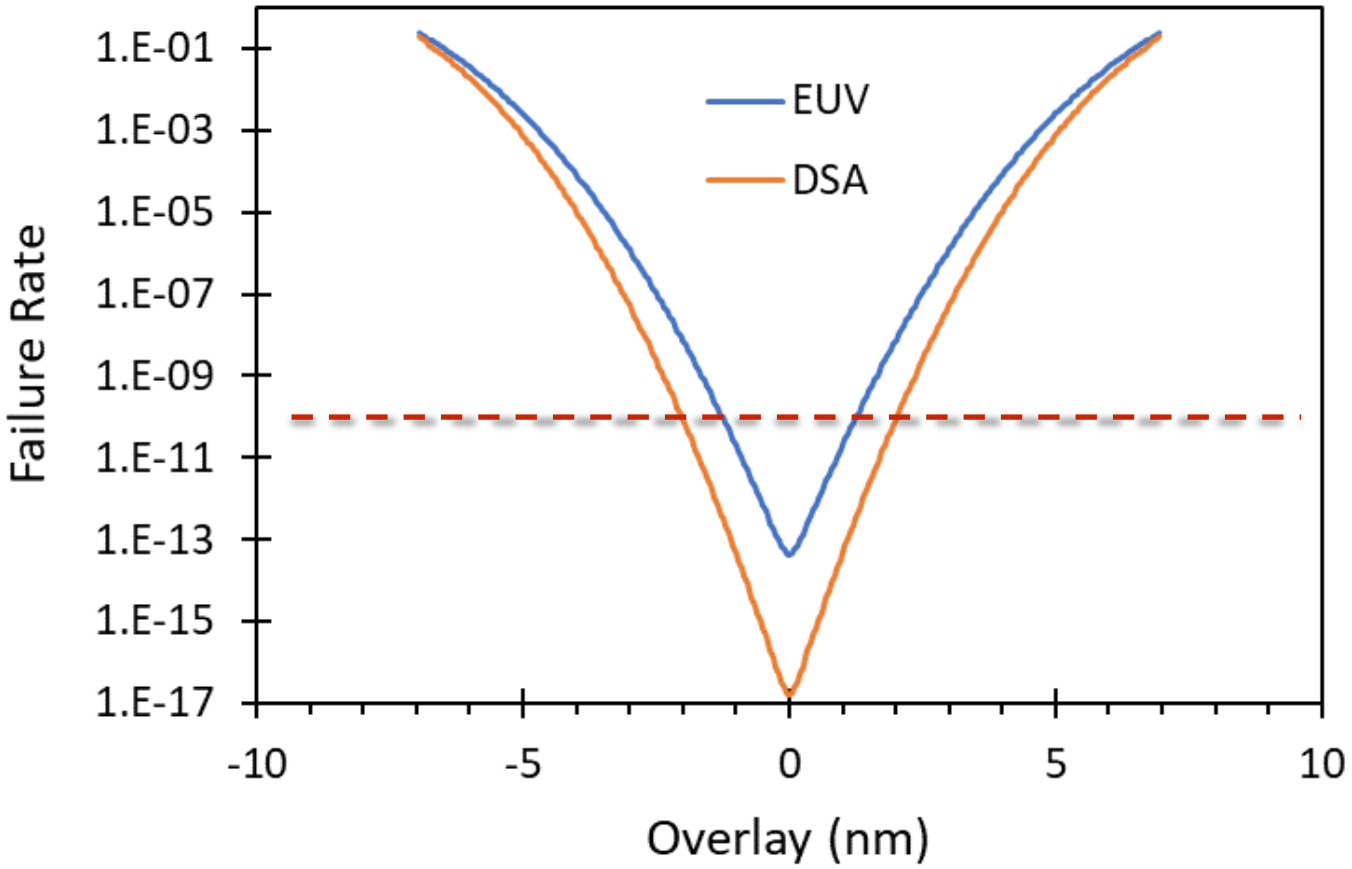
For a failure rate threshold of 1 ppb, $2 * \left(\mu_{CD_3}/\sigma_{CD_3}\right)$ = 12

For a failure rate threshold of 0.1 ppb, $2 * \left(\mu_{CD_3}/\sigma_{CD_3}\right)$ = 12.7





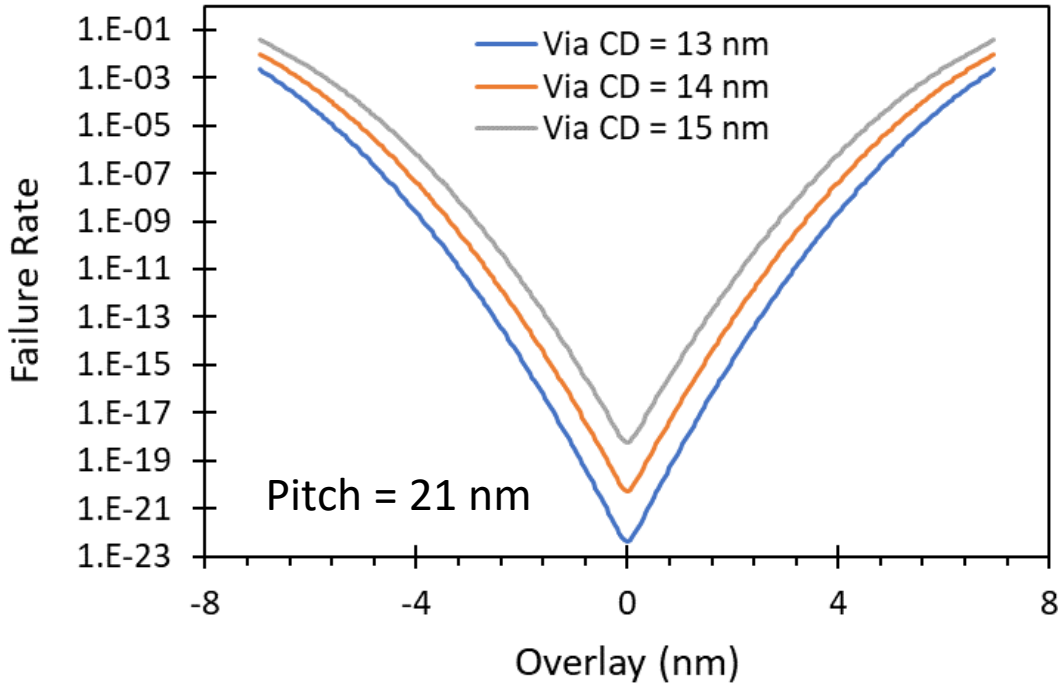
The Overlay Process Window



- The Overlay Process Window (OPW) for 21 nm pitch is
  - EUV = 6.9 ± 0.2 nm
  - DSA = 7.5 ± 0.2 nm
- For 18 nm pitch:
  - EUV = 2.5 ± 0.2 nm
  - DSA = 4.0 ± 0.2 nm

Parametric Study – The Role of Via Size

- A smaller via size increases the likelihood of poor line contact
  - Not investigated here
- A larger via size increases the likelihood of touching the neighboring line



1 nm increase in Via CD
results in a 1 nm reduction in the
Overlay Process Window (OPW)

(assumes stochastic variability the same for all via sizes)

Conclusions

- Stochastic failure rate analysis using EPE metrology data enables quantitative estimation of the overlay process window for different processes
- There is a small but statistically significant failure rate benefit to using DSA flow for the SADP backbone for making 21 nm pitch patterns
- There is a large failure rate benefit to using DSA rectification flow for the SADP backbone for making 18 nm pitch patterns
  - Final patterns exhibit lower segment LEPE when made with DSA rectification
- Suggestions for metrology improvements
  - Add across-field measurements for lines/spaces
  - Increase via image size to 1024x1024 (same pixel size) to increase number of vias per image and increase accuracy of LPPE and LEPE measurements
- Next Step: add low contact area failure mechanism

Acknowledgements

- Mike Adel, Intellectual Landscapes

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Thank You

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