Enablence

Advances in machine learning-based design for high-volume manufacturing of planar lightwave circuits

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Enablence Technologies Inc.

Photonics North
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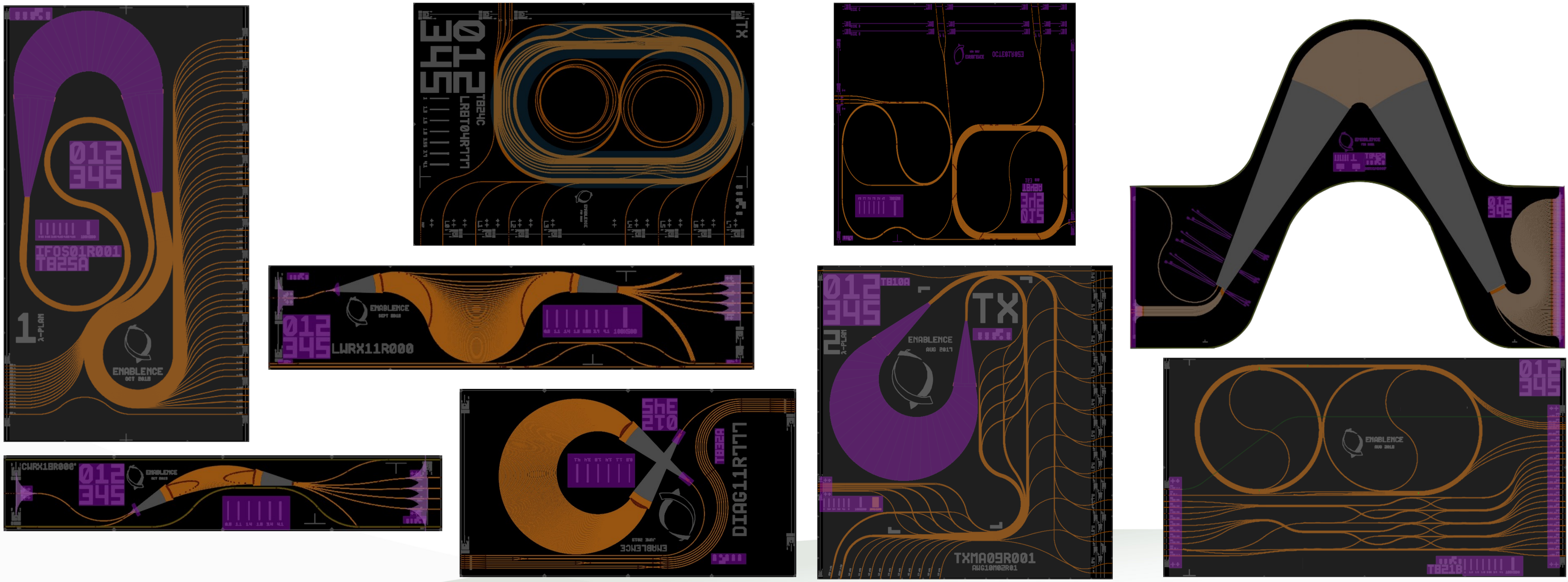
Introduction

PLC Technology

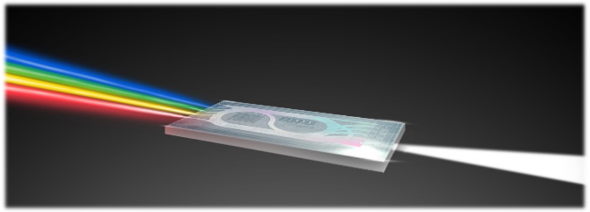
- Integrated photonics has emerged as a key technology to enable advancements in high-speed communication and advanced vision systems.
- Photonic integrated circuits possess high optical performance and are well suited for both monolithic and hybrid integration in a compact form factor, low cost and excellent reliability.

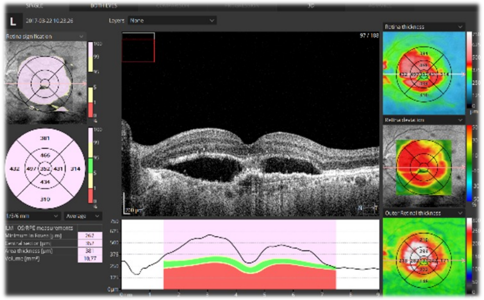


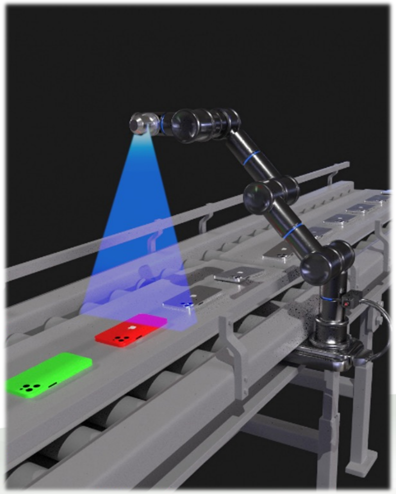
Introduction

Silica-on-silicon PLC platform

- A versatile and low-cost platform with powerful characteristics.
- Widespread applications, including high-speed communication, medical imaging, autonomous driving, and environmental sensing.







Our PLC Platform

Silica-on-silicon

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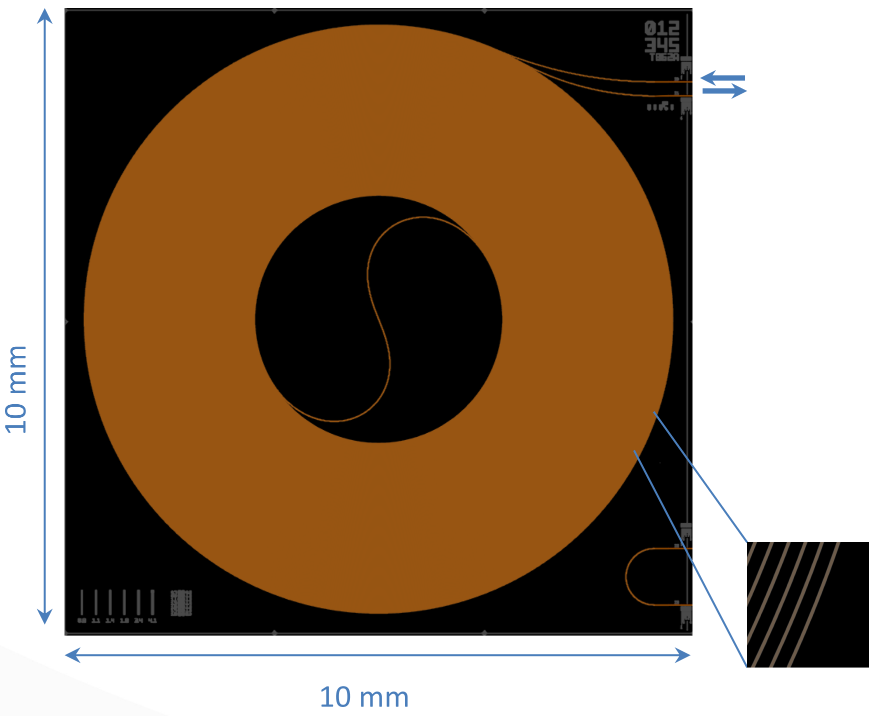
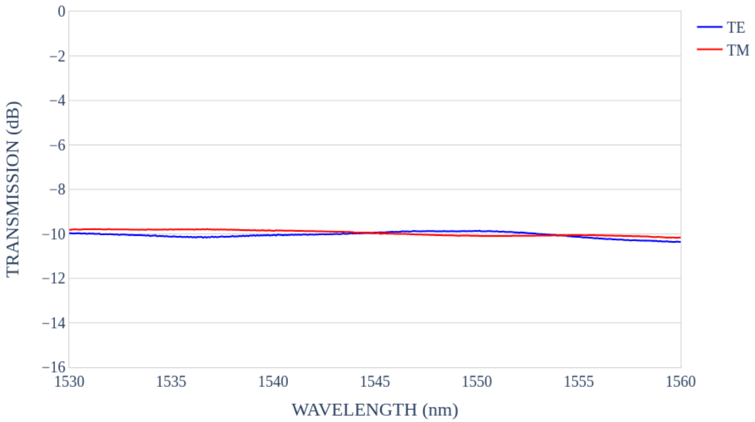
- Buried silica-based waveguides with a Δn = 2.0% refractive index contrast and typical waveguide dimensions of 3 × 3 µm.
- Fabricated using atmospheric pressure chemical-vapor deposition (APCVD) and reactive ion etching.
- We offer our fabrication services for external clients for rapid prototyping and cost-effective custom solutions.
- Typical performance characteristics:
  - Low waveguide propagation losses (< 1 dB/m)
  - Efficient fiber-to-waveguide coupling (~0.5 dB per facet)
  - Temperature-stable optical performance (< 10 pm/°C)
  - Polarization-invariant waveguides with zero birefringence

Ultra-dense architectures

Long delay lines

- An example of a 10-meter-long spiral with waveguide density close to the theoretical limit:

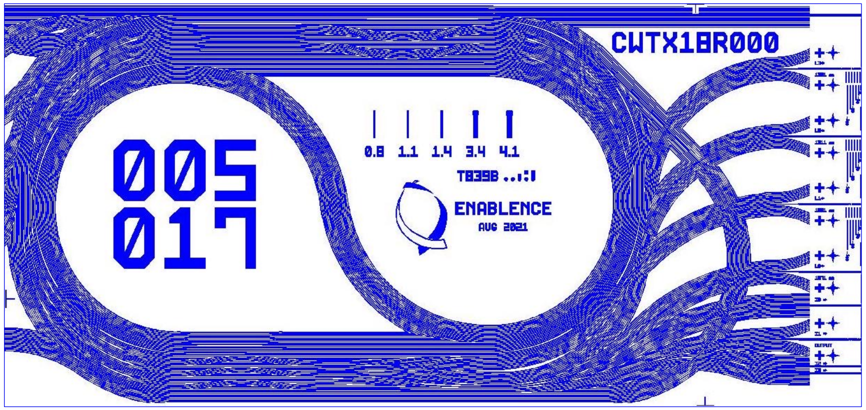


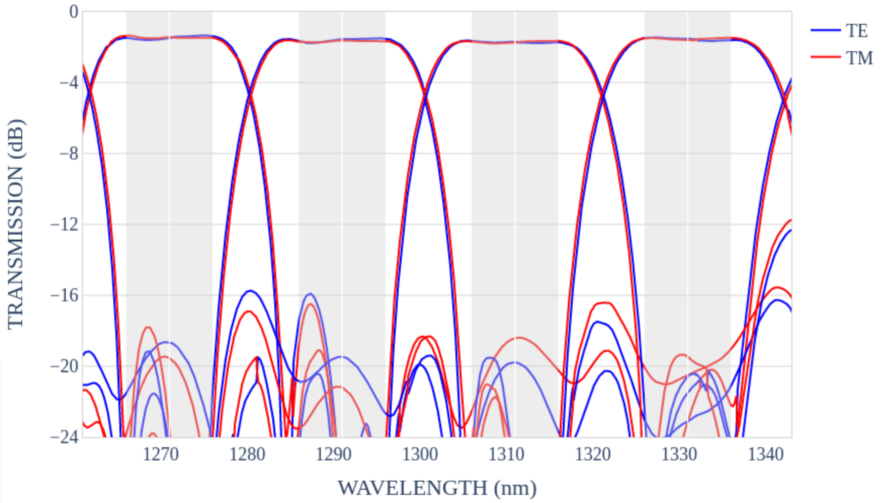


- Realized in silica-on-silicon with a refractive index contrast of Δn = 2.0%.
- Total device footprint: 1.0 cm^2
- Waveguide density close to the theoretical limit
- 1 dB/m propagation loss
- Polarization- and wavelength-independent operation across the C-band

Ultra-dense architectures

4-channel CWDM multiplexer

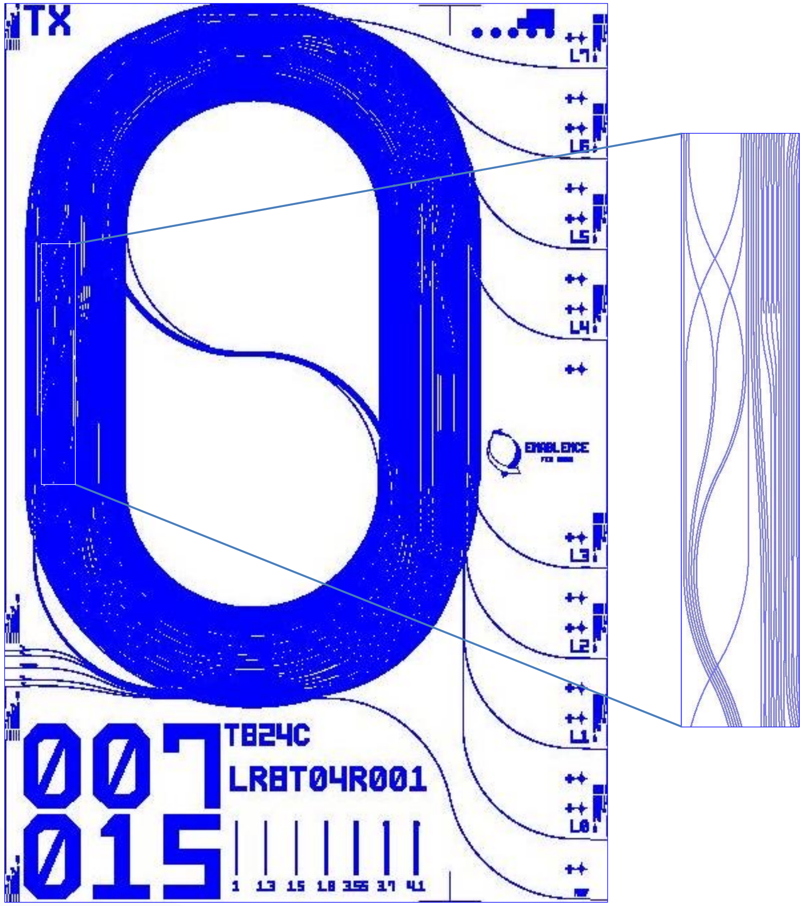




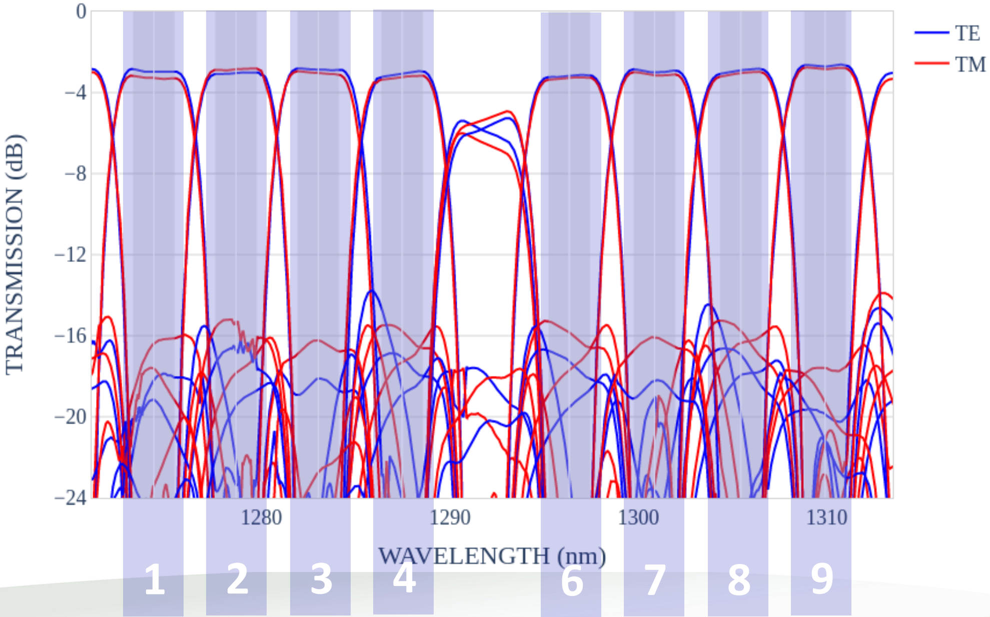
- Total device footprint: 0.18 cm^2
- Worst-channel insertion loss of 1.5 dB
- Without the two fiber couplings, on-chip loss estimated at 0.3 dB
- 1 dB bandwidth of 16.4 nm (>82% of the channel pitch)
- Worst case crosstalk of 19 dB
- Polarization-independent operation across the O-band (polarization dependent loss < 0.2 dB)

Ultra-dense architectures

8-channel LAN-WDM multiplexer



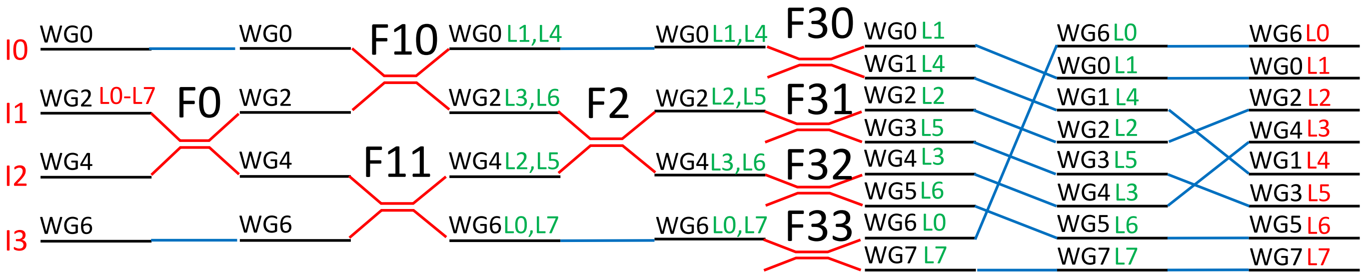
- Total device footprint: 0.38 cm^2
- On-chip loss estimated at 0.3 - 0.5 dB
- 1 dB bandwidth of 3.5 nm (80% of the channel pitch)
- Polarization-independent operation across the O-band (polarization dependent loss < 0.2 dB)



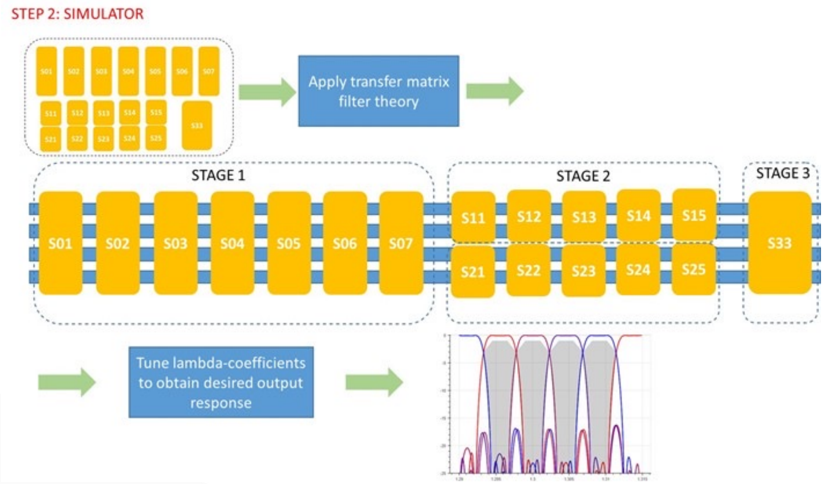
Machine-driven design

Progressive abstraction of complexity

STEP 1: Simplified functional view



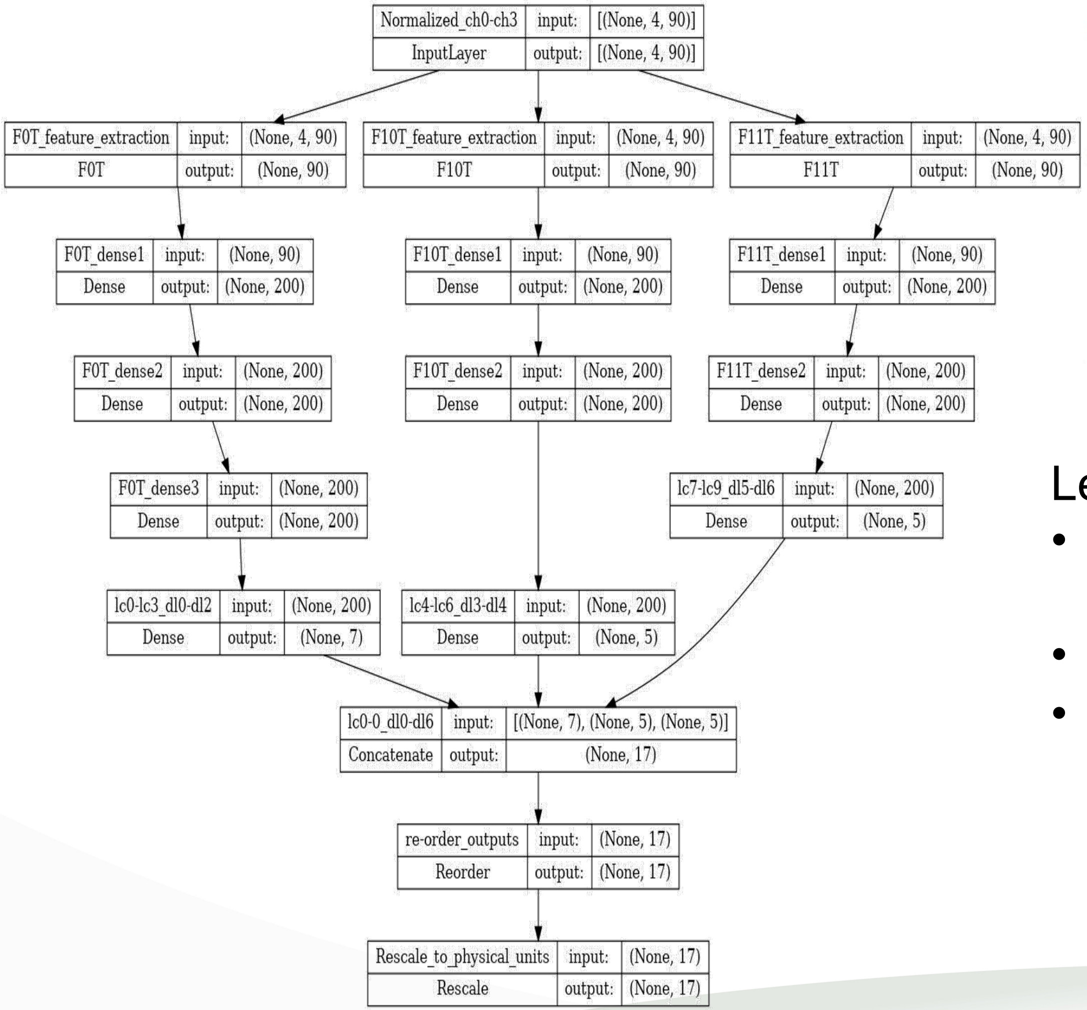
STEP 2: Expanded physical / simulation diagrams

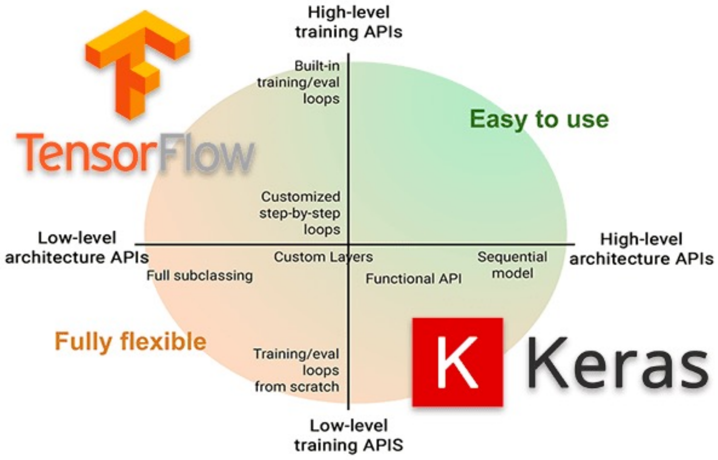


STEP 3: Automated transformer from diagrams to physical layout

ML-driven design

Building custom models





Leveraging ML technologies:

- Adopt Keras API for arbitrary advanced workflows
- Build on top of TensorFlow 2
- Deploy on AWS

Advanced vision

Optical processing

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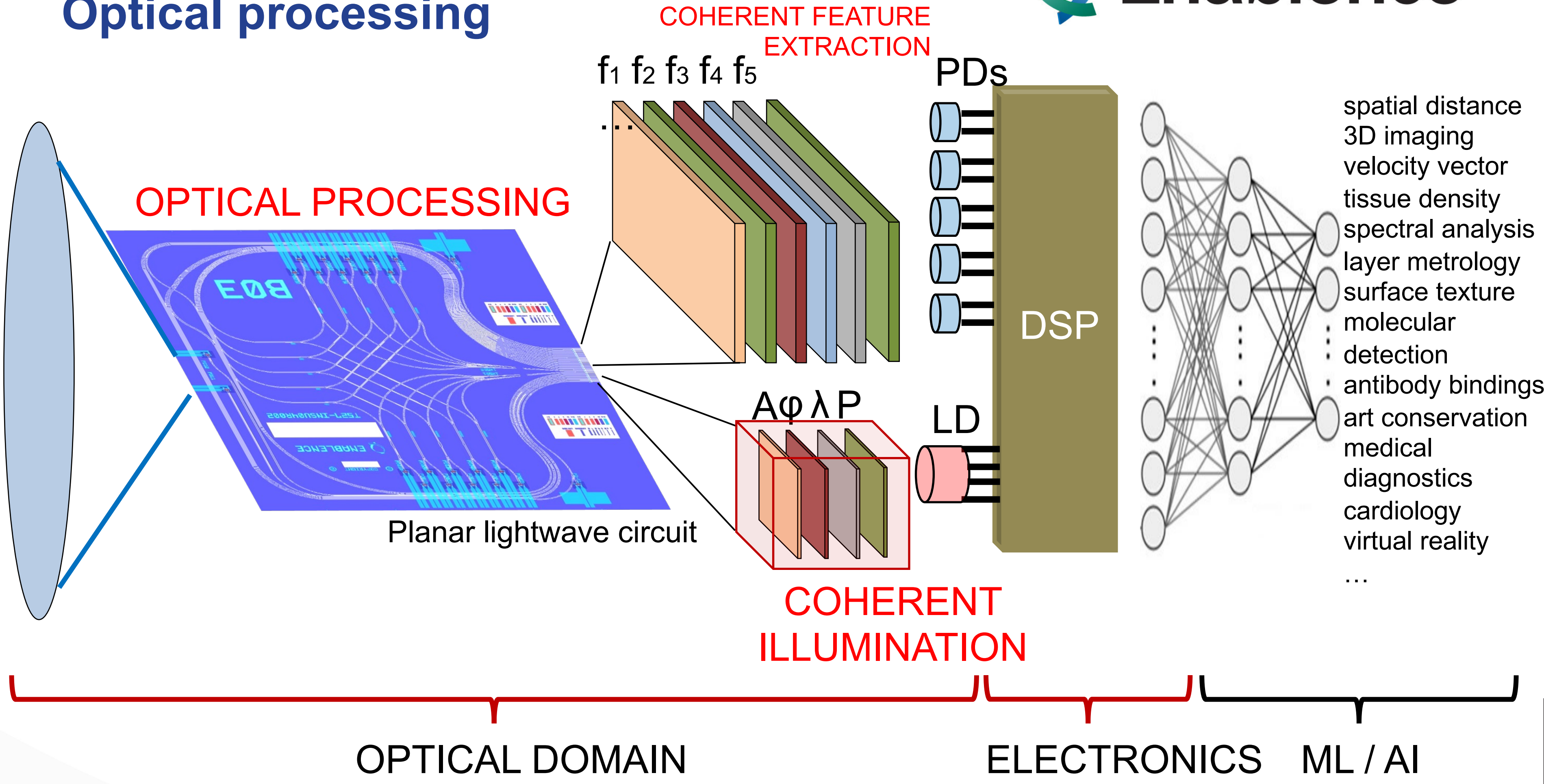


COHERENT FEATURE EXTRACTION

f_1 f_2 f_3 f_4 f_5 …

PDs

DSP

OPTICAL PROCESSING

Planar lightwave circuit

$A\varphi\ \lambda\ P$

LD

COHERENT ILLUMINATION

spatial distance
3D imaging
velocity vector
tissue density
spectral analysis
layer metrology
surface texture
molecular detection
antibody bindings
art conservation
medical diagnostics
cardiology
virtual reality
…

OPTICAL DOMAIN

ELECTRONICS

ML / AI

Advanced vision systems use coherent illumination and perform optical processing BEFORE the signal is detected electrically. Rich palette of optical features feed deep ML/AI models to enable a wide range of advanced vision applications

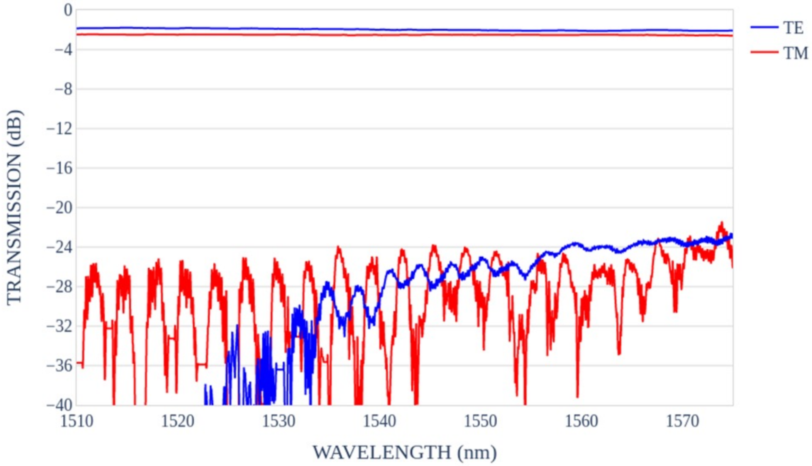
Optical building blocks

Polarization beam splitters

composite coupler

birefringent region

composite coupler



- Polarization isolation > 22 dB over 1510 – 1575 nm measurement range
- Highly-integrated arrayed PBS solution for LiDAR applications

Optical building blocks

k-clocks for OCT and LiDAR

- Swept-source OCT (SS-OCT) and FMCW LiDAR measure the signal in k-space, which is linear to the change in the optical frequency of the swept source.
- k-clock is a timing control signal that is produced by an auxiliary MZI that is used as a highly linear optical frequency fiducial marker.
- Extremely low propagation losses of the PLC platform allow for the realization of wide range of k-clocks:

10 GHz (OCT)

10 MHz (LiDAR)

PLCs in Production

Challenges in high volumes

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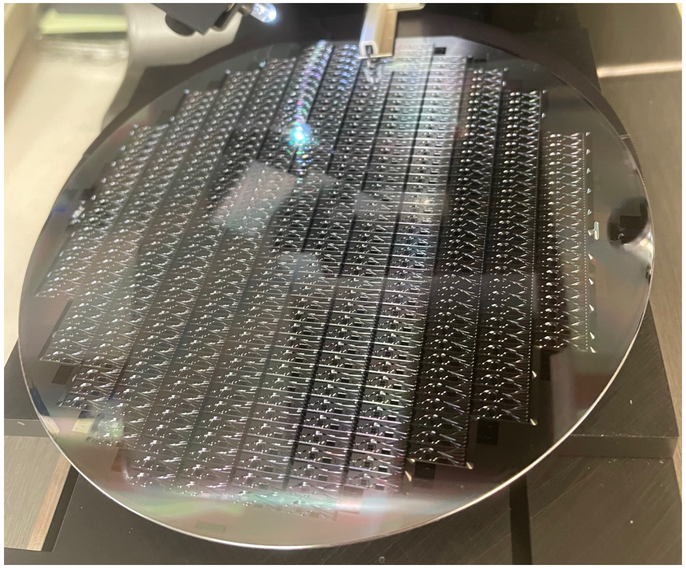
- To achieve high-performing devices, we rely on advanced data analysis that is tightly coupled to our design and fabrication.

- We use machine learning (ML) algorithms to scale the capabilities of the silica-on-silicon PLC platform to high-volume manufacturing, where reproducible performance is critical to the adoption of integrated optics solutions.

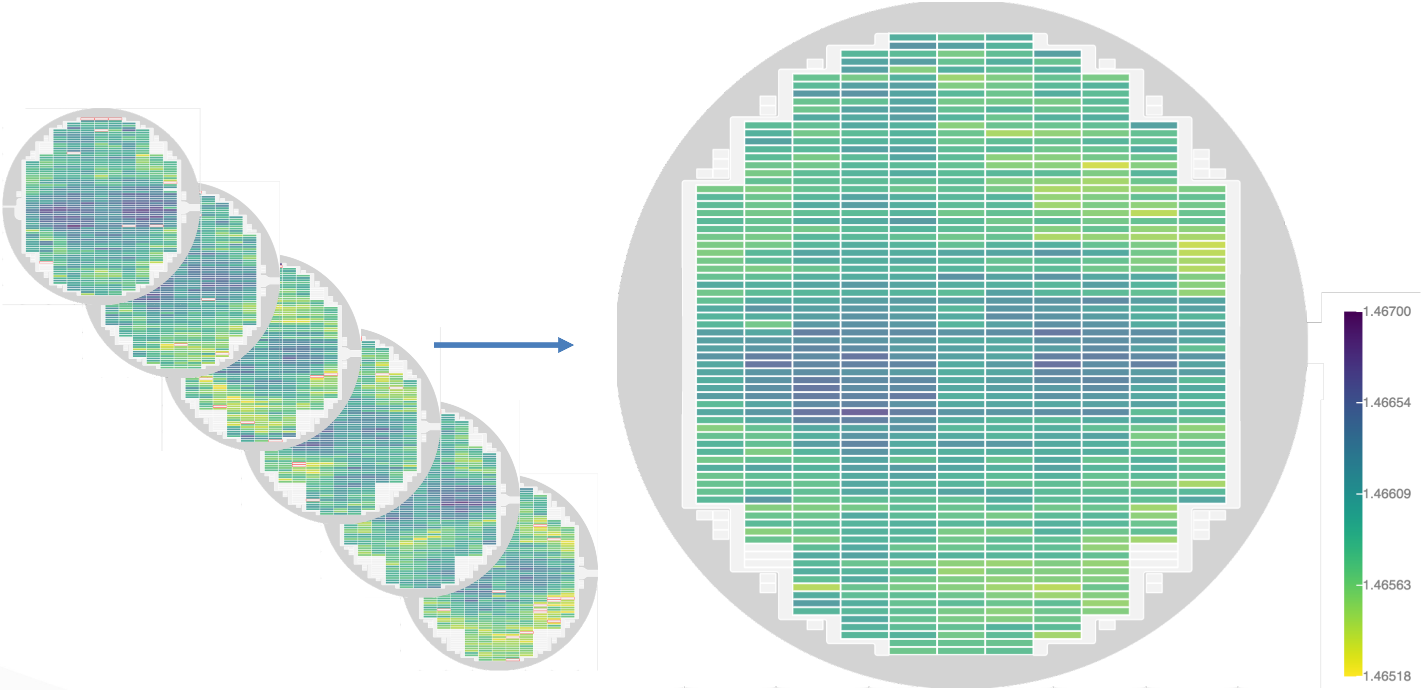
- Two challenges to achieving homogeneous performance:
  1. Systematic variability within a wafer
  2. Variations between fabricated wafers



Design optimizations

The challenge of process uniformity

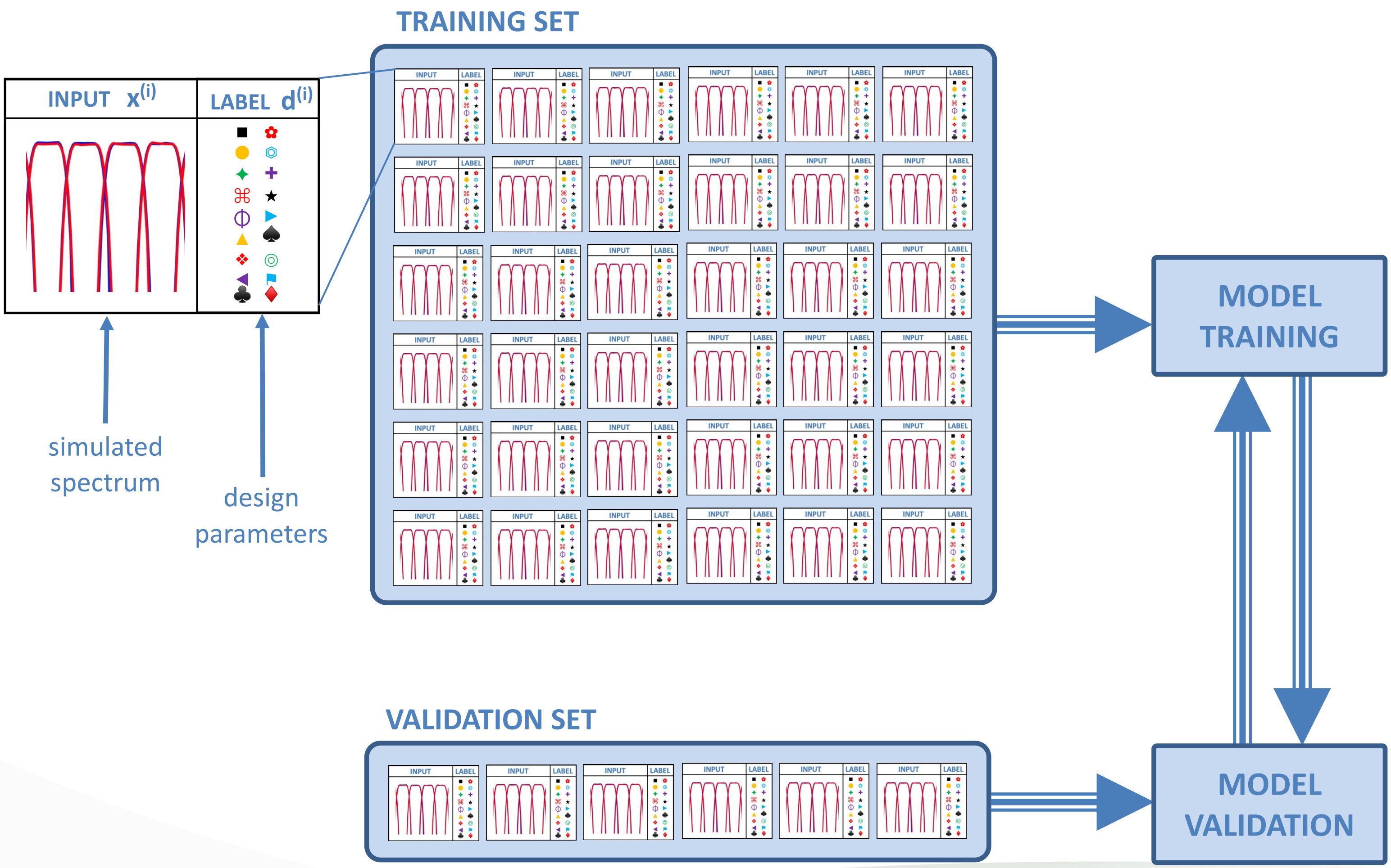
- Process uniformity and consistency is critical in the manufacturing of photonic chips.
- Traditionally, standard statistical methods are used to compensate for systematic process non-uniformities:



systematic index variation

Design Optimizations

Adjustments of design parameters through ML



TRAINING SET

INPUT $x^{(i)}$

LABEL $d^{(i)}$

simulated spectrum

design parameters

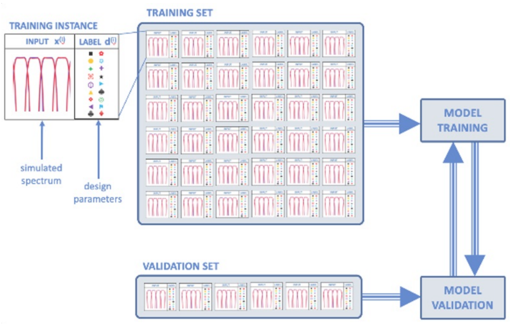
MODEL TRAINING

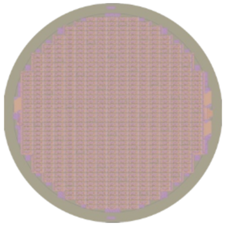
VALIDATION SET

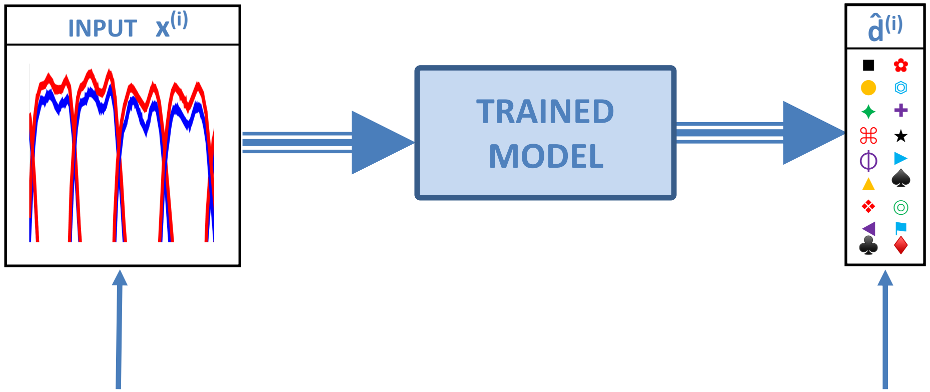
MODEL VALIDATION

Design Optimizations

Adjustments of design parameters through ML







INPUT $x^{(i)}$

TRAINED MODEL

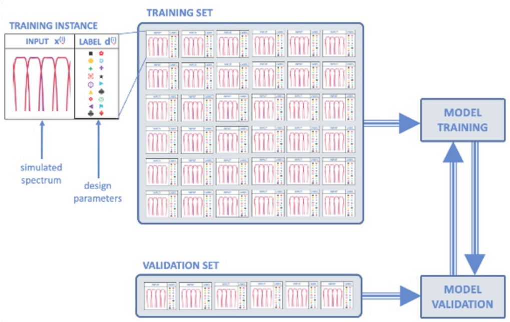
$\hat{d}^{(i)}$

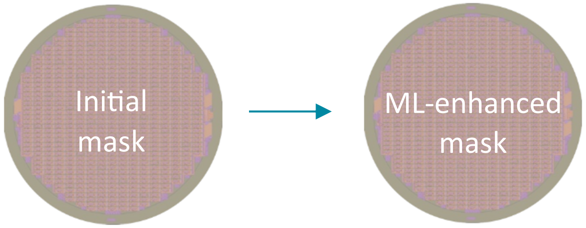
measured spectrum

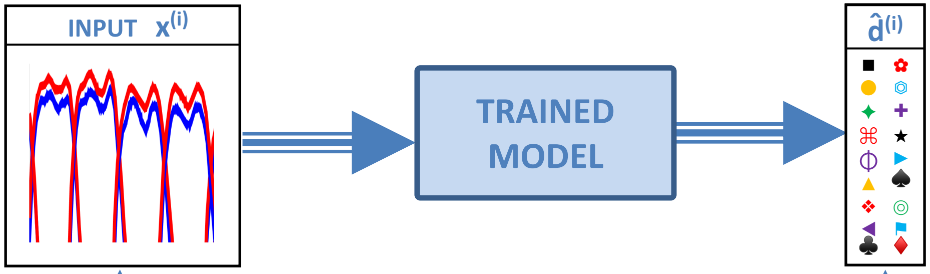
inferred design parameters

Design Optimizations

Adjustments of design parameters through ML




Initial mask → ML-enhanced mask


INPUT $x^{(i)}$

TRAINED MODEL

$\hat{d}^{(i)}$

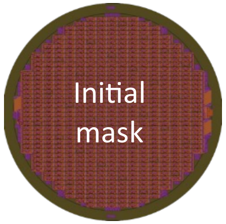
measured spectrum

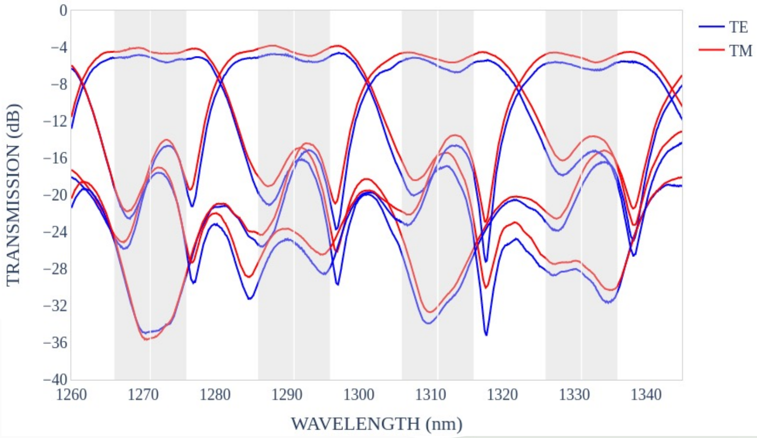
inferred design parameters

Design Optimizations

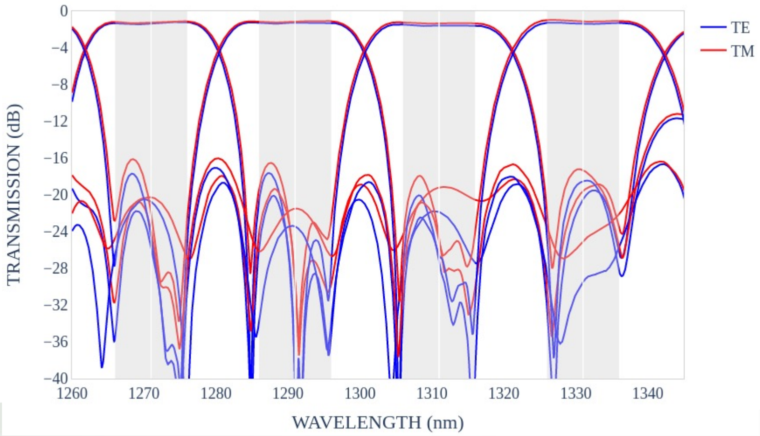
Adjustments of design parameters through ML

- To validate the approach, we applied it to a production mask with 600 devices:
  - Devices on the mask were designed to be identical, except for a refractive index distribution correction computed by traditional statistical means.
  - Despite the built-in compensation for systematic refractive index variations, nominally identical devices showed significant variations in performance stemming from process variabilities:





A poor-performing chip

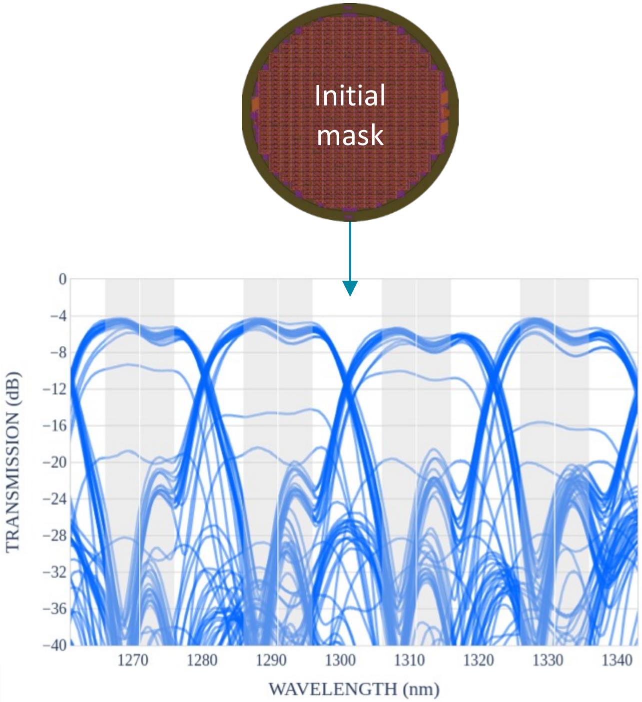


A high-performing chip from the same wafer

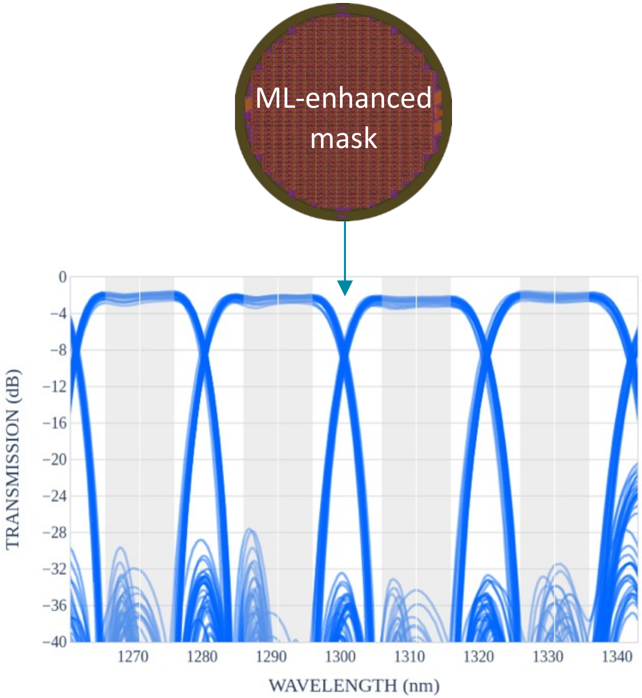
Design Optimizations

Adjustments of design parameters through ML

- To validate the approach, we applied it to a production mask with 600 devices:
  - We used the model predictions to insert corrections into each of the chips on the mask, thereby producing a ML-enhanced version of the production mask.



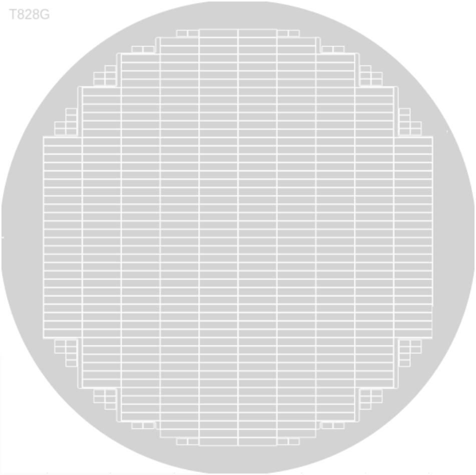
20 worst performing chips in the initial version of the mask.



The same 20 chips in the ML-enhanced version of the mask.

Performance Predictions

Classification based on a wafer probe measurement



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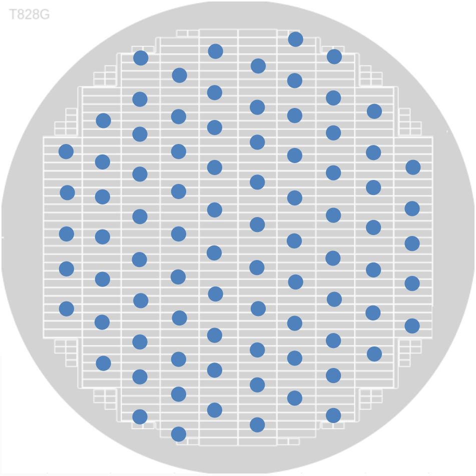
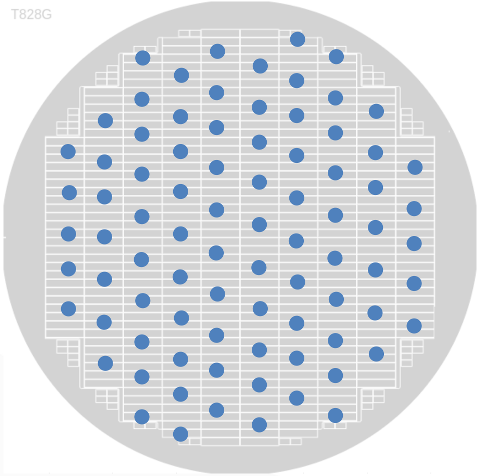


Probed locations
on the wafer

Performance Predictions

Classification based on a wafer probe measurement



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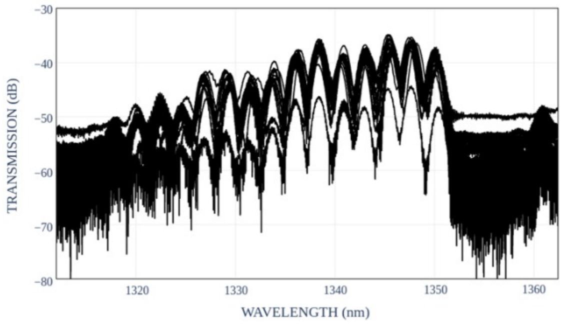
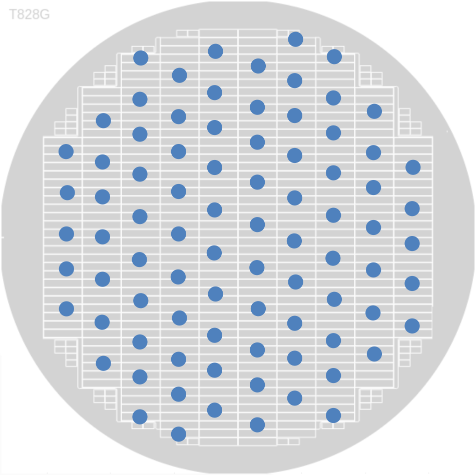


Typical spectroscopic
signature

Performance Predictions

Classification based on a wafer probe measurement



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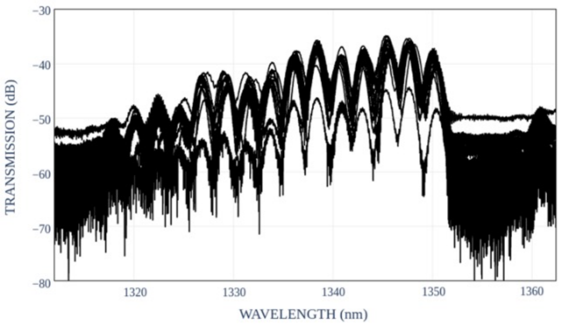

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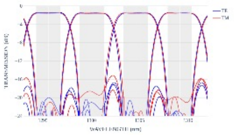
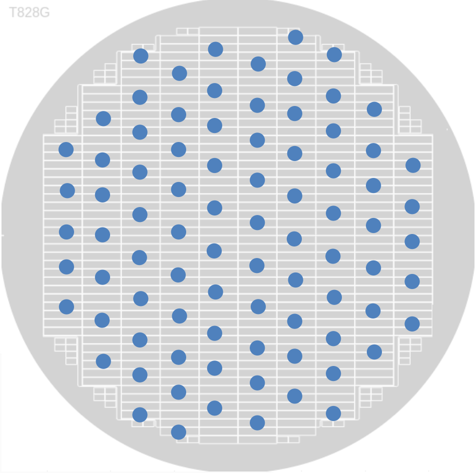


Predicted performance of
hundreds of chips on a wafer

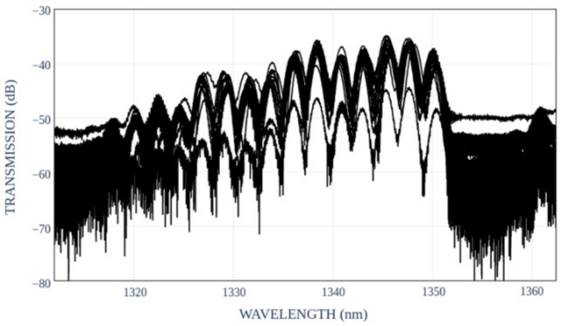
Performance Predictions

Classification based on a wafer probe measurement

Enablence



Probed locations on the wafer



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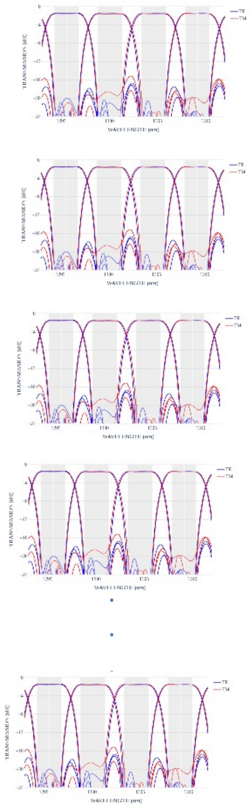

Predicted performance of hundreds of chips on a wafer

Specification parameters:

1. IL
2. IL uniformity
3. Grid detuning
4. Channel spacing uniformity
5. 0.5 dB passband
6. 1 dB passband
7. 3 dB passband
8. PDL
9. Ripple
10. Adjacent crosstalk
11. Non-adjacent crosstalk
12. Total crosstalk

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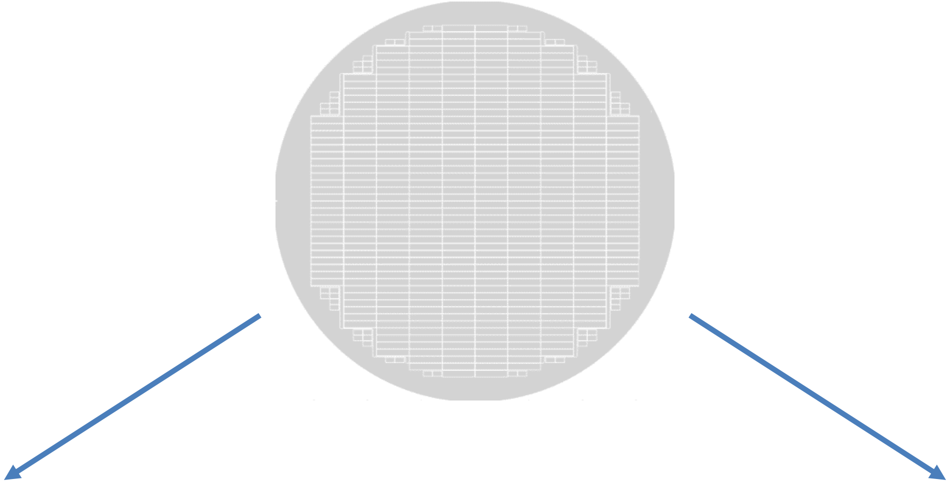
Performance Predictions

Classification based on a wafer probe measurement



Traditional chip testing

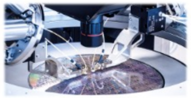
Time to measure a 4-channel chip	2 minutes
Cost of measuring a 4-channel chip (North America)	$4.25
Cost of measuring a 4-channel chip (Asia)	$0.55
Cost of characterizing a wafer with 600 chips	$2550 / $330
Time to measure a wafer with 600 chips	20 hours

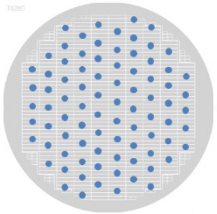
Wafer probe testing

Time to perform a wafer probe measurement	12 minutes
Time to infer the PASS/FAIL of all chips on a wafer	instantaneous
Effective measurement time per chip	1.2 seconds
Cost of characterizing a wafer with 600 chips	$25
Time to measure a wafer with 600 chips	12 minutes

Performance Predictions

Classification based on a wafer probe measurement





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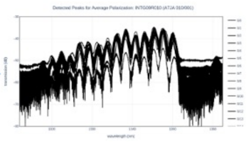

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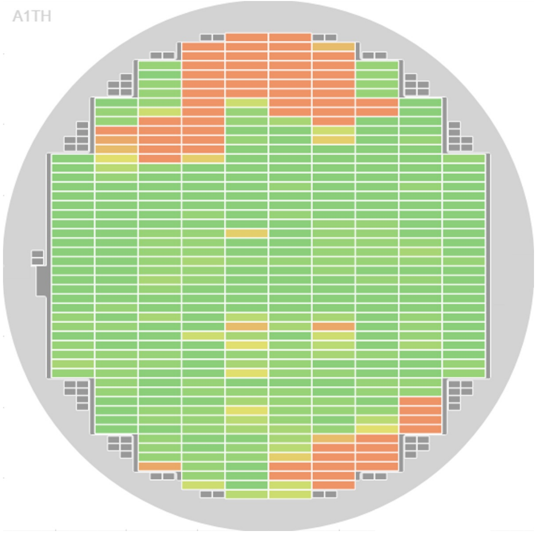
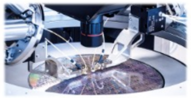
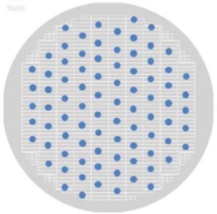


Predicted PASS/FAIL
over 26 specification
parameters

Performance Predictions

Classification based on a wafer probe measurement





Probed locations
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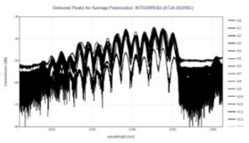

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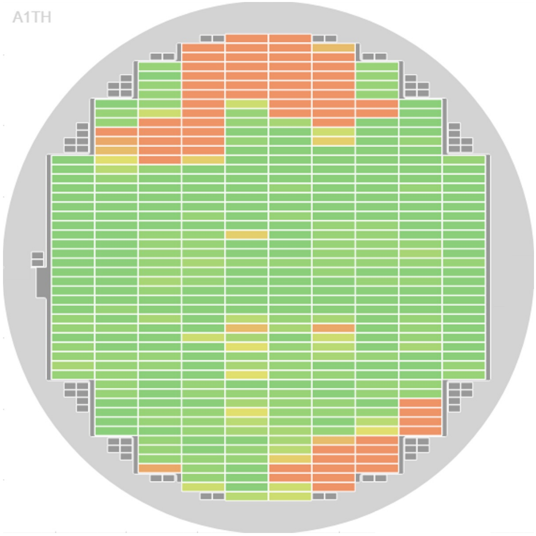

Predicted PASS/FAIL
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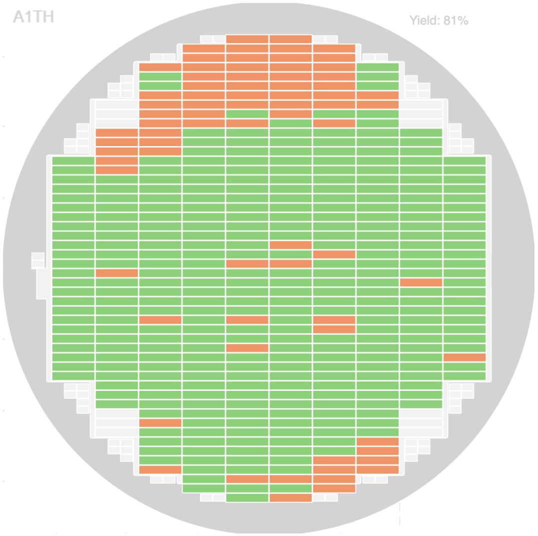
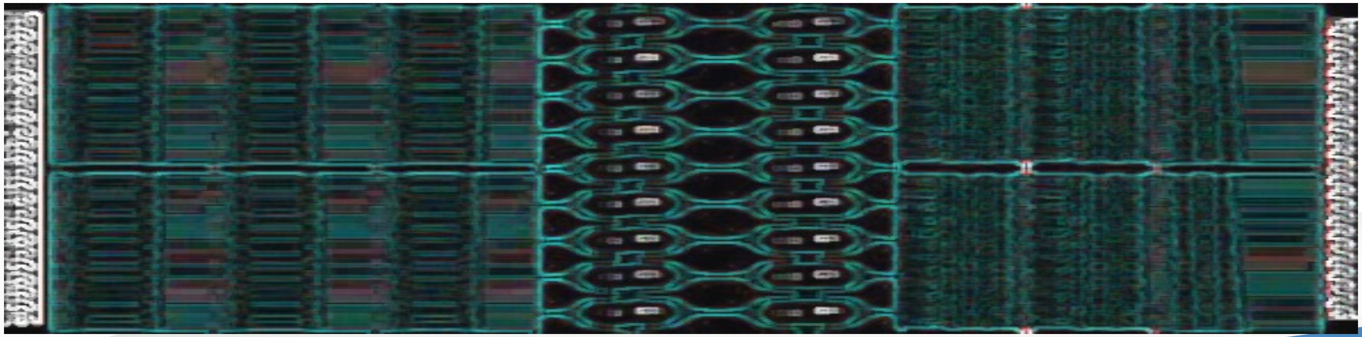


Actual PASS/FAIL
over 26 specification
parameters

Conclusions

- We described how AI/ML revolutionized the way photonic integrated circuits are designed and fabricated in a high-volume environment:
    - The automated layout transformers overcome the complexity of design and physical layer layout enabling novel architectures not only in communications but also advanced vision applications, such as LiDAR and OTC.
    - Deep neural network multivariate regression models optimize the individual design parameters of hundreds of devices on a mask.
    - A support vector machine (SVM) predicts the performance of optical chips in multi-dimensional space.
- These approaches bring the power of ML to both the design of optical chips and their manufacturing, demonstrating the tremendous potential of AI/ML for increasing the scale and reach of the photonics industry.

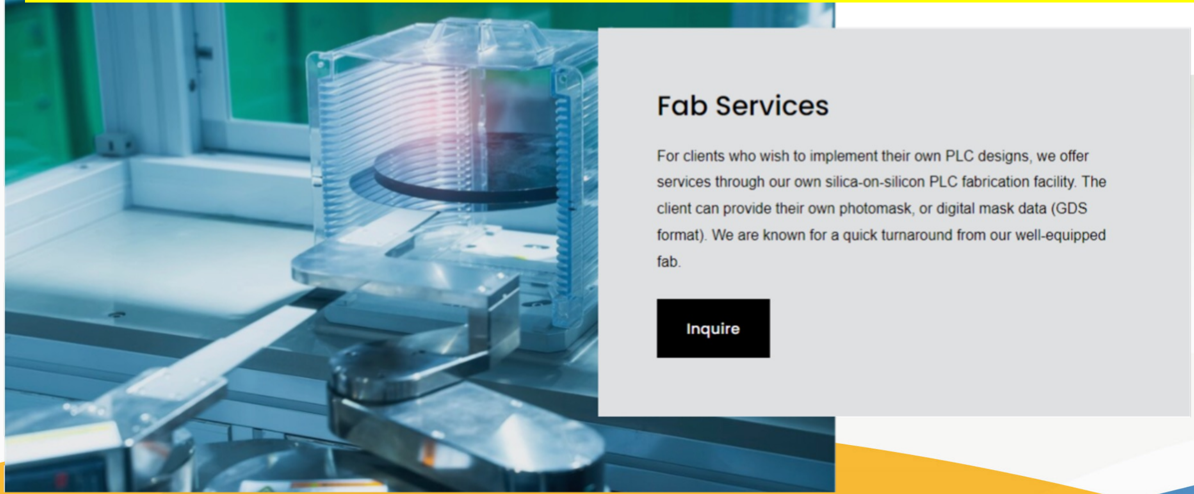


Enablence

Custom Optical Design

We have built systems-on-a-chip for avionics, medical robotics, automotive LIDAR, 3D mapping, and optical sensing. We can do commercial-grade prototyping or high-volume production of chips. Our mechanical design engineers can also assist with fiber pigtailing and packaging. Through PLC, we can help our customers to open new market opportunities.

Tutorial 2 – Ksenia Yadav
Machine Learning Fundamentals with Applications in Photonics, Wed, June 14, 11:05 – 12:05, ROOM 513



Fab Services

For clients who wish to implement their own PLC designs, we offer services through our own silica-on-silicon PLC fabrication facility. The client can provide their own photomask, or digital mask data (GDS format). We are known for a quick turnaround from our well-equipped fab.

USA

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