IEDM 65th International Electron Devices Meeting

2019 IEDM Conference Proceedings

Innovative Devices for an Era of Connected Intelligence

IEEE Electron Devices Society

For More Information
IEDM Online: ieee-iedm.org

Social Networks:
ieee-iedm.org/social-media

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Intro

IEEE International Electron Devices Meeting (IEDM) is the world's preeminent forum for reporting technological breakthroughs in the areas of semiconductor and electronic device technology, design, manufacturing, physics, and modeling. IEDM is the flagship conference for nanometer-scale CMOS transistor technology, advanced memory, displays, sensors, MEMS devices, novel quantum and nano-scale devices and phenomenology, optoelectronics, devices for power and energy harvesting, high-speed devices, as well as process technology and device modeling and simulation.

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- Wikipedia: https://en.wikipedia.org/wiki/International_Electron_Devices_Meeting

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Topics of Interest

ADVANCED LOGIC TECHNOLOGY (ALT)

Papers are solicited in the areas of CMOS platform technology, logic circuit design challenges, advanced node process integration schemes, process module advancements and process control techniques, and device technology co-optimization solutions. Platform technologies include the state-of-art Si technologies, beyond Si channel such as SiGe/Ge, and advanced device technologies such as Gate-All-Around nanowire and stacked nanosheet are of strong interest. Topics include device and circuit performance and scaling approaches, power-performance-area analysis, and architectural implications of interconnect technology and performance. Papers addressing process integration of heterogeneous channel materials, substrate and isolation technologies, shallow junctions, novel dielectrics and metal electrodes for gate stacks, contact and via processes, interconnect bottleneck, sequential monolithic 3D, heterogeneous chiplets, advanced packaging, and BEOL compatible transistors are solicited. Process module advancements in EUV lithography, deposition, planarization, etch and self-assembly techniques; and process control topics include defect detection as well as novel techniques for variability reduction are of interest. Submission of papers discussing interactions between advanced device technology and circuit design issues such as variability, aging, power constraints, physical layout effects, yield implication and DTCO solutions is highly encouraged.

EMERGING DEVICE and COMPUTE TECHNOLOGY (EDT)

Papers are solicited on novel devices and concepts that enhance existing or novel computing models. This includes devices based on novel transport mechanisms such as tunnel FET, negative capacitance FET, topological insulators, phase transitions, and Qubit devices. Devices based on low-dimensional systems including 2D materials, nanowires, and quantum dots are welcomed. Neuromorphic and approximate computing devices as well as non-charge-based logic such as magnetic logic, spintronics, and plasmonics are key topics. Submission on Cryo-CMOS for quantum computing enablement and high-performance computing is solicited. Furthermore, emerging state machines, continuous time dynamical systems, and lifelong learning machines are also of interest. Papers in EDT focus primarily on device physics, innovative transistor structures, and novel computing concepts; more mature "platform candidate" papers should be submitted to ALT. Reliability assessment of novel devices are also solicited here, while that for more mature technologies/devices should be submitted to RSD.

MEMORY TECHNOLOGY (MT)

Papers are solicited in all memory technology topics, including embedded and standalone memories, as well as computing-in-memory and neuromorphic computing applications. Topics span from novel concept cells to fully integrated memories, from prototyping to manufacturing issues and performance. Specific areas of interest include both conventional and novel memory cells including charge-based memories, ReRAM, MRAM, PCRAM, FeRAM, crosspoint and selectors, organic memory and NEMS-based devices, including their design and scaling, processing, reliability, and modeling. Novel concepts and demonstrations that enhance memory properties or apply to bio-inspired computing paradigms are of interest. Higher-level topics include 3D architectures and integration, novel read/program/erase schemes, solid state drive (SSD) applications, novel hierarchies and architectures for memory-centric systems, security, computing-in-memory and nonvolatile memory-enabled applications.

MICROWAVE, MILLIMETER WAVE and ANALOG TECHNOLOGY (MAT)

Papers are solicited in the areas of high frequency device technology, device physics and high frequency circuit applications in the micro, mm-wave and THz frequency spectrum. Device processes of interest include Si-based RF CMOS, such as FD-SOI and FinFET processes and SiGe HBTs. Compound semiconductors including InP/InGaAs/GaAs III-V HEMTs, FETs, DHBTs, mm-wave Schottkys and other microwave-enabling devices are also of key interest, as well as AlGaN/InGaN/GaN processes and devices optimized for RF performance. Other wide bandgap and organic RF-compatible devices and processes are also of interest. The area also includes passive devices implementing tunable passives, microwave and mm-wave switches and SAW/BAW filters. Basic RF-device modeling and reliability aspects are also covered. The circuit aspects covers analog front ends for 5G and beyond, mixers, transceivers, filters, beam formers, switches, LNAs, PAs, tunable passives, antenna arrays, as well as mixed signal implementations in the micro and mm-wave domain. Devices and circuits for RF energy harvesting are also a good fit.

MODELING and SIMULATION (MS)

Papers are solicited in the areas of analytical, numerical, and statistical approaches to model electronic, optical, and hybrid devices including sensors and interconnects. Topics include physical and compact models for semiconductor and novel devices, the modeling of interconnects, the modeling and emulation of fabrication processes and equipment, atomistic material modeling, parameter extraction, compact models for advanced and novel technologies, performance benchmarking, and the modeling of reliability and variability mechanisms. Other topics include the modeling of novel computing approaches (e.g. neuromorphic and quantum computing) and the modeling of interactions between process, device, circuit, and packaging including thermal, mechanical, and electromagnetic effects. Submissions should advance the state-of-the-art in modeling and simulation or apply existing techniques to gain new insights into device behavior.

OPTOELECTRONICS, DISPLAYS, and IMAGING SYSTEMS (ODI)

Papers are solicited on devices, structures, and integration for optoelectronics, displays, and imaging systems. Optoelectronics focus is on photonic-electronic process integration schemes and devices advancing the state-of-the-art. There is particular interest in platform technologies enabling energy efficient scaling of optoelectronic applications such as silicon photonics towards and beyond 100Gbaud, including novel approaches to the integration of light sources, high speed modulators and photodetectors. Furthermore, papers are solicited in the area of large-scale heterogeneous integration of electronic and photonic circuits for optical interconnects, on-chip networks and sensing. Papers on quantum photonics for computation, sensing and encryption are also of interest. Displays and imagers include CMOS imagers, high speed and high time-resolution imagers, CCDs, TFTs, organic, amorphous, and polycrystalline devices, as well as emissive and reflective displays. Papers addressing flexible and/or stretchable electronics, printed electronics, stacked image sensors with Si or other photosensitive materials, organic and inorganic displays, and covering new technology trends in imagers and displays are encouraged. Papers concerning optoelectronic integration for neuromorphic and quantum computing, as well as VCSEL/micro LED display applications are welcomed.

POWER DEVICES and SYSTEMS (PDS)

Papers are solicited on discrete and integrated power devices, modules and systems using Si, diamond, and compound semiconductors. Papers exploring the system-level impact of power devices are also of interest. Topics of interest include power devices (diodes, BJTs, FETs, superjunction devices, IGBTs, etc.), and materials (Si, diamond, SiC, GaAs, GaN, AlN, Ga2O3, etc.), manufacturing processes, device design, TCAD modeling, physics, and reliability. Devices targeting the full range of power and power conversion applications, including automotive, power supplies for computers and data centers, power conditioners for photovoltaic, motor drives and smart grid (solid-state transformers and HVDC transmission), and wireless power transfer, are of interest besides fundamental studies on doping, deep-level traps, interface state densities and device reliability for power switches.

RELIABILITY OF SYSTEMS and DEVICES (RSD)

Papers are solicited in all areas of electrical and physical characterization, reliability evaluation and yield analysis of transistors, interconnects, circuits and systems mainly (but not limited) to Si-, Ge- and SiGe-based technologies. Specific reliability topics include, for FEOL: transistor degradation due to hot carriers and bias temperature instabilities; dielectric wear-out and breakdown; self-heating effects; process charging damage; latch-up and ESD; soft error mechanisms in logic and memories. For MEOL/BEOL, topics include: electromigration failure of contacts and interconnects; breakdown of BEOL dielectrics and MEOL spacers; thermal management. For system and circuit reliability, topics include: design for reliability and variability-aware design, robustness and security of electronic circuits and systems. Of particular interest are investigations of degradation mechanisms for devices, circuits and systems in the following areas: emerging memories; More-than-Moore applications; biomedical devices and systems; automotive and aerospace.

SENSORS, MEMS, and BIOELECTRONICS (SMB)

Papers are solicited in the areas of sensors, micro/nano electromechanical systems (MEMS and NEMS), microfluidics and bioelectronics, with particular emphasis on new device concepts, integrated implementations, CMOS co-integration, flexible devices and multi-sensors on a chip for wearable and IoT applications. The sensors area includes chemical, molecular and biological detection based on electrical, electrochemical, mechanical and optical principles. Topics of interest in the MEMS area include actuators, physical sensors, resonators, integrated inertial measurement units, RF MEMS, micro-optical and optomechanical devices, micro power generators, devices for energy harvesting and on-chip energy storage as well as micro/nanofluidics for thermal management. The Bioelectronics area covers organic-inorganic hybrid devices, bio-electronic interface, integrated biomedical sensing and implantable neural interfaces.

Program

See the Program Download for all abstracts and speaker bios.

Tutorials

The tutorials are in their ninth year and are 90 minute stand alone presentations on specialized topics taught by world-class experts. These tutorials will provide a brief introduction to their respective fields, and facilitate understanding of the technical sessions. In contrast, the traditional short courses are intensive full-day events focused on a single technical topic.

All Tutorials will be On Demand starting on Saturday, December 5 (will be held PST)

Live Q&A with the Lecturers for Tutorials 1-3 will be on Saturday, December 12, 7:50AM-8:45AM (PST)

Live Q&A with the Lecturers for Tutorials 4-6 will be on Saturday, December 12, 9:00 AM- 9:45 AM (PST)

- Oxide Semiconductors and Application, Hideo Hosono, Tokyo Institute of Technology
- In-memory Computing for AI, Abu Sebastian, IBM Research – Zurich
- Magnetic Field Sensors, Keith Green, Texas Instruments
- Cryogenic MOSFET Modeling, Christian Enz, EPFL
- Ferroelectric Memories and Beyond, Johannes Muller, Globalfoundries and Thomas Mikolajick, NaMLab/TuDresden
- Sequential Integration, Perrine Batude, LETI

Short Courses

IEDM will offer two, full-day short courses with in-depth coverage of highly relevant topics from world experts. Advance registration is recommended. Details on the short courses will be published later this year.

Sunday, December 8, 2019, 9:00 a.m. – 5:30 p.m.

Short Course 1 – Technology Scaling in the EUV Era and Beyond

Course Organizer: Wook-Hyun Kwon, Samsung

- Future of Computing: From Core to Edge Computing, Karim Arabi, Atlazo
- Device Technology for 3nm and Beyond, Jin Cai, TSMC
- EUV Lithography Technology, Ho Chul Kim, Samsung
- Design Technology Co-Optimization for 3nm and Beyond, Lars Liebmann, TEL
- Novel Interconnect Techniques for Advanced Devices Beyond 3nm Technologies, Chris Wilson, IMEC
- Ultra-Low Power Devices for Advanced Signal Processing Architectures, Arokia Nathan, Cambridge Touch Technologies, University of Cambridge

Short Course 2: Technologies for Memory-Centric Computing

Organizer: Ali Keshavarzi, Stanford University

- Memory Devices and Selectors for High-Density Memory Technologies, Alessandro Calderoni, Micron Technology
- 3D-Stacked DRAM Technology and Function-in-Memory Solution, Kyomin Sohn, Samsung
- Novel Memory Technologies for Advanced Nodes, Oleg Golonzka, INTEL
- Emerging Technologies for Memory-Centric and Low Power Architectures, Edith Beigne, Facebook
- Towards Memory-Centric Autonomous Systems: A Technology and Device Perspective, Arijit Raychowdhury, Georgia Institute of Technology
- 3D NAND: Challenges and Potentials, Jian Chen, Western Digital

Plenary Session

Welcome and Awards

General Chair: Mariko Takayanagi, Toshiba

Plenary Papers

Technical Program Chair: Suman Datta, Notre Dame University

Plenary 1

Process and Packaging Innovations for Moore's Law Continuation and Beyond (Invited), Robert Chau, Senior Fellow, Intel Corporation

Plenary 2

Continued Scaling in Semiconductor Manufacturing Enabled by Advances in Lithography (Invited), Martin van den Brink, President and CTO, ASML

Plenary 3

Future of Non-Volatile Memory: From Storage to Computing (Invited), K. Ishimaru, Institute of Memory Technology R&D, Kioxia Corporation

Focus Sessions

As every year, IEDM 2019 will offer Special Focus Sessions on emerging topics with invited talks from world experts to highlight the latest developmets. Below are this year's Focus Sessions.

Session 10 – Monday, December 9, 1:30 PM, Sensors, MEMS and BioElectronics/Optoelectronics, Displays, and Imagers, Focus Session: Human Machine Interface

Session 13 – Tuesday, December 10, 9:00 AM, Reliability of Systems and Devices , Focus Session: Reliability and Security in Circuit and Systems

Session 22 – Tuesday, December 10, 2:15 PM, Memory Technology/Emerging Device and Compute Technology, Focus Session: Emerging AI Hardware

Session 31 – Wednesday, December 11, 9:00 AM, Emerging Device and Compute Technology, Focus Session: Quantum Computing Infrastructure

Career Session

Tuesday, December 10, 12:15– 2:00 p.m.

Grand Ballroom B

Speakers:

From Datacenters to Wearables: The Continuing Evolution of Moore's Law

Ramune Nagisetty, Sr. Principal Engineer and Director of Process-Product Integration, Intel Corporation

A Passion for Technology: Memory and Macro Trends

Linda K. Somerville, Ph.D., Corporate Vice President of Technology Strategy and Operations, Micron Technology, Inc.

Technical Program

See the Program Download for all abstracts and speaker bios.

Monday – December 9

- Session 1 – Plenary Session — 9:00 am – 12:00 pm
- Technical Sessions – 1:30 pm – 5:00 pm
- Session 2 – Memory Technology – STT-MRAM

- Session 3 – Advanced Logic Technology – Monolithic 3D Integration and BEOL Transistors
- Session 4 – Power Devices and Systems – Advances in GaN Power Devices and GaN Monolithic Integration
- Session 5 – Reliability of Systems and Devices – Back End and Advanced Characterization
- Session 6 – Emerging Device and Compute Technology – EDT-Neuromorphic Session I-Device Focus
- Session 7 – Modeling and Simulation – Physics of Ferroelectric and Negative Capacitance Devices
- Session 8 – Optoelectronics, Displays, and Imagers – Circuitry for Optoelectronics
- Session 9 – Microwave, Millimeter Wave and Analog Technology – Compound Semiconductors and Novel Materials for RF and mmWave
- Session 10 – Sensors, MEMS and BioElectronics/Optoelectronics, Displays and Imagers – Focus Session: Human Machine Interface

Monday 6:30 pm – 8:00 pm

- Reception – 6:30 pm – 8:00 pm
- Tuesday – December 10
- Technical Sessions 9:00 am – 12:30 pm
- Luncheon – 12:30 pm- 2:00 pm
- Technical Sessions 2:15 pm – 5:30 pm
- IEDM Evening Panel Session – 8:00 pm – 10:00 pm

Tuesday – 9:00 am – 12:30 pm

- Session 11 – Advanced Logic Technology – Gate-All-Around Device Technologies
- Session 12 – Power Devices and Systems – Advances in Silicon and Galium Oxide Power Device Technologies
- Session 13 – Reliability of Systems and Devices – Focus Session: Reliability and Security in Circuit and Systems
- Session 14 – Emerging Device and Compute Technology – Neuromorphic Session II-Architecture Focus
- Session 15 – Memory Technology – Ferroelectrics
- Session 16 – Optoelectronics, Displays, and Imagers – Image Sensors
- Session 17 – Microwave, Millimeter Wave and Analog Technology – III-Nitride Devices and Co-Integration
- Session 18 – Sensors, MEMS and BioElectronics – Biomedical Sensors and Neural Interfaces
- Career Luncheon Tuesday, December 10, 12:25 – 2:10 PM

Tuesday – 2:15 pm – 5:30 pm

- Session 19 – Advanced Logic Technology – BEOL and 3D Packaging Innovation
- Session 20 – Power Devices and Systems – SiC Power Devices
- Session 21 – Reliability of Systems and Devices – Emerging Transistor Reliability and Pertinent Strategies
- Session 22 – Memory Technology/Emerging Device and Compute Technology – Focus Session: Emerging AI Hardware
- Session 23 – Emerging Device and Compute Technology – Emerging Devices for Extending Moore's Law
- Session 24 – Modeling and Simulation – Ab Initio Simulation of Materials, Devices, and Interconnects
- Session 25 – Microwave, Millimeter Wave, and Analog Technology – Advanced Si and Packaging Technologies for 5G and Beyond
- Session 26 – Sensors, MEMS, and Bioelectronics – Integrated Energy Devices and Sensors

Tuesday – 8:00 pm – 10:00 pm

- Session 27 – PANEL SESSION Tuesday, December 10, 8:00 p.m.

Wednesday – December 11

- Session 28 – Memory Technology – Charge Based Memory and Emerging Memories
- Session 29 – Advanced Logic Technology – High Mobility Ge-Based Channel Devices
- Session 30 – Reliability of Systems and Devices – Memory Reliability and Applications
- Session 31 – Emerging Device and Compute Technology – Focus Session: Quantum Computing Infrastructure
- Session 32 – Modeling and Simulation – Modeling of Emerging Memory Systems
- Session 33 – Optoelectronics, Displays, and Imagers – Silicon Photonics
- Session 34 – Sensors, MEMS, and Bioelectronics – Micro and Nano-electromechanical Resonant Sensors and Relays
- Session 35 –Memory Technology – Selectors and RRAM: Technology and Computing

- Session 36 – Advanced Logic Technology – CMOS Platform Technologies
- Session 37 – Emerging Device and Compute Technology – Nano Devices for Low-Power Technologies
- Session 38 – Memory Technology – Memory for Neural Network
- Session 39 – Modeling and Simulation – Multiscale Modeling of Devices and Circuits

SRC Student Showcase Poster Session

Tuesday, December 10th, 2:00 – 4:00 pm

Yosemite Ballroom

Returning for a second year, Semiconductor Research Corporation (SRC) and IEEE Electron Devices Society (EDS) are co-hosting a student research showcase. SRC is sponsored by industry members and government agencies with the mission to drive advances in materials, devices, processing, metrology, and modeling, among other areas. Because these topics are relevant to the IEDM and EDS community, SRC and EDS are organizing a poster session led by students highlighting fundamental semiconductor research in universities worldwide. This session will be a great opportunity to engage with student researchers and their budding ideas.

Learn more at the SRC Event Page: https://www.src.org/calendar/e006864/

Panel Discussion

Tuesday, December 8, 8:00 PM – 10:00 PM

Continental 1-5

Rest in Peace Moore's Law, Long Live AI

Moderator: Vijay Narayanan, IBM Research

The traditional benefits of Dennard Scaling, the engine behind Moore's law, is facing considerable headwinds with significant increase in process complexity and patterning cost with each successive logic node. At the same time, the demand for compute and memory resources needed for ingesting, processing and extracting actionable intelligence from large volumes of structured and unstructured data is growing exponentially. This is fueling research and development in novel compute technologies and heterogeneous integration techniques.

We assemble a team of industry and academic panelists who will discuss and debate the future of computing and the role of hardware. Will CMOS technology become commoditized and differentiation occur mostly in circuit design, algorithm and architecture development? Will special purpose co-processor adoption rate accelerate beyond CPUs and GPUs ? What is the role of heterogeneous integration in the AI Hardware Eco-system? Will the traditional memory hierarchy be upended by the arrival of non-volatile memory? Will Analog Accelerators using non-volatile memory elements drive the future semiconductor roadmap as scaling slows, enabling exponential improvements in compute efficiency and performance? These are many of the questions that are on all of our minds and we look forward to having an engaging dialogue with the experts on the panel.

Panelists:

- Vivek De, Intel
- Wilfried Haensch, IBM Research
- Mike Henry, Mythic
- Ron Ho, Facebook
- Seongjun Park, Samsung
- Dimitri Strukov, University of California,Santa Barbara
- Douglas Yu, TSMC

Exhibits & Exhibit Events

IEDM 2019 will host an Exhibits area during the conference where you can learn more about the latest products and publications. This will be open in the Yosemite Ballroom during the conference from Monday 12:00 pm, through Wednesday 12:00 pm. Stop by any time during the exhibition open hours to browse the booths and enjoy complementary coffee. The Exhibition will be open to all IEDM attendees as well as qualified Exhibit Only participants.

Exhibition Opening Times

Monday: 12:00 p.m. – 4:00 p.m.

Tuesday: 8:00 a.m. – 4:00 p.m.

Wednesday: 8:00 a.m. – 12:00 p.m.

Complementary coffee will be available in the exhibits area

INFORMATION ON EXHIBITING IN 2019

2019 IEEE – IEDM exhibits will feature products, equipment and services directly related to the areas covered by the Conference. Information is available by writing to:

Scien-Tech Associates, Inc., P.O. Box 2097, Banner Elk, NC 28604-2097

Tel: 1-828-898-7001 Fax: 1-828-898-6379

Email: exhibits@ieee-iedm.org

MRAM Posters and Forum

Technically sponsored by the IEEE Magnetics Society

Two IEEE Magnetics Society events at IEDM 2019

With the rising interest of the microelectronics industry in STT-MRAM, it is very important to strengthen the relationship between the microelectronics and magnetism communities since this technology requires expertizes from both areas. For that, two special events related to MRAM technology are being organized around IEDM by the IEEE Magnetics Society with the particular help of the program committee formed of D. Worledge (Program chair), B. Dieny (General chair), L. Thomas, K.J. Lee, S. Fukami, J. Katine, K. Gao and of P. Mahoney and J.A. Incorvia for the logistics.

1) A special poster session dedicated to MRAM

(Wednesday 11 December 2019, 9am-Noon, YOSEMITE Ballroom)

Various topics will be covered including MRAM materials, phenomena, technology, testing, hybrid CMOS/MTJ technology and circuits, spin-logic. Similar MRAM poster sessions took place at IEDM 2016 and IEDM2017 which were very successful with more than 30 posters presented and very active cross-disciplinary discussions. This year, 30 posters were accepted for presentation. This session is technically organized by the IEEE Magnetics Society. This event is a great opportunity to bring

together experts in magnetism and in microelectronics. Participants in this poster session need to register at IEDM as regular attendees. More information including the list of presented posters are posted on the IEEE Magnetics Society website: http://www.ieeemagnetics.org/

2) The 11th MRAM Global Innovation Forum

(Hilton Union Square, IMPERIAL Ballroom), 12 Dec 2019

This is a one-day forum organized the day following IEDM (i.e on 12 December 2019, 8:45am – 5:30pm) in the same hotel as IEDM (Hilton Union Square, 333 O'Farrell St, San Francisco). The Forum will consist of 10 invited talks from leading experts and a panel discussion on "MRAM for AI". Various MRAM related topics will be covered including STT-MRAM technology, memory and processor demonstrations, spin orbit torque MRAM, and the needs, challenges and potential of MRAM. The Forum was originally initiated by Samsung Semiconductor, and this forum marks the 11th edition of the series.

The Forum is entirely supported by Samsung Semiconductor and IEEE Magnetics Society. The registration to the Forum is free of charge. To register to the Forum, send an email to incorvia@austin.utexas.edu with first name, last name, contact email, affiliation. A confirmation email will be sent to you. The deadline for registering to the Forum is 15th November 2019.

More information including the Forum program is posted on the IEEE Magnetics Society website: http://www.ieeemagnetics.org/

EDS Function

The time to make those important professional connections is now!

Sponsored by the IEEE EDS Young Professionals and Women in Electron Devices Committees.

Attend the IEEE EDS Women in Engineering and Young Professionals Breakfast Networking Event

Monday, 9 December 2019 7:30 AM to 9:00 AM

Hilton San Francisco 4th Floor, Union Square 15 and 16

Meet and network with your peers and leaders in the electron devices community. Stop by for a complimentary continental breakfast, and pick up important tips to help you make the most of the conference.

A valuable experience you should not miss!

2019 Heterogeneous Integration Roadmap (HIR)

Sunday, 8 December 2019 5:30 PM to 7:00 PM

Hilton San Francisco Grand Ballroom Level, Grand Ballroom A

We have just announced the release of the 2019 Heterogeneous Integration Roadmap (HIR).

The roadmap can be downloaded from the EPS HIR Page.

A press release was also just issued –

https://www.businesswire.com/news/home/20191010005211/en/2019-Heterogeneous-Integration-Roadmap-HIR-Identifies-Long-Term

IRDS Panel Discussion

Sunday, 8 December 2019 6:00 PM to 8:00 PM

Hilton San Francisco Franciscan Room

IRDS promotes cooperative approach to overcome the end of the semiconductor industry Hilton San Francisco Union Square, 333 O'Farrell Street, San Francisco, CA

Appendix - Abstracts, Bios & Technical Program

Tutorial 1: Oxide Semiconductors and Application

Hideo Hosono, Tokyo Institute of Technology

Oxide semiconductor has a long research history comparable to Si/Ge semiconductors but almost no distinct device application was seen up to ~2012. Since then, oxide TFTs represented by amorphous IGZO-TFTs are practically used to drive pixels of advanced displays such as high precision LCDs and large-sized OLED-TVs. Oxide semiconductors rather differ from conventional semiconductors such as Si in several respects. This striking difference arises from that in chemical bonding nature, i.e., ionic vs. covalent. Understanding oxide semiconductors in comparison with Si will enable us to get a comprehensive view for semiconducting materials. In this lecture I talk about historical background, chemical bonding, p/n-orientation and band lineup, materials design concept and concrete materials for crystalline and amorphous oxide semiconductors, and application to TFTs as channel semiconductors and perovskite LEDs as electron injection/transport layer. Emphasis is placed on crystalline and amorphous IGZO-TFTs and their characteristics and instability issue. Recent reviews and monographs are also introduced for further reading.

Tutorial 2: In-memory Computing for AI

Abu Sebastian, IBM Research - Zurich

The explosive growth in data-centric artificial intelligence related applications necessitates a radical departure from traditional von Neumann computing systems, which involve separate processing and memory units. In-memory computing is one such approach where certain computational tasks are performed in place in the memory itself. This is achieved by exploiting in tandem the physical attributes of the memory devices, its array-level organization and peripheral circuitry as well as the control logic. Any computational task that is realized within the confines of these three units could be called in-memory computing. However, the key distinction is that at no point during computation, the memory content is read back and processed at the granularity of a single memory element. Both charge-based as well as resistance-based memory devices are being explored for in-memory computing. In-memory computing can be applied both to reduce the computational complexity of a problem via analog computing as well as to reduce the amount of data being accessed by performing computations inside the memory arrays. In this tutorial, I will provide a broad overview of the key computational primitives enabled by these memory devices as well as their applications spanning scientific computing, signal processing, machine learning, deep learning and stochastic computing. I will conclude with a discussion on the challenges and new directions of research.

Tutorial 3: Magnetic Field Sensors

Keith Green, Texas Instruments

The objective of this tutorial is to introduce magnetic field sensing to an audience that is not familiar with it. Applications and several magnetic field sensing technologies will be discussed. The majority of the tutorial will be spent on Hall-effect sensing, which is the most widely used technology. In particular, the tutorial will focus on integrated, silicon-based Hall sensors. Key performance characteristics of the sensing element will be explained. Also, attendees will have access to hand-on demonstrations to help them better understand Hall-effect sensors.

Tutorial 4: Cryogenic MOSFET Modeling

Christian Enz, EPFL

There is currently a large effort to try to miniaturize quantum computers taking advantage of solid-state technologies enabling a potentially large number of qubits operating in regimes that allow superposition and entanglement. CMOS is the preferred technology for building the qubit array and mixing it with the control and readout electronics taking advantage of the cryogenic temperature to operate the electronics at lower power and/or faster. The design and optimization of these CMOS analog and digital circuits need a compact transistor model that is valid down to cryogenic temperatures. Unfortunately, the current MOSFET compact models do not scale properly with temperature down to such low temperature. This tutorial will address this limitation. It starts with an assessment of the analog performance at cryogenic temperatures using the simplified EKV MOSFET model. The main effects occurring at cryogenic temperature are then described and a physics-based MOSFET model that scales down to ultra-low temperatures is then presented.

Tutorial 5: Ferroelectric Memories and Beyond

Johannes Műller, Globalfoundries

Recent advances in scaling and CMOS-compatible implementation of ferroelectric thin films has sparked renewed interest to utilize the unique properties of these materials in advanced CMOS technology nodes. Led by the ferroelectric memory development and further fueled by new applications fields such as steep slope devices and neuromorphic applications, this field has seen a strong growth in R&D activity over the last decade. This tutorial will give an introduction to ferroelectric materials and devices with special emphasis on the utilization of hafnium oxide based thin films. The working principle as well as the challenges of capacitors based ferroelectric random access memory (FRAM), ferroelectric field effect transistor (FeFET) and ferroelectric tunnel junction (FTJ) will be reviewed. In addition, a brief outlook on beyond memory applications of CMOS-compatible ferroelectric thin films will be given.

Tutorial 6: 3D Sequential Integration

Perrine Batude, LETI

3D sequential integration allows vertically stacking several layers of devices with a unique connecting via density above 10^8 via/mm^2. However, the thermal stability of the lower tier(s) constrains the thermal budget of the sequentially processed upper tier(s).

The first aim of this tutorial will be to present the main prospective application sectors, namely (i)Pursuing Moore's law without resorting to MOSFETs scaling ii) Enabling alternative computing paradigms through close proximity between logic and memory units iii) offering new heterogeneous co-integrations schemes for smart sensor arrays iv) adding low cost functionalities above ICs.

Moreover, major 3D sequential integration demonstrations examples will be reviewed revealing the rich diversity of stacked low temperature devices currently under study ranging from traditional low temperature Si MOSFETs, poly-Si TFTs, junction-less devices, carbon nanotubes, oxide semiconductors, etc.

This tutorial will give a synoptic view of all the key enabling process steps required to build high performance Si CMOS with thermal budget preserving the integrity of active devices and interconnects (top channel formation, gate stack reliability, junction's activation, low resistivity gate realization, selective epitaxy, spacer's formation) and will sketch a status on current low temperature device performance with respect to their high temperature counterparts.

Future of Computing: From Core to Edge Computing,
Karim Arabi, Atlazo

Dr. Karim Arabi is founder and CEO of Atlazo, Inc. developing AI semiconductor and software for edge computing applications targeting the rapidly growing hearable, wearable and ultra-low power industrial IoT markets. Previously, he was Vice President, R&D at Qualcomm where was head of Corp. R&D ASIC and Hardware responsible for research and development and new product development. Karim was VP, Engineering and Technology at Dialog Semiconductor responsible for driving overall technology and new product development. Karim held technical positions at PMC Sierra and Cirrus Logic and was co-founder of Opmaxx, an innovative startup in analog design and test acquired by Credence in 1998. Karim obtained his Ph.D. and M.Sc. in Electrical Engineering from Polytechnique Montréal, Canada and his B.Sc. in Electrical Engineering from Tehran Polytechnic. Karim has published more than 100 papers in accredited journals and international conferences and holds several key patents.

Abstract: We are living in the era of Cloud Computing where most of data we produce or consume goes to or emanates from data centers, which are the backbone of Cloud Computing. Cloud Computing enabled major mega trends in competing such as Deep Learning. As a natural evolution of Cloud Computing, we are starting to move more computing back to the edge of the network to complement Cloud Computing. By moving some portion of the computing to the edge, it is possible to enable better response time and reduced data overload while offering enhanced privacy and lower power dissipation. This new paradigm shift in computing called Edge Computing is addressing applications where real-time processing of data is required. Prominent current and future applications of Edge Computing include gaming, AR/VR, Robotics, Drones, Autonomous Driving, Security, Camera, Health Monitoring and Industrial IoT.

Device Technology for 3nm and Beyond, *Jin Cai, TSMC*

Jin Cai received the B.S. degree in physics from Fudan University, Shanghai, China and the M.S. and Ph.D. degrees in electrical engineering from University of Florida, Gainesville, FL. In September 2000, he joined IBM T. J. Watson Research Center at Yorktown Heights, NY in the silicon technology department. He worked on exploratory device research and technology pathfinding, and contributed to several generations of advanced CMOS technology development. In June 2015, he joined TSMC in Hsinchu, Taiwan. He is currently a deputy technical director in Corporate Research. He has published in international conferences and IEEE journals in the areas of strained silicon CMOS, fully depleted SOI CMOS, low-pow device and circuits, lateral SOI bipolar and tunneling field-effect transistors. He is an author of a book chapter and over 60 papers. He was granted over 60 US patents. He is a senior member of IEEE and served as an associate editor for IEEE Electron Device Letters from 2008 to 2017.

Abstract: The advent of FinFET technology ushered in a new era of transistor scaling where channel geometry became the main driver for gate length scaling. Transistor density scaling has been augmented by design-technology co-optimization to keep CMOS circuit density improvement unabated over the past decade. In this short course, we will focus on the main device options for 3nm which include the incumbent FinFET technology and the emerging nanosheet option. Contacted gate pitch scaling puts pressure on gate length and contact length scaling. Innovations in gate stack, S/D contact, and channel mobility continue to improve FinFET performance. The nanosheet option brings some relief for gate length scaling but faces new integration challenges and device design limits. In the longer term, geometrical scaling for all bulk materials will hit a limit. Naturally-thin materials, such as 2D layered materials and carbon nanotubes, provide the ultimate channel geometry. These new channel materials will be discussed at the end of this short course.

EUV Lithography Technology, *Ho Chul Kim, Samsung*

Dr. Ho Chul Kim is a research for advanced lithographic technology, R&D department in Samsung Electronics. He is an advanced lithography specialist such as aberration, RET (resolution enhancement technology) and flare since 1998. Recently, he is working on lithography strategy planning including EUV lithography technology. He obtained his Ph. D. and M.S. in Physics at Seoul National University, 1998.

Abstract: As a new lithographic technology, EUV lithography had been introduced and will be used for mass production of 7nm logic devices and beyond. There are several big changes from previous lithographic technology like KrF, ArF and ArF Immersion. Defects, CD control and productivity enhancement became more difficult for EUV lithography. Several approaches to overcome the difficulties at EUV lithography are introduced at this course.

Design Technology Co-Optimization for 3nm and Beyond, *Lars Liebmann, TEL*

Lars Liebemann spend over 25 years enabling semiconductor scaling first at an IDM and then a foundry, Lars Liebmann recently joined Tokyo Electron at their TEL Technology Center America, Albany, NY. Having received BS and MS degrees in Nuclear Engineering and a PhD in Engineering Physics from Rensselaer Polytechnic Institute, Troy, NY, Dr. Liebmann started working on semiconductor scaling in 1991 when critical dimensions were approaching a quarter micron. As his work on resolution enhancement techniques became increasingly complex and layout invasive, he found himself interacting with the design community earlier and more fundamentally in every technology node. These engagements on restrictive design rules, lithography friendly design, and multiple exposure enhanced design flows laid the foundation for what is now known as design-technology co-optimization (DTCO). After spending a decade advancing DTCO as a means of developing robust technology definitions in the early stages of leading-edge technology nodes. Dr. Liebmann joined TEL where he is focusing primarily on 3D integration as a means of maintaining semiconductor scaling. He holds over 95 patents, has published over 70 technical papers, is a fellow of SPIE, and summarized his early tenure work in a book: 'Design Technology Co-Optimization in the Era of Sub-resolution IC Scaling'.

Abstract: The semiconductor industry is on the verge of hitting what appears to be the most decisive scaling barrier yet. While the end of VLSI logic scaling has been prophesized and proven wrong many times in the last five decades, the imminent end to any possibility of further reduction in critical dimensions is cause for concern. As with the many scaling barriers that have come before, we will engineer our way through this to prosper for many more technology nodes. Though unlike the barriers of the past, this one will require unprecedented interdisciplinary collaboration to maintain meaningful value-add at a time when the three main pillars that have supported this industry: Moore, Dennard, and von Neumann are all crumbling. 3D integration for logic scaling, unlike memory, is not merely an exercise in integrating transistor density in volume rather than area; it is an exercise in deriving value from highly-complex system-level benefits. Just as pitch-based scaling with a focus on resolution enhancement techniques (RET) gave way to design-technology co-optimization (DTCO) with a focus on scaling boosters such as self-aligned gate contacts (SAGC) and buried power-rails (BPR), we are now transitioning to the era of system-technology co-optimization (STCO) to exploit value from solutions such as complementary FET (CFET) and 3D integrated logic. When once it was seen as revolutionary those etch engineers and lithography engineers collaborated, we are now challenged to synergistically innovate across the entire spectrum of the design-to-silicon infrastructure. After briefly reviewing the contributions DTCO has made to semiconductor scaling thus far, this short course will show examples of how engineers with skillsets in diametrically opposed specialties within our broad technical endeavor have to join forces to seek out opportunities for incremental value gain. Through examples focused on different potential 3nm node scenarios, attendees will be introduced to DTCO's latest 'tools of the trade', including process emulation and technology prototyping to quantify achievable power-performance-area-cost (PPAC) gains.

Christopher J. Wilson received the Ph.D. degree from Newcastle University, Newcastle upon Tyne, U.K., and the MBA degree from the Vlerick Business School, Leuven, Belgium. He is a Principal Member of Technical Staff with Imec, Leuven, Belgium, where he manages both the Nano-Interconnect Program and Back end of line Integration team. His team is responsible for projects covering advanced node integration, patterning and EUV exploration, advanced metallization, CPI vehicles, interconnect modelling and road mapping. His previous roles include Project Manager and Senior Scientist, where he led a broad range of projects. He is an active member of the IEEE Interconnect Technology Conference (IITC) and Materials for Advanced Metallization (MAM) committees, and recently chaired the 2019 IITC/MAM joint conference.

Abstract: Interconnects are no longer simply the wiring for devices, rather becoming enablers of new concepts and architectures for advanced nodes. In this short course a toolbox of options will be reviewed to keep pace and drive PPA scaling for 3nm technology and beyond. Scaling boosters to help with pattering, yield and area scaling will be reviewed. These include: Fully-Self-Aligned-Via (FSAV) and Self-Aligned-Block (SAB) techniques to reduce variability and enhance edge placement error (EPE) tolerance; multi-level high aspect ratio Super-Vias (SV) mitigate minimum area and via extension restrictions; and Buried Power Rails (BPR) to enable track height scaling. The extendibility of traditional Cu-Low-k and entry points for the integration of alternative metals will be discussed. Finally, disruptive metal etching integration schemes to maintain aggressive RC scaling will be motivated.

Ultra-Low Power Devices for Advanced Signal Processing Architectures,
Arokia Nathan, Cambridge Touch Technologies, University of Cambridge

AROKIA NATHAN (S'84-M'87-SM'99-F'10) received the Ph.D. degree in electrical engineering from the University of Alberta. Following post-doctoral years at LSI Logic Corp., USA, and ETH Zurich, Switzerland, he joined the University of Waterloo, Canada, where he held the DALSA/NSERC Industrial Research Chair in sensor technology and subsequently the Canada Research Chair in nano-scale flexible circuits. He was a recipient of the 2001 NSERC E.W.R. Steacie Fellowship. In 2006, he moved to the UK to take up the Sumitomo Chair of Nanotechnology at the London Centre for Nanotechnology, University College London, and subsequently held the Chair of Photonic Systems and Displays in the Department of Engineering, Cambridge University, where he led a multi-disciplinary research group working on the heterogeneous integration of materials and processes, sensors, energy harvesting and storage devices pertinent to wearable technologies. He is currently the Chief Technical Officer of Cambridge Touch Technologies, a company spun out of his lab at the University of Cambridge developing advanced interactive technologies. He received the Royal Society Wolfson Research Merit Award and recently the BOE Distinguished Contribution Award for TFT Compact Modeling and Circuit Design. He has held Visiting Professor appointments at the Physical Electronics Laboratory, ETH Zürich and the Engineering Department, Cambridge University, UK. He has published over 600 papers in the field of sensor technology, CAD, thin film transistor electronics, and is a co-author of four books. He has over 100 patents filed/awarded and has founded/co-founded four spin-off companies. He serves on technical committees and editorial boards in various capacities. Dr. Nathan is a Chartered Engineer (U.K.), Fellow of the Institution of Engineering and Technology (UK), Fellow of IEEE (USA), and an IEEE/EDS Distinguished Lecture

Abstract: Thin film semiconductor materials, such as oxides and organics, are becoming key for the future flexible electronics because of their potentially wide band gap, hence high transparency and low OFF current, compared with the ubiquitous silicon counterparts. These material systems can be processed at low temperature and at low fabrication cost, which makes them amenable for integration on a wide range of substrate materials including plastic and paper. This course will review the new generation of applications using selected oxides and organics ranging from large area flexible electronics to the newly emerging Internet of Things. While the thin film transistor continues to evolve, producing devices with higher mobility, steeper sub-threshold slope and lower threshold voltage, practical analog signal processing circuits are constrained by issues related to non-uniformity, electrically- and illumination-induced instability, and temperature dependence. We will discuss the critical design considerations of displays, sensors and sensor interfaces, along with advanced signal processing architectures, to show how device-circuit interactions should be handled and how compensation methods can be implemented. In particular, the quest for low power becomes highly compelling in newly emerging application areas related to wearable devices in the Internet of Things. We will discuss thin-film transistor operation near the OFF state, driven by the pivotal requirement of low supply voltage and ultralow power. The operation of the wearable device is challenged by limited battery lifetime even if augmented with energy harvesting. One of the key requirements for design of flexible electronics for these emerging applications is physically-based circuit models, which requires good knowledge of the underlying transport mechanisms in the thin film transistor, and in particular, the associated density of states and field-effect mobility. The major developments in thin film transistor modeling for computer-aided design of circuits and systems will be reviewed, along with simple and compact analytical description of the current-voltage characteristics of thin film transistors in the above-threshold and sub-threshold regions for expedient circuit simulations.

Memory Devices and Selectors for High-Density Memory Technologies,
Alessandro Calderoni, Micron Technology

Alessandro Calderoni received the Laurea degree in Electrical Engineering (cum laude) from Politecnico di Milano, Italy, in 2006. He joined the Research and Development department of STMicroelectronics (then Numonyx) in 2006 and the Emerging Memory department of Micron Technology in 2010. He has been working on Emerging Memory for more than 10 years in different roles and with different responsibilities. His research interests include: CMOS modeling; NAND characterization and modeling; Phase Change Memory (PCM) array characterization and reliability, transport mechanisms and low-frequency noise characterization and modeling; Read margin improvement tool development; different RRAM and CBRAM systems with particular focus on reliability aspects; Cross-point architectures evaluation and selector device characterization; path-finding evaluation of DRAM-like architectures. He is currently a Senior Manager of Device Technology in the Emerging Memory Research and Development Team at Micron Technology.

Abstract: Over the last decade, the Memory Sub-System has become a fundamental bottle-neck for all Computing Systems from mobile devices to servers. The exponential increase of generated data and the growing demand for faster processing and analytics on big data has sparked the interest for in-memory computing. In-memory computing demands a significant increase of main memory (DRAM) density as well as high performance memories. DRAM scaling requires an aggressive and cost-effective lithography roadmap and it faces several materials and process integration challenges. New Emerging Memories may enable scaling beyond the limits of existing technologies as well as offer alternative ways to design a system architecture that enables a memory-centric computing (as opposed to a long history of processor-centric computing). In this course, we will be discussing scaling challenges of traditional memories (DRAM and NAND) as well as focus on Emerging Memory requirements for high-density applications.

3D-Stacked DRAM Technology and Function-in-Memory Solution,
Kyomin Sohn, Samsung

Kyomin Sohn received the B.S. and M.S. degrees in Electrical Engineering in 1994 and 1996, respectively, from Yonsei University, Seoul. From 1996 to 2003, he was with Samsung Electronics, Korea, involved in SRAM Design Team. He designed various kinds of high-speed SRAM for external cache and buffer memory. He received the Ph.D. degree in Electrical Engineering and Computer Science in 2007 from KAIST, Daejeon, Korea. He rejoined Samsung Electronics in 2007, where he has been involved in DRAM Design Team. He is a Master (Technical VP) in Samsung and he is responsible for design and development of HBM (High Bandwidth Memory) DRAM. His interests include the next generation 3D-DRAM, robust memory design, and processing-in-memory for artificial intelligence applications. In addition, he has currently served as a Technical Program Committee member of Symposium on VLSI Circuits since 2012.

Abstract: Advances in 3D-stacked DRAM technology has been essential in today's High-Performance Computing (HPC) and AI applications. HBM (high bandwidth memory) DRAM can provide unparalleled high bandwidth by ultra-wide IO utilizing 3D-stacked DRAMs with TSV technology. An advanced 2.5D integrated packaging technology using Si-interposer is also one of the key enablers for the critical HBM DRAM. However, there are many challenges in realizing systems with these technologies like power density, thermal dissipation, testability and reliability of 3D-DRAM stacking in 2.5D configuration. All these topics will be explained and discussed in this talk. Furthermore, data-centric and memory-intensive computing are pursued actively because of big data and the efficient use of it. HBM DRAM has great possibility for more efficient and powerful near-memory computing. In this talk, a Function-in-Memory (FIM) solution as a near-data-processing platform will be provided with various considerations based on the technology fundamentals covered in this short course.

Novel Memory Technologies for Advanced Nodes, *Oleg Golonzka, INTEL*

Dr. Oleg Golonzka is a Principal Engineer at Intel Corporation. He received his BA/MS from Moscow Institute of Physics and Technology and completed his Doctoral and Post-Doctoral studies in Physics at The Pennsylvania State University and Massachusetts Institute of Technology. Oleg Golonzka joined Portland Technology Development Division of Intel Corporation in 2001 and worked on device and process integration of Intel's 65nm, 32nm, and 14nm CMOS nodes. Most recently he led the device development and process integration of Intel's STT-MRAM and RRAM-based embedded Non-Volatile Memory technologies.

Abstract: Recent years witnessed rapid acceleration in the development of new memory technologies. Several of them have reached performance and yield levels suitable for high volume manufacturing and commercialization. This work covers the device physics and array-level characterization for STT-MRAM and RRAM, and further discusses the suitability of these technologies for solving embedded memory needs of advanced CMOS nodes in Non-Volatile and High-Bandwidth-High-Endurance application space.

Emerging Technologies for Memory-Centric and Low Power Architectures,
Edith Beigne, Facebook

Edith Beigné joined Facebook Inc. in Menlo Park in November 2018 to lead the AR/VR Silicon Research team. Before that, she was with CEA-LETI, Grenoble, France, from 1998 to 2018 where she was the Research Director of Integrated Circuits and System Division. Since 2009, she has been a senior scientist in the digital and mixed-signal design lab where she focused on low power and adaptive circuit techniques, exploiting asynchronous design and advanced technology nodes like FDSOI 28nm and 14nm for many different applications from high performance MPSoC to ultra-low power IoT applications. Her main research interests today are low power digital and mixed-signal circuits and design with emerging technologies. She is part of ISSCC TPC since 2014 and part of VLSI Symposium TPC since 2015. Distinguished Lecturer for the SSCS in 2016/2017, Women-in-Circuits Committee chair and JSSC Associate Editor since 2018. She visited Stanford University in 2018.

Abstract: Many of today's edge computing applications are suffering from high energy and lack of on-chip memory capacity. Memories are the most power-hungry components in many of these applications. Significant improvement can be traded off by using new emerging technologies like 3D integration and Non-volatile memories. This course will first discuss power and integration challenges for edge computing applications and give an overview of alternate technologies to be used in conjunction with CMOS technologies. State-of-the-art solutions for design and architecture leveraging non-volatile memories and 3D integration will be presented. We will conclude on Augmented Reality applications challenges.

Towards Memory-Centric Autonomous Systems: A Technology and Device Perspective, *Arijit Raychowdhury, Georgia Institute of Technology*

Arijit Raychowdhury is currently a Professor in the School of Electrical and Computer Engineering at the Georgia Institute of Technology where he joined in January 2013. He is the co-director of the Georgia Tech Quantum Alliance. From 2013 to July 2019 he was an Associate Professor and held the ON Semiconductor Junior Professorship in the department. He received his Ph.D. degree in Electrical and Computer Engineering from Purdue University (2007) and his B.E. in Electrical and Telecommunication Engineering from Jadavpur University, India (2001). His industry experience includes five years as a Staff Scientist in the Circuits Research Lab, Intel Corporation, and a year as an Analog Circuit Researcher with Texas Instruments Inc. His research interests include low power digital and mixed-signal circuit design, design of power converters, sensors and exploring interactions of circuits with device technologies. He and his students have won eleven best paper awards and multiple fellowships and awards over the years. Dr. Raychowdhury is a Senior Member of the IEEE.

Abstract: As we look at future computing systems, we realize the need for fundamentally new approaches to sustain the exponential growth in performance beyond the end of the CMOS roadmap. In particular, we observe that new computing models that deal with “data analytics” have compute and storage interleaved in a fine grained manner - not separated as in the Von Neumann world. Such a paradigm shift requires breakthrough innovations in memory technologies, BEOL and FEOL devices, packaging and integration as well as computing architectures that can be married to these technologies. In this talk, I will discuss the latest advances in near-memory and in-memory computing circuits and their potential when integrated in novel memory arrays. In particular, I will discuss the promise of working with various resistive memory technologies and how they can accelerate the pathway towards future autonomous systems. Furthermore, I will show examples of some of the fundamental and engineering limitations in the associated technologies and devices that can be addressed by careful system design. Overall, the focus of the talk will be on devices and technologies that are needed to build end-to-end autonomous systems for example used in micro robots applications and more.

3D NAND: Challenges and Potentials, *Jian Chen, Western Digital*

Jian Chen is Senior Vice President of Technology for Western Digital, responsible for the company's overall 3D NAND technology development. Prior to his current role, he was Vice President of Memory System Engineering, led the exploring of novel storage system architecture and eco-system for emerging memories, and managed the memory system group, responsible for the architecture design of USB, CF, SD/µSD, and SSD products from 2007 to 2013. From 1999 to 2007, he started as device manager for the first Toshiba-SanDisk joint project 0.16um 1G MLC NAND development, and involved in all subsequent generations of 2D NAND development in various roles, including 3 years starting the first 300mm joint fab in Yokkaichi Japan. From 1996 to 1999, he worked on the original SanDisk triple-poly NOR technology as device, foundry and FA engineer. Prior to SanDisk, he worked on 3 generations of NOR flash memory at AMD. Holder of over 140 granted US patents, he is co-author of a book chapter on Flash Memory Reliability and JEDEC flash memory reliability standard. He is the author of several key patents that have been used in NAND for over 15 years, such as binary cache, coupling canceling technique, fast programming method and cell airgap. He published the papers that first discovered and coined the term GIDL. He received his MS and Ph.D. in EECS from UC Berkeley, and B.S. in Solid State Device Physics from University of Electronic Science and Technology, Chengdu, China.

Abstract: In our modern data abundant and dominant world, memory and storage are becoming ever more important in the memory and computing hierarch. As an industry, we are gifted with secular and insatiable demand with no end in sight. In the past 30 years, we have successfully met that challenge, scaled the NAND flash cost by more than one million times with 17 generations of 2D and 3D NAND technologies, increased density, performance and functionality, and played critical role in transforming modern mobile world. As successor to the floating gate 2D NAND, charge-trap 3D NAND technology has successfully been developed and entered the 100+ layer era, with various architectures choices that focus on optimization of different parameters. The industry is facing huge challenges in further scaling and cost reduction, with abundant opportunities for Capital tool vendors, for new process and material and architecture innovations. 3D NAND is also quite veritable, with proper design trade-offs, within the same technology generation, it can offer chips with write performance from 10MB/s to 1GB/s, read access time from 100us to 1us, endurance from 1 thousand to 1 million, and cost difference of 10X. There is opportunity for the industry to utilize the full spectrum of capabilities and values of the ever-scaling 3D NAND technology.

2019 Technical Program

Session 1: Plenary
Monday, December 9, 9:00 AM
Grand Ballroom B

Welcome and Awards
General Chair: Mariko Takayanagi, Toshiba

Plenary Papers
Technical Program Chair: Suman Datta, University of Notre Dame

1.1 Process and Packaging Innovations for Moore's Law Continuation and Beyond (Invited)
1.2 Robert Chau, Senior Fellow, Intel Corporation

For the last 50 years Moore's Law has been the guiding principle for the silicon industry, enabled by numerous process innovations. Yet in the last few years there has been great concern that Moore's Law will soon come to a halt. This presentation will describe various game-changing process and packaging technologies that will enable both monolithic and system 3D heterogeneous integration to continue Moore's Law scaling, while improving performance/Watt. Beyond EUV capability, new patterning techniques using DSA, new interconnects using subtractive metal etch and 2D barriers, high performance Ge and 2D-material transistors, GaN devices, hybrid bonding and Omni Directional Interconnect for packaging, are all enablers. Furthermore, many of these new technologies enable new, exciting integrated circuit opportunities such as monolithic co-integration of GaN devices and Si CMOS on the same wafer for future 5G and power delivery products. By using these new and exciting technologies holistically, and coupled with technology and design co-optimization, the future of Moore's Law is brighter than ever.

1.2 Continued Scaling in Semiconductor Manufacturing Enabled by Advances in Lithography (Invited)
Martin van den Brink, President and CTO, ASML

An important contributor to Moore's Law is physical scaling of devices enabled by advances in lithography. This year, extreme-UV lithography (EUVL) entered high-volume manufacturing at the 7-nm node of logic integrated circuits. Efforts to uphold Moore's Law include continued enhancements of system performance and the development of high-numerical-aperture (0.55 NA) EUVL systems. They also include constant innovations in well-established deep-UV lithography systems that have been driving down cost of ownership and have supported the manufacturing of new device architectures e.g. 3D memories. Full potential of lithography – its ultimate capability when used in manufacturing – is realized by making exposure systems, metrology tools, and computational algorithms/software work together synergistically. Continued advances in this holistic lithography will enable cost-effective scaling in semiconductor device manufacturing beyond the next decade.

1.3 Future of Non-Volatile Memory: From Storage to Computing (Invited), K. Ishimaru
Institute of Memory Technology R&D, Kioxia Corporation

More than thirty years have passed since the first NAND flash memory was presented at the IEDM. NAND flash memory expanded its market and application by reducing the cost per bit ($/GB) and will continue in coming decades. Many innovations, such as double/quadruple patterning, multi-bit programming, wear leveling, etc. were introduced to keep the cost trend and improve the performance. Now 5G and AI are changing our society and "memory centric" computing system is required. Non-volatile memory is a key component to enable this paradigm shift. The challenges and opportunities of NAND flash and other emerging memories for next decades will be discussed.

Session 2 - Memory Technology - STT-MRAM
Monday, December 9, 1:30 p.m.
Grand Ballroom A
Co-Chairs: G. Hu, IBM TJ Watson Research Center
S. Kang, Qualcomm

1:35 PM **2.1** Demonstration of a Reliable 1 Gb Standalone Spin-Transfer Torque MRAM For Industrial Applications
Sanjeev Aggarwal, Hamid Almasi, Mark DeHerrera, Brian Hughes, Hui Lu, Sumio Ikegawa, Jason Janesky, Han Kyu Lee, Frederick Mancoff, Kerry Nagel, Goei Shimon, Jijun Sun, Tom Andre, Syed Alam, Everspin Technologies

We demonstrate reliable operation of our 1 Gb standalone STT-MRAM product over a temperature range of -40C to 110C. Well-behaved read and write distributions over 4 sigma enable an endurance lifetime of 2e11 cycles and data retention of 10 years at 85C.

2:00 PM **2.2** 1Gbit High Density Embedded STT-MRAM in 28nm FDSOI Technology
Kilho Lee, Samsung Electronics

High density 1Gb embedded STT-MRAM in 28nm FDSOI technology was successfully demonstrated. Based on the highly reliable and manufacturable eMRAM technology, high yield over 90% was achieved with satisfying read, write function and 10 years retention. Improved endurance up to 1E10 cycles was achieved to broaden eMRAM applications.

2:25 PM **2.3** Manufacturable 22nm FD-SOI Embedded MRAM Technology for Industrial-grade MCU and IOT Applications
Vinayak Bharat Naik, Kangho Lee, Kazutaka Yamane, Robin Chao, Jae-Hyun Kwon, Naganivetha Thiyagarajah, Nyuk Leong Chung, Suk Hee Jang, Behtash Behin-Aein, Jia Hao Lim, Tae Young Lee, Wah Peng Neo, Hemant Dixit, Sivabalan K, Lian Choo Goh, Timothy Ling, Jay Hwang, Dinggui Zeng, Jia Wen Ting, Eng Huat Toh, Lei Zhang, Rachel Low, Nivetha Balasankaran, Li Ying Zhang, GLOBALFOUNDRIES Singapore Pte. Ltd, GLOBALFOUNDRIES Malta Pte. Ltd.

We demonstrate the manufacturable 22nm FD-SOI embedded-MRAM by achieving product functionality and reliability in package level at -40~125 °C. The product reliability is confirmed by passing LTOL, HTOL, 1M endurance and 5x-solder reflows tests. In addition, we demonstrate the macro capability to cover magnetic immunity of >500 Oe.

2:50 PM *COFFEE BREAK*

3:15 PM **2.4** 2 MB Array-Level Demonstration of STT-MRAM Process and Performance Towards L4 Cache Applications
Juan G. Alzate, Intel Corporation, Umut Arslan, Peng Bai, Justin Brockman, Yu-Jin Chen, Nilanjan Das, Kevin Fischer, Tahir Ghani, Philip Heil, Patrick Hentges, Rawshan Jahan, Aaron Littlejohn, Mohammad Mainuddin, Daniel Ouellette, James Pellegren, Tanmoy Pramanik, Conor Puls, Pedro Quintero, Tofizur Rahman, Meenakshi Sekhar, Bernhard Sell, Mansi Seth, Andrew Smith, Angeline Smith, Intel Corporation

We demonstrate 2 MB arrays of scaled-size MTJ devices capable of meeting L4 Cache specifications across all proposed temperatures of operation. The technology achieves ECC-correctable bit fail rates for a 20 ns write time, a 4 ns read time, endurance of 10^{12} cycles, and retention of 1 second at 110C.

3:40 PM **2.5** A Novel Integration of STT-MRAM for On-chip Hybrid Memory by Utilizing Non-Volatility Modulation,
Jeong-Heon Park, Joonmyoung Lee, Junho Jeong, UngHwan Pi, Whan Kyun Kim, SungChul Lee, EUNSUN NOH, Kwangseok Kim, WOOCHANG LIM, Shin Kwon, Byoung-Jae Bae, InHo Kim, NaYoung Ji, Kilho Lee, HyunChul Shin, Shin Hee Han, Sohee Hwang, Daeeun Jeong, Junghyuk Lee, Sechung Oh, Soon Oh Park, Yoonjong Song, Gitae Jeong, Gwan-Hyeob Koh, Samsung Electronics

We demonstrate a novel way of integrating STT-MRAM for on-chip hybrid memory which exhibits either features of high-retention or high-speed implemented in separate zones in a single chip. For satisfying high-temperature retention requirement, tailored MTJs are shown to support > 10 year retention at 220℃.

4:05 PM **2.6** Spin-transfer torque MRAM with Reliability 2ns Writing for Last Level Cache Applications
Guohan Hu, Janusz Nowak, Matthias Gottwald, Stephen Brown, Bruce Doris, Christopher D'Emic, Pouya Hashemi, Dimitri Houssameddine, Qing He, Daeshik Kim, Samsung Electronics, Juhyun Kim, Samsung Electronics, Raman Kothandaraman, Gen Lauer, H. K. Lee, Nathan Marchack, Mark Reuter, Ray Robertazzi, Jonathan Sun, Thitima Suwannasiri, Philip Trouilloud, Seonghoon Woo, Daniel Worledge, IBM Research

Reliable 2ns switching of STT-MRAM devices was achieved for the first time by demonstrating 100% write-error-rate yield at 1e-6 write-error floor of 254 devices. A single device with less than 1e-11 write-error rate was demonstrated with 2ns write pulses. Reliable 3ns switching was demonstrated with a completely different stack design.

4:30 PM **2.7** 22nm STT-MRAM for Reflow and Automotive Uses with High Yield, Reliability, and Magnetic Immunity and with Performance and Shielding Options (Late News)
William Gallagher, Eric Chien, Tien-Wei Chiang, Jian-Cheng Huang, Meng-Chun Shih, C.Y. Wang, Chih-Hui Weng, Sean Chen, Christine Bair, George Lee, Yi-Chun Shih, Chia-Fu Lee, Po-Hao Lee, Roger Wang, Kuei-Hung Shen, J.J. Wu, Wayne Wang, Harry Chuang, TSMC

We demonstrate high yielding solder-reflow-capable STT-MRAM embedded in 22nm CMOS. The technology supports -40 to 150°C operation and has ten-year native magnetic field immunity >1100 Oe at 25°C at 1ppm bit upset level, with a shield-in-package demonstrating even higher immunity. Trading off retention, higher performance and endurance are also demonstrated.

Session 3 - Advanced Logic Technology - Monolithic 3D Integration and BEOL Transistors
Monday, December 9, 1:30 p.m.
Grand Ballroom B
Co-Chairs: S. Eccofey, Universite de Sherbrooke
P. Baars, Globalfoundries

1:35 PM **3.1** Monolithic 3D BEOL FinFET Switch Arrays Using Location-Controlled-Grain Technique in Voltage Regulator with Better FOM than 2D Regulators
Chihchao Yang, TSMC

Monolithic 3D BEOL-FinFET switch arrays are demonstrated in large single crystalline Si islands (2.56 μm^2), whose location, size and shape are determined by design. Details of the improved LCG technique is presented. A voltage regulator implemented with the BEOL switch arrays shows better theoretical FOM(0.089ns) than 2D voltage regulators(0.43ns).

2:00 PM **3.2** 3D-Stacked CAAC In-Ga-Zn Oxide FETs with Gate Length of 72 nm
Masashi Oota, Ltd, Yoshinori Ando, Ltd, Kazuki Tsuda, Satoru Oshita, Akio Suzuki, Kunihiro Fukushima, Shuhei Nagatsuka, Tatsuya Onuki, Ryota Hodo, Takayuki Ikeda, Shunpei Yamazaki, Semiconductor Energy Laboratory Co., Ltd

We have fabricated two monolithic 3D-stacked c-axis aligned crystalline In-Ga–Zn oxide FETs (CAAC-IGZO FETs) with a gate length of 72 nm using CAAC-IGZO as the channel material. A memory cell using the CAAC-IGZO FETs has long-term data retention, high-speed operation, and high endurance.

2:25 PM **3.3** Monolithic 3D SRAM-CIM Macro Fabricated with Stackable Gate-All-Around MOSFETs
FuKuo Hsueh, Chun-Ying Lee, Cheng-Xin Xue, Chang-Hong Shen , Jia-Min Shieh, Bo-Yuan Chen, Taiwan Semiconductor Research Institute, Yen-Cheng Chiu, Hsiu-Chih Chen, Ming-Hsuan Kao, Wen-Hsien Huang, Kai-Shin Li, Chien-Ting Wu, Kun-Lin Lin, Kun-Ming Chen, Guo-Wei Huang, Meng-Fan Chang, Chenming Hu, Wen-Kuan Yeh, Taiwan Semiconductor Research Institute, National Tsing Hua University, University of California Berkeley

For the first time, below 400^{o}C-fabricated gate-all-around (GAA) transistor fabrication process was demonstrated with monolithic computing-in-memory circuit. The 3D stackable GAA MOSFETs exhibit record-high $I_{on}I_{off}$ ratio (10^{8}) Moreover, the stackability of the GAA MOSFETs and the differential output of dual-mode 10T SRAM readout enable 2x throughput in the CIM circuitry.

2:50 PM *COFFEE BREAK*

3:15 PM **3.4** Inter-tier Dynamic Coupling and RF Crosstalk in 3D Sequential Integration
Petros Sideris, José Lugo, Perrine Batude, Laurent Brunet, Pablo Acosta-Alba, Sebastien Kerdiles, Claire Fenouillet-Beranger, Gilles Sicard, Olivier Rozeau, François Andrieu, Jean-Pierre Colinge, Gérard Ghibaudo, IMEP-LAHC, Christoforos Theodorou, CEA-Leti; UGA, IMEP-LAHC

An extensive analysis of the intertier dynamic coupling and RF crosstalk of digital circuits in 3D Sequential Integration concludes on the necessity of a Ground Plane insertion for several applications. A novel integration scheme of a polysilicon Ground Plane shows more than 20dB of RF crosstalk suppression up to 100GHz.

4:05 PM **3.5** BEOL Compatible 15-nm Channel Length Ultrathin Indium-Tin-Oxide Transistors with Ion = 970 μA/μm and On/off Ratio Near 1011 at Vds = 0.5 V
Li Shengman, Mengchuan Tian, Huazhong University of Science and Technolog, Chengru Gu, Runsheng Wang, Mengfei Wang, Xiong Xiong, Xuefei Li, Ru Huang, Yanqing Wu, Huazhong University of Science and Technology, Peking University

We fabricate ultrathin-body (3.5 nm) sub-100-nm channel length indium-tin-oxide transistors with ultrahigh on/off ratio near 10^{11} where the 15-nm-long ITO transistor exhibits I_{dmax} of 970 μA/μm at V_{ds} = 0.5 V. We demonstrated a record fast stage delay of 0.49 ns/stage for a 5-stage ring oscillator based on BST inverter.

Session 4 - Power Devices and Systems - Advances in GaN Power Devices and GaN Monolithic Integration
Monday, December 9, 1:30 p.m.
Continental Ballroom 1-3
Co-Chairs: P. Moens, ON Semiconductor
G. Prechtl, Infineon Technologies

1:35 PM **4.1** 1200 V Multi-Channel Power Devices with 2.8 Ω·mm ON-Resistance
Jun Ma, Catherine Erine, Minghua Zhu, Luca Nela, Peng Xiang, Kai Cheng, Elison Matioli, EPFL, Enkris Inc.,

This work demonstrates novel multi-channel GaN devices with slanted tri-gates, presenting high breakdown voltage of 1200 V on a highly-conductivity epi-structure with 80 Ω/sq and low on-resistance of 2.8 Ω*mm. The excellent figure-of-merit of 3.2 GW/cm ^{2} significantly outperforms conventional single-channel devices, providing a promising pathway for future efficient power devices.

2:00 PM **4.2** Impact Ionization Coefficients in GaN Measured by Above- and Sub-Eg Illuminations for p−/n+ Junction
Takuya Maeda, Tetsuo Narita, Shinji Yamada, Tetsu Kachi, Tsunenobu Kimoto, Masahiro Horita, Jun Suda, Nagoya University, Kyoto University, Toyota Central R&D Labs

We propose a novel method to extract impact ionization coefficients of electrons and holes using above- and sub-bandgap illuminations for a $p^-/n\ s^+$ junction diode. By analyzing the avalanche multiplication of electron- and hole-injected (Franz-Keldysh-induced) photocurrents, the impact ionization coefficients of electrons and holes in GaN are extracted separately.

2:25 PM **4.3** Investigation of nBTI degradation on GaN-on-Si E-mode MOSc-HEMT
Abygaël VIEY, William Vandendaele, Marie-Anne Jaud, Jacques Cluzel, Jean-Paul Barnes, Simon Martin, Alexis Krakovinsky, Romain Gwoziecki, Marc Plissonier, Fred Gaillard, Roberto Modica, Ferdinando Iucolono, Matteo Meneghini, Enrico Zanoni, Gaudenzio Meneghesso, Gérard Ghibaudo, CEA-Leti, ST Microelectronics, Grenoble Alpes University, University of Padova

We investigate the negative gate stress influence on V_{TH} instabilities in GaN devices. NBTI transients and complementary ToF-SIMS analysis reveal two trap populations positions involved on V_{TH} instabilities. Both of them are related to C_N acceptor traps. NBTI transients exhibit LG influence, which is consistent with the E-field distribution simulation.

3:15 PM **4.4** GaN-on-SOI: Monolithically Integrated All-GaN ICs for Power Conversion
Xiangdong Li, Nooshin Amirifar, imec, Karen Geens, imec, Ming Zhao, imec, Weiming Guo, Hu Liang, Shuzhen You, Niels Posthuma, Brice De Jaeger, Steve Stoffels, Benoit Bakeroot, Dirk Wellekens, Benjamin Vanhove, Thibault Cosnier, Robert Langer, Denis Marcon, Guido GroesenekenStefaan Decoutere, imec/KULeuven, imec, KU Leuven

We report the first comprehensive research about GaN power ICs on GaN-on-SOI. HEMT, MIM capacitor, SBD, 2DEG resistor, and resistor-transistor logic (RTL) are co-integrated. A 48V-to-1V buck converter is realized using 200 V GaN half-bridges with integrated drivers. Further, an all-GaN buck converter is successfully designed using the GaN PDK.

3:40 PM *COFFEE BREAK*

4:05 PM **4.5** GaN/AlN Schottky-gate p-channel HFETs with InGaN Contacts and 100mA/mm On-current
Samuel Bader, Reet Chaudhuri, Austin Hickman, Kazuki Nomoto, Shyam Bharadwaj, Han Wui Then, Huili Xing, Debdeep Jena, Cornell University, Intel Corporation

High-performance wide-bandgap p-channel devices are broadly desirable to expand the design topologies available in power/RF electronics. To meet that need, this work advances the GaN-on-AlN platform.

Authors fabricate p-channel HFETs with 100mA/mm on-currents at room temperature. Various temperature-dependencies, benchmarking results, and technology perspectives are discussed.

4:30 PM **4.6** First Demonstration of a Self-Aligned GaN p-FET
Nadim Chowdhury, Qingyun Xie, Mengyang Yuan, Nitul Rajput, Peng Xiang, Enkris Inc., Kai Cheng, Han Wui Then, Tomas Palacios, Massachusetts Institute of Technology, Khalifa University, Enkris Inc., Intel Corporation

A self-aligned p-FET with GaN/$Al_{0.2}$ Ga 0.8 N (20 nm)/GaN heterostructure grown by MOCVD on Si-substrate is demonstrated. Reported Lg=100 nm E-mode p-FET V_{TH} =-1V , exhibits a record R_{ON} =400 Ω·mm and I_{ON} >5 mA/mm with I_{ON} /I_{OFF} =6×10^{5} among p-FETs based on GaN/AlGaN heterostructure, making it a promising candidate for GaN-based complementary circuit technology.

Session 5 - Reliability of Systems and Devices - Back End and Advanced Characterisation
Monday, December 9, 1:30 p.m.
Continental Ballroom 4
Co-Chairs: K. Weide-Zaage, Leibniz Universität Hannover
G. Reimbold, CEA-LETI

1:35 PM **5.1** Reverse Tip Sample Scanning for Precise and High-Throughput Electrical Characterization of Advanced Nodes
Umberto Celano, Thomas Hantschel, Thijs Boehme, Antti Kanniainen, Lennaert Wouters, Hugo Bender, Niels Bosman, Chris Drijbooms, Steven Folkersma, Kristof Paredis, Wilfried Vandervorst, Paul van der Heide, imec

A new method is proposed to enable high-throughput and high-resolution electrical atomic force microscopy in nanoelectronics. Using a reversed pathway of operation, our technique yields an increased time-to-data (>10x), enhanced dataset statistics and nm-precise resolution; as herein demonstrated for two- and three-dimensional carrier profiling in fin structures of advanced nodes.

2:00 PM **5.2** Hot-Spot Thermal Sensor Design in FinFETs
L. Liu, TSMC

This paper analyzes device-structure-induced and process- dependent temperature inaccuracy sources of thermal sensing applications in FinFETs: Self-heating and Joule-heating interaction, non-uniform FinFET-array temperature distribution, and distance limitation due to gate-area non-uniformity. Thermal behaviors of these inaccuracy sources are comprehensively characterized to mitigate the temperature gap between hot-spots and measurements.

2:25 PM **5.3** Characterizing Electromigration Effects in a 16nm FinFET Process Using a Circuit Based Test Vehicle
Nakul Pande, Chen Zhou, M. H. Lin, Rita Fung, Rick Wong, Shi-Jie Wen, Chris Kim, University of Minnesota, Maxim Integrated, TSMC, Cisco

This work showcases measured data corresponding to direct-current (DC) stress induced electromigration (EM) phenomenon, characterized using on-chip circuits for mutiple interconnect test structures fabricated in a 16nm FinFET process.

2:50 PM *COFFEE BREAK*

3:15 PM **5.4** Humidity Penetration Impact on Integrated Circuit Performance and Reliability,

Franco Stellari, Cyril Cabral, Peilin Song, Robert Laibowitz, IBM Research

We study the impact of humidity penetration into ICs . We found that the humidity penetration causes the performance of the circuit to be reduced because of the BEOL capacitance increase, while no detectable impact on the overall circuit lifetime is observed because of FEOL BTI and GOX mechanisms dominance.

3:40 PM **5.5** Non-Planarization Cu-Cu Direct Bonding and Gang Bonding with Low Temperature and Short Duration in Ambient Atmosphere
Tzu-Chieh Chou, Kai-Ming Yang, Jian-Chen Li, Ting-Yang Yu, Ying-Ting Chung, Cheng-Ta Ko, Yu-Hua Chen, Tzyy-Jang Tseng, Kuan-Neng Chen, National Chiao Tung University, Unimicron Technology Corp.

Low temperature (150ºC) and short duration Cu-Cu direct bonding, without planarization, and gang bonding approaches are demonstrated. The concept is based on the high stress-led inducing deformation and internal friction to achieve low temperature bonding. The bonding structure has the advantage of high roughness tolerance on surface without CMP requirement.

Session 6 - Emerging Device and Compute Technology - EDT-Neuromorphic Session I-Device Focus
Monday, December 9, 1:30 p.m.
Continental Ballroom 5
Co-Chairs: U. Avci, Intel Corp.
Q. Liu, Chinese Academy of Sciences

1:35 PM **6.1** Reducing the Impact of Phase-Change Memory Conductance Drift on the Inference of large-scale Hardware Neural Networks
Stefano Ambrogio, Mathieu Gallot, Katherine Spoon, Hsinyu Tsai, Charles Mackin, Marie Wesson, Harvard University, Sanjay Kariyappa, Pritish Narayanan, Chi-Chun Liu, Arvind Kumar, An Chen, Geoffrey W Burr, IBM Research, Harvard University

We analyze the impact of conductance drift and noise in Deep Neural Networks (DNNs) inference. We provide PCM array partial-set states experimental characterization, describe the impact of drift on Fully-Connected DNN on MNIST, ResNet on CIFAR-10 and LSTM on Alice-in-Wonderland, and we consider 1/f and Random Telegraph Noise sources.

2:00 PM **6.2** Performance Maximization of In-Memory Reinforcement Learning with Variability-Controlled $Hf_{1-x}Zr_xO_2$ Ferroelectric Tunnel Junctions,
Kensuke Ota, Marina Yamaguchi, Radu Berdan, Takao Marukame, Yoshifumi Nishi, Kazuhiro Matsuo, Kota Takahashi, Yuta Kamiya, Shinji Miyano, Jun Deguchi, Shosuke Fujii, Masumi Saitoh, Toshiba Memory Corporation, Kioxia Corporation

We develop strategies to maximize performance and reliability of in-memory reinforcement learning with $Hf_{1-x}Zr_xO_2$ ferroelectric tunnel junction. Small cycle-to-ccle variability and large voltage tuning window is desirable. $Hf_{1-x}Zr_xO_2$ thinning reduces variability, while voltage margin is larger with lower Zr concentration. Device size scaling enables low-power, high-density, and high-reliability reinforcement learning.

2:25 PM **6.3** Sub-nA Low-Current HZO Ferroelectric Tunnel Junction for High-Performance and Accurate Deep Learning Acceleration
Tzu-Yun Wu, Hsin-Hui Huang, Yueh-Hua Chu, Chih-Cheng Chang, Ming-Hung Wu, Chien-Hua Hsu, Chien-Ting WuMin-Ci Wu, Wen-Wei Wu, Tian-Sheuan Chang, Heng-Yuan Lee, Shyh-Shyuan Sheu, Wei-Chung Lo, Tuo-Hung Hou, National Chiao Tung University, Industrial Technology Research Institute, Taiwan Semiconductor Research Institute

A HZO FTJ operates at sub-nA current while achieving 50-ns switching, >10^7 endurance, >10-yr retention, and analog state modulation. We analyze an FTJ-based BNN. It achieves better accuracy and 702, 101, and 7×10^4 times improvements in power, area, and energy-area-product efficiency compared with those using NVMs with typical mA current.

2:50 PM **6.4** Capacitor-less Stochastic Leaky-FeFET Neuron of Both Excitatory and Inhibitory Connections for SNN with Reduced Hardware Cost
Jin Luo, Liutao Yu, Tianyi Liu, Mengxuan Yang, Zhiyuan Fu, zhongxin liang, Liang Chen, Shuhan Liu, Cheng Chen, Si Wu, Qianqian Huang, Ru Huang, Peking University

A capacitor-less L-FeFET neuron enabling both excitatory and inhibitory input connections with two transistors and one resistor isexperimentally demonstrated to emulate biological neuronal dynamics. The new neuron with dramatically-reduced hardware cost is applied to unsupervised SNN with the implementation of clustering and high-accuracy inference, showing great potentials for neuromorphic computing.

3:15 PM *COFFEE BREAK*

3:40 PM **6.5** Complementary Graphene-Ferroelectric Transistors as Synapses with Modulatable Plasticity for Supervised Learning
Yue Zhou, Nuo Xu, Bin Gao, Yangyang Chen, Boyi Dong, Yi Li, Yuhui He, Xiangshui Miao, Tsinghua University, Huazhong University of Science and Technology, University of California Berkeley, Tsinghua University

The complementary graphene-ferroelectric transistors (GFT) have been developed as synapses for the first time, which can be dynamically reconfigured between potentiative and depressive modes. Both modes demonstrate excellent linearity, small cycle-to-cycle variation of 2%, over 5-bit levels and power consumption of 8 pJ/per operation in MNIST learning task.

4:05 PM **6.6** A Novel Scalable Energy-Efficient Synaptic Device: Crossbar Ferroelectric Semiconductor Junction
Mengwei Si, Yandong Luo, Wonil Chung, Hagyoul Bae, Dongqi Zheng, Junkang Li, Jingkai Qin, Gang Qiu, Shimeng Yu, Peide Ye, Purdue University, Georgia Institute of Technology

A ferroelectric semiconductor α-In_2 Se_3 based crossbar ferroelectric semiconductor junction as a synaptic device is demonstrated. A metal-ferroelectric semiconductor-metal crossbar structure is used instead conventional ferroelectric tunnel junction. The crossbar ferroelectric semiconductor junction shows good on-line learning accuracy, low latency and energy consumption as a promising and competitive synaptic device.

4:30 PM **6.7** Experimental Demonstration of Conversion-Based SNNs with 1T1R Mott Neurons for Neuromorphic Inference
Xumeng Zhang, Zhongrui Wang, Wenhao Song, Rivu Midya, Ye Zhuo, Rui Wang, Mingyi Rao, Navnidhi Upadhyay, Qiangfei Xia, J. Joshua Yang, Qi Liu, Ming Liu, Institute of Microelectronics of Chinese Academy of Sciences, University of Massachusetts, Amherst

We experimentally demonstrated a one-layer SNN (320 ×10) based on fully memristive devices for the first time. Experimental results show 95.7% converting accuracy of the neurons and − 85.7% − recognition accuracy in − MNIST − datasetsAt last, a neuron X-bar architecture is proposed for parallel multi-tasking and better system integration.

Session 7 - Modeling and Simulation - Physics of Ferroelectric and Negative Capacitance Devices
Monday, December 9, 1:30 p.m.
Continental Ballroom 6
Co-Chairs: Y. Singh Chauhan, IIT Kanpur
A. Islam Khan, Georgia Institute of Technology

1:35 PM **7.1** Hysteresis-free Negative Capacitance in the Multi-Domain Scenario for Logic Applications
Jorge Gomez, Sourav Dutta, Kai Ni, Jeffrey Smith, Benjamin Grisafe, Asif Khan, Georgia Institute of Technology, Suman Datta, University of Notre Dame

We report for the first time that hysteresis-free negative capacitance can be achieved in a multi-domain FE-DE structure. The results could pave the way for understanding the design framework of robust, steep negative capacitance FETs (NCFETs) with multi- domain ferroelectrics.

2:00 PM **7.2** Revised Analysis of Negative Capacitance in Ferrolectric-Insulator Capacitors: Analytical and Numerical Results, Physical Insight, Comparison to Experiments
Tommaso Rollo, Franco Blanchini, Giulia Giordano, Ruben Specogna, David Esseni, University of Udine, Delft University of Technology

We present a revised analysis of Negative Capacitance(NC) in ferroelectric-insulator capacitors, focusing on the difference between MFMIM and MFIM-systems. We develop a model accounting for 3D-electrostatics, reporting analytical and numerical results. We explained the lack of NC operation in MFMIMs, compare well with experiments and enlighten the role of traps.

2:25 PM **7.3** Electrostatic Integrity in Negative-Capacitance FETs – A Subthreshold Modeling Approach (Invited)
Pin Su, Wei-Xiang You, National Chiao Tung University

Using a subthreshold potential model, this paper shows that the negative-capacitance FinFET inherently possesses a superior electrostatic integrity than the baseline FinFET. Considering the spacer-induced distributed-charges in our model, we demonstrate that an adequate spacer design can be utilized to further enhance the negative-capacitance effect and the EI for NC-FinFETs.

2:50 PM *COFFEE BREAK*

3:15 PM **7.4** Equivalent Oxide Thickness (EOT) Scaling With Hafnium Zirconium Oxide High-κ Dielectric Near Morphotropic Phase Boundary
Kai Ni, Atanu Kumar SahaWriddhi Chakraborty, Huacheng Ye, Benjamin Grisafe, Jeffrey Smith, G. Bruce Rayner, Sumeet Gupta, Suman Datta, University of Notre Dame, Purdue, Kurt J. Lesker Co.

We demonstrate a novel strategy to scaling the equivalent oxide thickness of MOSFETs by tuning the composition of $Hf_{1-x}ZrxO_2$ thin-film near morphotropic phase boundary, where orthorhombic ferroelectric phase and tetragonal anti-ferroelectric phase co-exist such that a small external electrical perturbation gets amplified to a large charge response through phase transformation.

3:40 PM **7.5** Surface potential-Based Compact Model for Negative Capacitance FETs Compatible for Logic Circuit: with Time Dependence and Multidomain Interaction,

Ying Zhao, Ling Li, Institute of Microelectronics, Chinese Academy of Sciences, Quan Li, Xichen Chuai, Guanhua Yang, Ming Liu, Qiang Li, Yue Peng, Genquan Han, Institute of Microelectronics of Chinese Academy of Sciences, University of Electronic Science and Technology of China, Xidian university

A continuous surface potential based compact model ofNCFET is proposed, incorporating the multi-domain interaction term, polarization relaxation, temperature dependence and scattering. For the first time, an analytical solution of surface potential without any empirical fitting parameters is obtained. The model is calibrated by experiment and successfully implemented into Verilog-A.

Session 8 - Optoelectronics, Displays, and Imagers - Circuitry for Optoelectronics
Monday, December 9, 1:30 p.m.
Continental Ballroom 7-9
Co-Chairs: B. Leo Kwak, Applied Materials
L. Zhou, BOE Corp.

1:35 PM **8.1** 14nm FinFET Process Technology Platform for Over 100M Pixel Density and Ultra Low Power 3D Stack CMOS Image Sensor
Donghee Yu, Choongjae Lee, Myoungkyu Park, Samsung, Samsung Electronics

CMOS Image Sensor(CIS) products need higher voltage device and better analog characteristics than conventional SOC & Logic products. This work presents newly developed 14nm FinFET process with 2.xV high voltage FinFET device characteristics showing excellent analog and low power digital characteristics comparing to 28nm planar process.

2:00 PM **8.2** High Performance Gigahertz Flexible Radio Frequency Transistors with Extreme Bending Conditions
Mengfei Wang, Mengchuan Tian, Zhenfeng Zhang, Huazhong University of Science and Technology, Li Shengman, Runsheng Wang, Chengru Gu, Xiaoyu Shan, Xiong Xiong, Xuefei Li, Ru Huang, Yanqing Wu, Peking University, Huazhong University of Science and Technology

Ultrathin indium tin oxide RF TFT have been demonstrated for the first time, with record-high extrinsic f_T of 2.1 GHz and f_{max} of 3.7 GHz. The stability of DC and RF performance after bending for 50,000 bending cycles or with 1 mm bending radius are studied without device failure.

2:25 PM **8.3** A Novel Structure Serving as a Stress Relief Layer for Flexible LTPS TFTs
Yu-Xuan Wang, National Chiao Tung University, Ting-Chang Chang, Shin-Ping Huang, Mao-Chou Tai, Yu-Zhe Zheng, Chia-Chuan Wu, Simon Sze, National Chiao Tung University, National Sun Yat-Sen University

A novel structural design, naming as wing-shape TFTs, is proposed to enhance the performances of flexible LTPS TFTs. By extending the active layer, also serving as a stress relief layer, removes the degradation regions away from the channel. No additional process is needed which leads its potential for commercialization.

2:50 PM *COFFEE BREAK*

3:15 PM **8.4** Self-Aligned Elevated-Metal Metal-Oxide Thin-Film Transistors for Displays and Flexible Electronics
Zhihe XIA, Lei Lu, Jiapeng LI, Hoi-Sing Kwok, Man Wong, The Hong Kong University of Science and Technology

Unlike the source/drain regions, formed using extrinsic dopants, of top-gate self-aligned (SA) metal-oxide (MO) thin-film transistors (TFTs), those of presently reported bottom-gate ones are formed using a thermal annealing process, improving TFT scalability. The demonstrated short-channel high-mobility (>20 cm^2/Vs) bottom-gate SA MO TFT is beneficial for displays and flexible electronics.

3:40 PM **8.5** Flexible, Active-Matrix Flat-Panel Image Sensor for Low Dose X-ray Detection Enabled by Integration of Perovskite Photodiode and Oxide Thin Film Transistor
Taoyu Zou, Changdong Chen, Sun Yat-sen University, Ben Xiang, Ya Wang, Chuan Liu, Sun Yat-sen University, Shengdong Zhang, Hang Zhou, Peking University Shenzhen Graduate School, Sun Yat-sen University

An image sensor based on low-cost two-step deposited perovskite photodiode arrays and oxide (IGZO) TFTs is demonstrated for direct and indirect X-ray imaging applications. The system can be fabricated on flexible substrates, and the perovskite photodiode exhibits a significant direct X-ray response, reaching a sensitivity of ~887 $\mu CGy^{1}\ cm^{-2}$

Session 9 - Microwave, Millimeter Wave and Analog Technology - Compound Semiconductors and Novel Materials for RF and mmWave
Monday, December 9, 1:30 p.m.
Imperial Ballroom A
Co-Chairs: M. Urteaga, Teledyne Science
F. Gianesello, STMicroelectronics

1:35 PM **9.1** First Demonstration of III-V HBTs on 300 mm Si Substrates Using Nano-Ridge Engineering
Abhitosh Vais, Liesbeth Witters, Yves Mols, Arturo Sibaya-Hernandez, Amey Walke, Hao Yu, Marina Baryshnikova, Veeresh Vidydhar Deshpande, Geert Mannaert, Reynald Alcotte, Mark Ingels, Piet Wambacq, Bertrand Parvais, Robert Langer, Bernadette Kunert, Niamh Waldron, Nadine Collaert, imec, imec/KU Leuven, imec/Vrije Universteit Brussel

In this paper, we demonstrate GaAs/InGaP HBTs grown on a 300 mm Si substrate. A DC current gain of ~112 and breakdown voltage, BV_{CBO} of 10 V is achieved. The emitter-base and base-collector diodes show an ideality factor of ~1.2 and ~1.4, respectively.

2:00 PM **9.2** Millimeter-wave InP Device Technologies for Ultra-high Speed Wireless Communications toward Beyond 5G
Hiroshi Hamada, NTT Corporation

300 GHz, 100 Gb/s InP-HEMT wireless transceiver (TRx) is presented. Fabricated TRx can handle the data rate of 100 Gb/s at the link distance of 2.2 meter. Furthermore, 120 Gb/s, 9.8 meter wireless data transmission was achieved by applying the newly designed high-linearity PAs to our TRx.

2:25 PM **9.3** Impact Ionization Control in 50 nm Low-Noise High-Speed InP HEMTs with InAs Channel Insets
Diego Calvo Ruiz, Tamara Saranovac, Daxin Han, Olivier Ostinelli, Colombo Bolognesi, ETH-Zurich

Composite InAs/GaInAs channels with thin InP subchannels can suppress impact ionization in 50 nm HEMTs and improve noise properties while outperforming similar devices in
$-f-_T/-f-_{MAX}$ These are the first HEMTs combining InAs insets with InP subchannels. Ionization is mapped/quantified over the $-I-_{DS}/-V-_{DS}$ domain, and correlated to $-NF-_{MIN}$ for different designs.

2:50 PM **9.4** Weyl Semi-Metal-Based High-Frequency Amplifiers
Alessandra Toniato, Bernd Gotsmann, Erik Lind, Cezar Zota, IBM Research – Zurich, Lund University

In this work, we propose and simulate a novel amplifier based on Weyl semi-metals. Results show the device provides high gain with extremely low power dissipation. This device is promising to replace HEMTs in quantum computers, where low power dissipation enables it to be integrated at lower cryostat temperature stages.

3:15 PM *COFFEE BREAK*

Microwave, Millimeter Wave and Analog Technology - Compound Semiconductors and Novel Materials for RF and mmWave
Monday, December 9, 1:30 p.m.
Imperial Ballroom A
Co-Chairs: M. Urteaga, Teledyne Science
F. Gianesello, STMicroelectronics

3:40 PM **9.5** Non-volatile RF and mm-wave Switches Based on Monolayer hBN
Myungsoo Kim, Emiliano Pallecchi, Ruijing Ge, Xiaohan Wu, Vanessa Avramovic, Etienne Okada, Jack Lee, Henri Happy, Deji Akinwande, The University of Texas at Austin, University of Lille

Non-volatile RF switches based on hBN is realized for the first time with low insertion loss ($\leq$ 0.2 dB) and high isolation ($\geq$ 15 dB) up to 110 GHz. It offers a promising combination of non-volatility, nanosecond switching, power handling, high cutoff frequency (43 THz), and heater-less ambient integration.

4:05 PM **9.6** Non-Reciprocal Acoustoelectric Amplification in Germanium-Based Lamb Wave Delay Lines
Faysal Hakim, Mehrdad Ramezani, Sushant Rassay, Roozbeh Tabrizian, University of Florida

This paper reports on the use of acoustoelectric effect in single crystal germanium for non-reciprocal amplification of Lamb waves in RF delay lines. Waves are electromechanically excited using thin-film aluminum nitride transducers and amplified by the application of a DC electric field across the Ge waveguide through the deformation-potential coupling.

Session 10 - Sensors, MEMS and BioElectronics/Optoelectronics, Displays, and Analog - Focus Session: Human Machine Interface
Monday, December 9, 1:30 p.m.
Imperial Ballroom B
Co-Chairs: H. Lee, KAIST
A. Tournier, STMicroelectronics

1:35 PM **10.1** The Neuropixels probe: A wafer-scale CMOS based integrated microsystems platform for neuroscience and brain-computer interfaces (Invited)
Barundeb Dutta, Alexandru Andrei, Timothy Harris, Carolina Mora-Lopez, John O'Callaghan, Jan Putzeys, Bogdan Raducanu, Simone Severi, Sergey Stavisky, Stanford Univers, Eric Trautmann, Marleen Welkenhuysen, Krishna Shenoy, imec, Stanford University, HHMI Janelia Research Campus

CMOS enabled high-density electrophysiology probes are enabling transformational neuroscience experiments, e.g., single neuron precision, multi region, neuronal activity recording. They have enabled recording in multi-probe experiments with large neuronal populations (> 3000 neurons). Initial studies in

primates indicate their transformational potential in brain computer interfaces and research in neural disorders.

2:00 PM **10.2** Soft bioelectronic interfaces for prevention, diagnostics and treatement of neurological disorders (Invited)
Giuseppe Schiavone, Florian Fallegger, Philip Schönle, Qiuting Huang, Stephanie Lacour, EPFL, ETH-Zurich

Direct, physical interfacing of electrical probes with the neural tissue enable monitoring and modulating neural activity. We report on current progress and remaining challenges in miniaturized, biomimetic and integrated implantable neural systems.

2:25 PM **10.3** Haptics-Led Innovation for Coming Society (Invited)
Kouhei Ohnishi, Takahiro Nozaki, Yuki Saito, Tomoyuki Shimono, Yokohama National University, Takahiro Mizoguchi, Keio Universiy, Motion Lib Inc.

The real haptics based on the Hadamard transformation brings not only the vivid sensation of contact task without any force sensor but also two important applications into the coming society. One is a high-quality tele-operation and the other is a playback of skilled motion by human.

2:50 PM **10.4** Challenges in the Development of Wearable Human Machine Interface Systems (Invited)
Brendan O'Flynn, Javier Torres, Salvatore Tedesco, Michael Walsh, Tyndall National Institute

Tyndall National Institute has developed a glove-like device for Human Computer Interaction based on inertial sensors. Industry 4.0 represents one of the main applications for the possibility to control and monitor integrated systems. Current research focuses on enhancing bidirectional latency, sensor modalities, haptic feedback, interoperability, mainly concerning collaborative robotics scenarios.

3:15 PM *COFFEE BREAK*

3:40 PM **10.5** Intelligent Vision Systems – Bringing Human-Machine Interface to AR/VR (Invited)
Chiao Liu, Andrew Berkovich, Song Chen, Hans Reyserhove, Syed Shakib Sarwar, Tsung-Hsun Tsai, Facebook Reality Labs

An all-day wearable AR/VR device in a glasses form factor needs new input modalities. The candidates include voice, eye gazing, hand/body/head gestures, and BCI. This paper describes computer vision based modalities and the sensor and system specifications, and propose solutions to the extremely stringent power, form factor and performance challenges.

4:05 PM **10.6** Low-Latency Interactive Sensing for Machine Vision (Invited)
Paul K. J. Park, Jun-Seok Kim, Chang-Woo Shin, Hyunku Lee, Weiheng Liu, Qiang Wang, Yohan J. Roh, Jeonghan Kim, Yotam Ater, Hyunsurk Ryu, Samsung Electronics

We introduce the low-latency interactive sensing and processing solution for machine vision applications. The event-based vision sensor can compress the information of moving objects in cost-effective way, which in turn, enables the energy-efficient and real-time processing in various applications such as person detection, motion recognition, and Simultaneous Localization and Mapping.

4:30 PM **10.7** High-speed Image Processing Devices and Its Applications (Invited),

Masatoshi Ishikawa, The University of Tokyo

We have developed a high-speed and low-latency image processing devices and systems. In this talk, their architectures and applications such as robotics, factory automation, fuman interface, bio/medical applications, 3D achieving, and vehicles will be explained by using videos.

Session 11 - Advanced Logic Technology - Gate-All-Around Device Technologies
Tuesday, December 10, 9:00 a.m.
Grand Ballroom A
Co-Chairs: S. Maitrejean, CEA
K.H. Cho, Samsung

9:05 AM **11.1** Vertical Nanowire and Nanosheet FETs: Device Features, Novel Schemes for Improved Process Control and Enhanced Mobility, Potential for Faster & More Energy Efficient Circuits
Anabela Veloso, Geert Eneman, Trong Huynh-Bao, Adrian Chasin, Eddy Simoen, Emma Vecchio, Katia Devriendt, Stephan Brus, Erik Rosseel, Andriy Hikavyy, Roger Loo, Vasile Paraschiv, BT Chan, Dunja Radisic, Waikin Li, J. J. Versluijs, Lieve Teugels, Farid Sebaai, Paola Favia, Hugo Bender, Eric Vancoille, Jeroen E. Scheerder, Claudia Fleischmann, Naoto Horiguchi, CEA-Leti, imec

We report on p&n vertical gate-all-around nanowire and nanosheet FETs, evaluating the impact of doping and key dimensions on: performance, variability, noise, reliability (junctionless vs. inversion-mode) using RMG, which enables a new scheme for enhanced mobility by stress. Gate (mis)alignment control and their potential as MRAM selector are also discussed.

9:30 AM **11.2** Multiple-Vt Solutions in Nanosheet Technology for High Performance and Low Power Applications
Ruqiang Bao, Koji Watanabe, Jingyun Zhang, Jing Guo, Huimei Zhou, Andrew Gaul, Muthumanickam Sankarapandian, Juntao Li, Alex Hubbard, Reinaldo Vega, Shanti Pancharatnam, Paul Jamison, Miaomiao Wang, Nicolas LOUBET, Veeraraghavan Basker, Daniel Dechene, Dechao Guo, Bala Haran, Huiming Bu, Mukesh Khare, IBM Research

We reported an innovative integration scheme to enable volumeless multi-Vt and metal multi-Vt to provide the multi-Vt solutions in NS technology for high performance computing and low power applications. Meanwhile, metal gate boundary control was also developed to enable variable NS widths on the same wafer to satisfy both applications.

9:55 AM **11.3** 3D-carrier Profiling and Parasitic Resistance Analysis in Vertically Stacked Gate-All-Around Si Nanowire CMOS Transistors
Pierre Eyben, Romain Ritzenthaler, An De Keersgieter, Umberto Celano, Thomas Chiarella, Anabela Veloso, Hans Mertens, Vanessa Pena, Gaetano Santoro, Jerome Machillot, Myungsun Kim, Toshihiko Miyashita, Naomi Yoshida, Hugo Bender, Olivier Richard, Kristof Paredis, Lennaert Wouters, Jerome Mitard, Naoto Horiguchi, imec

We have utilized s-SSRM in order to extract for the first time 3D carrier distributions into multi-channel h-GAA Si NW-CMOSFETs. Good correlation with DIBL characteristics could be established. Thanks to these results and to TCAD simulations we could give a first explanation of the ON-current performance increase of GAA pMOSFETs.

10:20 AM **11.4** A Novel Dry Selective Etch of SiGe for the Enablement of High Performance Logic Stacked Gate-All-Around NanoSheet Devices

Nicolas LOUBET, Subhadeep Kal, Cheryl Alix, Shanti Pancharatnam, Huimei Zhou, Curtis Durfee, Michael Belyansky, Nathaniel Haller, Koji Watanabe, Thamarai Devarajan, Jingyun Zhang, Xin Miao, Muthumanickam Sankarapandian, Mary Breton, Robin Chao, Andrew M Greene, Daniel Chanemougame, Kandabara Tapily, Jeffrey Smith, Veeraraghavan Basker, Aelan Mosden, Peter Biolsi, Trace Hurd, Rama Divakaruni, TEL Technology Center, America, LLC, IBM Research, Tokyo Electron America

In this paper, we demonstrate a first of a kind SiGe dry etch technique for the formation of inner spacers and for channel release, enabling stacked NanoSheet (NS) gate-all-around device architectures with a wide range of NS device widths on the same wafer, critical for power/performance optimization of this technology.

10:45 AM COFFEE BREAK

11:10 AM **11.5** Imaging, Modeling and Engineering of Strain in Gate-All-Around Nanosheet Transitors
Shay Reboh, Remi Coquand, Nicolas Loubet, Nicolas Bernier, Emmanuel Augendre, Robin Chao, Juntao Li, Victor Boureau, Jingyun Zhang, Raja Muthinti, Olivier Faynot, Tenko Yamashita, CEA-Leti, IBM Research

3D modelling of strains in GAANS is calibrated on hardware using TEM strain-mapping. Compression of channels due to stress from the encapsulation of source/drain is reversed to tensile after gate stack/contact modules. Si-channel cladded with SiGe illustrates the co-integration of compressive SiGe channels with limited change of the integration flow.

11:35 AM **11.6** Full Bottom Dielectric Isolation to Enable Stacked Nanosheet Transistor for Low Power and High Performance Applications
Jingyun Zhang, Andrew M Greene, Xin Miao, Lan Yu, Reinaldo Vega, Pietro Montanini, Curtis Durfee, Andrew Gaul, Shanti Pancharatnam, Charlotte D Adams, Heng Wu, Huimei Zhou, Tian Shen, Ruilong Xie, Muthumanickam Sankarapandian, Junli Wang, Koji Watanabe, Ruqiang Bao, Xuefeng Liu, Chanro Park, Hosadurga K Shobha, Praveen Joseph, Dexin Kong, Abraham Arceo De La Pena, IBM Research

In this paper, full −BDI − is first demonstrated on horizontally stacked Nanosheet device structures with − Lmetal 12 nm. The comparison of full − BDI scheme − vs − PTS scheme has been systematically studied. −BDI scheme can potentially provide: 1) good immunity of sub-channel leakage due to process variation; 2) power-performance co-optimization.

12:00 PM **11.7** First Demonstration of CMOS Inverter and 6T-SRAM Based on GAA CFETs Structure for 3D-IC Applications
Yao-Jen Lee, Taiwan, S.-W. Chang, P.-J. Sung, T.-Y. Chu, Darsen D. Lu, Chun-Jung Su, N.-C. Lin, C.-J. Wang, S.-H. Lo, H.-F. Huang, J.-H. Li, M.-K. Huang, Y.-C. Huang, S.-T. Huang, H.-C. Wang, Y.-J. Huang, J.-Y. Wang, L.-W Yu, Y.-F. Huang, FuKuo Hsueh, Chien-Ting Wu, W. C.-Y. Ma, C. L. Lin, K.-H. Kao, National Cheng Kung University, National Chiao Tung University, National Sun Yat-sen University, Feng Chia University

CMOS inverters and 6T-SRAM cells based on vertically stacked GAA CFET are experimentally demonstrated, which is promising for 3D-ICs applications. Manufacturing difficulties of vertically stacked source/drain electrodes of the CFET device is overcome by using junctionless transistors. TCAD modeling shows CFET inverter has lower input capacitance than standard CMOS.

Session 12 - Power Devices and Systems - Advances in Silicon and Galium Oxide Power Device Technologies

Tuesday, December 10, 9:00 a.m.
Continental Ballroom 1-3
Co-Chairs: S. Madathil, University of Sheffield
M. Higashiwaki, NICT

9:05 AM **12.1** Modeling Needs for Power Semiconductor Devices and Power Electronics Systems (Invited)
Ramchandra Kotecha, Gilberto Moreno, Bary Mather, Sreekant Narumanchi, National Renewable Energy Laboratory

As energy systems move towards wide-spread electrification, penetration of power semiconductor devices and power electronics continue to grow at a rapid pace. The modeling needs for semiconductor devices vary depending on the end-goal and the level of abstraction needed towards model formulation also changes with the size

9:30 AM **12.2** Progress in Si IGBT Technology – As An Ongoing Competition with WBG Power Devices (Invited),
Thomas Laska, Infineon

Starting from state of the art Insulated Gate Bipolar Transistors (IGBT) and its underlying device concepts, an outlook on next IGBT development steps is given resulting in ongoing significant power density and efficiency increase. So Si IGBT technology will still play an important role also for the next years.

9:55 AM **12.3** Dynamic Avalanche Free Design in 1.2kV Si-IGBTs for Ultra High Current Density Operation
Peng Luo, Shankar Madathil, Shin-ichi Nishizawa, Wataru Saito, University of Sheffield, Kyushu University

Detailed analysis of 1.2 kV trench gated IGBTs are undertaken through experiments and simulations to show the fundamental cause of the dynamic avalanche as well as a method to achieve DA free design for ultra-high current density operation and reliability in 1.2 kV Si-IGBTs.

10:20 AM COFFEE BREAK

10:45 AM **12.4** Single and Multi-Fin Normally-off Ga_2O_3 Vertical Transistors with a Breakdown Voltage Over 2.6kV
Wenshen Li, Kazuki Nomoto, Zongyang Hu, Tohru Nakamura, Hosei University, Debdeep Jena, Huili Xing, Cornell University

Record-high performance is achieved in normally-off β-Ga_2O_3 vertical fin power transistors: a breakdown voltage of 2.66 kV (at ->V_{gs} =0 V) and a specific on-resistance of 25.2 mΩ·cm^2. The effective channel mobility is significantly improved up to ~130 cm^2 /V·s with a post-deposition annealing process. A unique fin orientation dependence is revealed.

11:10 AM **12.5** First Demonstration of Waferscale Heterogeneous Integration of vertical MOSFETs on SiC and Si Substrates by Ion-Cutting Process
Wenhui Xu, Yibo Wang, Tiangui You, Xin Ou, Genquan Han, Haodong Hu, Shibin Zhang, Fengwen Mu, Tadatomo Suga, Yuhao Zhang, Yue Hao, Xi Wang, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Xidian University, Meisei University, Virginia Polytechnic Institute State University

We for the first time demonstrate the heterogeneous integration of 2-inch crystalline β- Ga_2O_3 thin films onto the SiC and Si substrates by ion-cutting process and the fabrication of high-performance β-Ga_2O_3MOSFETs on heterogeneous wafers. This is promising to overcome the fundamental thermal limitations of $Ga_2 O_3$ power devices.

Session 13 - Reliability of Systems and Devices - Focus Session: Reliability and Security in Circuit and Systems
Tuesday, December 10, 9:00 a.m.
Continental Ballroom 4
Co-Chairs: G. Konstadinidis, Google
G. Sethi, Amazon

9:05 AM **13.1** Challenges in Radio Frequency and Mixed-Signal Circuit Reliability (Invited)
Vijay Reddy, Samuel Martin, Kamel Benaissa, Cathy Chancellor, Karan Bhatia, Venkatesh Srinivasan, Vijay Rentala, Srikanth Krishnan, James Ondrusek, Texas Instruments

Reliability challenges encountered during the design of radio frequency (RF) and mixed-signal circuits are discussed. RF circuits can operate at voltages greater than twice the supply voltage and thus hot-carrier/off-state stress degradation are key considerations. Mixed-signal circuits also present a reliability challenge due to their stringent matching and offset requirements.

9:30 AM **13.2** Telemetry for System Reliability (Invited),
Robert Kwasnick, Intel Corporation

Computer systems must be highly reliable for satisfactory user experience. Telemetry enables gathering actionable data from users. We review using field data to decide use conditions for IC reliability modeling and optimizations. Then we present concepts and results about telemetry for IC health monitoring, focusing on issue detection and support.

9:55 AM **13.3** Enabling Prognostics of Robust Design with Interpretable Machine Learning (Invited)
Jay Sarkar, Cory Peterson, Western Digital

Robust systems need to account for physics of operational stresses across the life cycle. This research demonstrates analysis of system-internal parametric data of Solid-State Storage Devices with interpretable Machine Learning (ML) - as effective and novel means of proactive prognostics - with significant possibilities across novel usage and application areas.

10:20 AM **13.4** Security and Reliability – Friend or Foe (Invited)
Ingrid Verbauwhede, Kai-Hsin Chuang, KU Leuven

Security and reliability are more closely related than one might expect. This paper studies interesting research topics at the boundaries between the two domains. Reliability concerns can benefit security, e.g. to improve the performance of PUFs. Reliability issues can also trigger new security breaches, e.g. enabling Rowhammer attacks.

10:45 AM *COFFEE BREAK*

11:10 AM **13.5** Designing Secure Cryptographic Circuits (Invited)
Naofumi Homma, Tohoku University

Hardware security in mobile and embedded systems is drawing much attention in recent years. In particular, a variety of side-channel attacks on cryptographic circuits have been reported until now. This paper introduces the design of cryptographic circuits resistant to side-channel attacks, including the-state-of-the-art side-channel attacks and circuit-level countermeasures.

11:35 AM **13.6** Leveraging Circuit Reliability Effects for Designing Robust and Secure Physical Unclonable Functions (Invited)
Chris Kim, Minsu Kim, Gyusung Park, Po-wei Chiu, University of Minnesota

Reliability mechanisms are undesirable from a product lifetime viewpoint, but their unique characteristics can enable novel applications. In this invited paper, we will discuss how reliability mechanisms can be leveraged for various circuit applications, and present a novel SRAM PUF where metal fuses are utilized for improved stability.

12:00 PM **13.7** Custom CMOS and Post-CMOS Crossbar Circuits for Resource-Constrained Hardware Security Primitives (Invited)
Kaiyuan Yang, Rice University

Securing ubiquitous resource-constrained systems in emerging applications faces severe hardware constraints on power and costs. In this paper, we present a suite of hardware security primitives, exploring crossbar circuits in CMOS and post-CMOS process, to lay a reliable and energy-efficient foundation for system security.

Session 14 - Emerging Device and Compute Technology - Neuromorphic Session II-Architecture Focus
Tuesday, December 10, 9:00 a.m.
Continental Ballroom 5
Co-Chairs: S. Amrogio, IBM Research
J. Deng, Qualcomm

9:05 AM **14.1** Programmable Linear RAM: A New Flash Memory-based Memristor for Artificial Synapses and Its Application to Speech Recognition System
Shifan Gao, Guangjun Yang, Xiang Qiu, Chun Yang, Cheng Zhang, Binhan Li, Chao Gao, Hong Jiang, Zhexian Wang, Jian Hu, Jun Xiao, Bo Zhang, Choong-Hyun Lee, Yi Zhao, Weiran Kong, , Shanghai Huahong Grace Semiconductor Manufacturing Corporation, Flash Billion Semiconductor Co. Ltd, Peking University

In this work, a new type of flash memory-based memristor, named programmable linear random-access memory (PLRAM), is presented to store analog synaptic weights in a single Flash memory cell. With a linearity-aware design, an application of speech recognition is presented, with recognition accuracy higher than 90%.

9:30 AM **14.2** On-Chip Trainable 1.4M 6T2R PCM Synaptic Array with 1.6K Stochastic LIF Neurons for Spiking RBM
Masatoshi Ishii, SangBum Kim, Seoul National University, Scott Lewis, Atsuya Okazaki, Junka Okazawa, Megumi Ito, Malte J. Rasch, Wanki Kim, Akiyo Nomura, Uicheol Shin, Seoul National University, Kohji Hosokawa, Matthew BrightSky, Wilfried Haensch, IBM Research, Seoul National University, IBM Research - Tokyo,

Scalable six-transistor/two analog-weighted PCM resistor (6T2R) cell array integrating with fully-parallelized asynchronous stochastic leaky integrated-and-fire (LIF) neuron circuit demonstrated ultra low-

power (8.95 pJ per synaptic operation) on-chip training and inference capabilities of restricted Boltzmann machine (RBM) using MNIST hand-written digit database.

9:55 AM **14.3** Fully Integrated Spiking Neural Network with Analog Neurons and RRAM Synapses
Alexandre Valentian, François Rummens, Elisa Vianello, Thomas Mesquida, Capucine Lecat-Mathieu de Boissac, Olivier Bichler, Carlo Reita, CEA-Leti, CEA-List,

This paper presents, to the best of the authors' knowledge, the first complete integration of a Spiking Neural Network, combining analog spiking neurons and RRAM-based synapses. The test chip, fabricated in 130nm CMOS, shows well-controlled integration of synaptic currents and a high RRAM endurance to inference tasks (750M spikes sent).

10:20 AM **14.4** A Deep Neural Network Accelerator Based on Tiled RRAM Architecture
Xinxin Wang, Seung hwan Lee, Fan-Hsuan Meng, Wei D. Lu, University of Michigan

Deep neural networks have been successfully mapped on an RRAM-based tiled in-memory computing (IMC) architecture. Effects of array size and quantized partial products (PPs) due to ADC precision constraints were analyzed. Methods were developed to solve these challenges and preserve DNN accuracies and IMC performance gains in the tiled architecture.

11:10 AM **14.5** On Designing Efficient and Reliable Nonvolatile Memory-Based Computing-In-Memory Accelerators (Invited)
Bonan Yang, Mengyun Liu, Yiran Chen, Krishnendu Chakrabarty, and Hai Li Duke University

11:35 AM **14.6** Bayesian Neural Network Realization by Exploiting Inherent Stochastic Behavior of Analog RRAM
Yudeng Lin, Qingtian Zhang, Jianshi Tang, Bin Gao, Chongxuan Li, Peng Yao, Zhengwu Liu, Jun Zhu, Jiwu Lu, Hunan University, Xiaobo Shraon Hu, University of Notre Dame, He Qian, Huaqiang Wu, Tsinghua University

For the first time, this paper develops a novel stochastic computing method by utilizing the inherent random noises of analog RRAM. The RRAM device can realize the function of sampling from a tunable probabilistic distribution required by BayNN. And this is the first demonstration work for BayNN with emerging devices.

12:00 PM **14.7** An Analog Neuro-Optimizer with Adaptable Annealing Based on 64×64 0T1R Crossbar Circuit
Mohammad Reza Mahmoodi, Hyungjin Kim, Zahra Fahimi, Hussein Nili, Leo Sedov, Valentin Polishchuk, Dmitri Strukov, University of California, Santa Barbara, Linkoping University

We demonstrate an analog neuro-optimization hardware, which supports various annealing techniques, using a crossbar circuit with 4096 passively-integrated analog-grade memristors. The hardware operation is successfully tested by experimentally solving weighted graph partitioning, maximum clique, vertex cover, and independent set problems, and observing good agreement with simulation results.

12:25:00 PM **14.8** A High-Speed and High-Reliability TRNG Based on Analog RRAM for IoT Security Application
Bohan Lin, Bin Gao, Yachuan Pang, Peng Yao, Dong Wu, Hu He, Jianshi Tang, He Qian, Huaqiang Wu, Tsinghua University

A novel True Random Number Generator (TRNG) based on analog RRAM is developed. The highest single-cell throughput >1 Mbit/sec is achieved among RRAM-based TRNGs with minimal circuit overhead. The TRNG performance shows excellent temperature stability, and the RRAM endurance issue is greatly relieved to meet the requirement for IoT application.

Session 15 - Memory Technology - Ferroelectrics
Tuesday, December 10, 9:00 a.m.
Continental Ballroom 6
Co-Chairs: J. van Houdt, imec/KU Leuven
M. Kobayashi, University of Tokyo

9:05 AM **15.1** Material Perspectives of HfO2-based Ferroelectric Films for Device Applications
Akira Toriumi, Lun Xu, Yuki Mori, Xuan Tian, Patrick Lomenzo, Halid Mulaosmanovic, Monica Materano, Thomas Mikolajick, Uwe Schroeder, The University of Tokyo, NaMLab/TU-Dresden

This paper gives material fundamentals and new insights to ferroelectric HfO2 for device applications. The key role of dopants, effects of the interface on ferroelectric phase, and a detailed discussion of switching kinetics are of central focus. Based on them, we discuss opportunities of ferroelectric HfO_2 for device applications.

9:30 AM **15.2** First Direct Measurement of Sub-Nanosecond Polarization Switching in Ferroelectric Hafnium Zirconium Oxide
Xiao Lyu, Mengwei Si, Pragya Shrestha, Kin Cheung, Peide Ye, Purdue University, National Institute of Standards and Technology

We report on an ultrafast direct measurement on the transient ferroelectric polarization switching in hafnium zirconium oxide with metal-insulator-metal structures. A record low sub-nanosecond characteristic switching time of 925 ps was achieved. The impact of electric field, film thickness and device area on the polarization switching speed is systematically studied.

9:55 AM **15.3** 3D Scalable, Wake-up Free, and Highly Reliable FRAM Technology with Stress-Engineered HfZrOx
Yu-De Lin, Heng-Yuan Lee, Ying-Tsan Tang, Po-Chun Yeh, Hsin-Yun Yang, Po-Shao Yeh, Chih-Yao Wang, Jian-Wei Su, Sih-Han Li, Shyh-Shyuan Sheu, Tuo-Hung Hou, Wei-Chung Lo, Min-Hung Lee, Meng-Fan Chang, Ya-Chin King, Chrong-Jung Lin, Taiwan Semiconductor Research Institute, Industrial Technology Research Institute, National Chiao Tung University, National Taiwan Normal University, National Tsing Hua University, National Tsing Hua University

The major challenge in FRAM scaling is to maintain the high polarization density on the vertical sidewall of 3D-ferroelectric capacitors. We achieved a 3D-sidewall FRAM with high reliability of 10^9 endurance, 10-year retention and sidewall P_r 18μC/cm^2 . Two simple methods are contributed to the scaling capability of 3D-FRAM in 3X-nm.

10:20 AM *COFFEE BREAK*

10:45 AM **15.4** Impact of Homogeneously Dispersed Al Nanoclusters by Si-monolayer Insertion into Hf0.5Zr0.5O2 Film on FeFET Memory Array with Tight Threshold Voltage Distribution
Keiichi Maekawa, Tadashi Yamaguchi, Takahiro Ohara, Atsushi Amo, Eiji Tsukuda, Kenichiro Sonoda, Hiroshi Yanagita, Masao Inoue, Masazumi Matsuura, Tomohiro Yamashita, Renesas Electronics Corporation

Threshold voltage variation for ferroelectric field-effect transistor memory using $Hf^{0.5}Zr^{0.5}O_2$ films with Al nanoclusters is investigated. Si-monolayer formed over Al nanoclusters effectively reduces the variation, due to suppressing the migration and aggregation of Al nanoclusters, resulting that the orientation and the growth rate for each ferroelectric domain is successfully aligned.

11:10 AM **15.5** Next Generation Ferroelectric Memories enabled by Hafnium Oxide (Invited)
Thomas Mikolajick, Uwe Schroeder, Patrick Lomenzo, Evelyn Breyer, Halid Mulaosmanovic, Michael Hoffmann, Terence Mittmann, Furqan Mehmood, Benjamin Max, Stefan Slesazeck, NaMLab gGmbH, Technische Universtität Dresden

Ferroelectrics are an ideal solution for low write power nonvolatile memories. The complexity of ferroelectric perovskites has hindered the scaling. Ferroelectricity in hafnium oxide solved this issue making ferroelectric memories in its three variants, ferroelectric RAM, ferroelectric field effect transistors and ferroelectric tunneling junctions interesting for future memory solutions again.

11:35 AM **15.6** Impact of Charge trapping on Imprint and its Recovery in HfO_2 based FeFET
Yusuke Higashi, Nicolò Ronchi, Ben Kaczer, Kaustuv Banerjee, Sean McMitchell, Barry O'Sullivan, Sergiu Clima, Albert Minj, Umberto Celano, Luca DiPiazza, Masamichi Suzuki, Dimitri Linten, Jan Van Houdt, Toshiba Memory Corporation, imec, imec/KU Leuven

For ferroelectric-HfO_2 based FET (FeFET), imprint has been regarded as a major issue. However, most studies have been conducted only on capacitors. In this paper, imprint of FeFET as well as simulation of charge trapping is reported. The strong effect of charge trapping is responsible for imprint and its recovery.

12:00 PM **15.7** Demonstration of BEOL-Compatible Ferroelectric Scaled Hf0.5Zr0.5O2 FeRAM Co-Integrated with 130nm CMOS for Embedded NVM Applications
Terry Francois, Laurent Grenouillet, Jean Coignus, Philippe Blaise, Catherine Carabasse, Nicolas Vaxelaire, Thomas Magis, François Aussenac, Virginie Loup, Catherine Pellissier, Stefan Slesazeck, Viktor Havel, Claudia Richter, Adam Makosiej, Bastien Giraud, Evelyn Breyer, Monica Materano, Philippe Chiquet, Aix-Marseille Université, Marc Bocquet, Aix-Marseille Université, Etienne Nowak, Uwe Schroeder, Fred Gaillard, CEA-Leti, NaMLab gGmbH,

We demonstrate scalability of HZO capacitors down to 300nm by co-integrating them for the first time in Back-End-Of-Line of 130nm CMOS technology. Excellent performance are reported: $2.P_R$ >40µC/cm², endurance $>10^{11}$, switching speeds <100ns, operating voltages <4V, and data retention at 125°C paving the way towards <10fJ/bit ultra-low power FeRAM for IoT applications.

Session 16 - Optoelectronics, Displays, and Imagers - Image Sensors
Tuesday, December 10, 9:00 a.m.
Continental Ballroom 7-9
Co-Chairs: A. Tournier, STMicroelectronics
P. Malinowski, imec

9:05 AM **16.1** Nanophotonics contributions to state-of-the-art CMOS Image Sensors (Invited)
Sozo Yokogawa, Sony Semiconductor Solutions Corporation

Recent progress of Back-illuminated CMOS image sensors (BI-CISs), focusing on their pixel improvements with the design of optical properties using subwavelength sizescale strcutures and photonics technologies, are reviewed. These technologies contribute not only improving BI-CIS basic performance but also adding new functions for versatile sensing applications.

9:30 AM **16.2** A 0.8 µm Smart Dual Conversion Gain Pixel for 64 Megapixels CMOS Image Sensor with 12k e- Full-Well Capacitance and Low Dark Noise
Donghyuk Park, Seung-Wook Lee, Jinhwa Han, Dongyoung Jang, Heesang Kwon, Seungwon Cha, Mihye Kim, Haewon Lee, Sungho Suh, Woong Joo, Yunki Lee, Seungjoo Nah, Heegeun Jeong, Bumsuk Kim, Sangil Jung, Jesuk Lee, Yitae Kim, Chang-Rok Moon, Yongin Park, Samsung Electronics

A 0.8 µm-pitch 64 megapixels CIS has been demonstrated for the first time. 6k e- full-well capacity (FWC) was achieved, and the advanced color filter isolation was introduced. Dual conversion gain enhanced the Tetracell FWC to 12k e-. Highly refined deep trench isolation and photodiode also improved dark noise characteristics.

9:55 AM **16.3** A 1/2inch 48M All PDAF CMOS Image Sensor Using 0.8µm Quad Bayer Coding 2×2OCL with 1.0lux Minimum AF Illuminance Level
Tatsuya Okawa, Susumu Ooki, Hiroaki Yamajo, Masakazu Kawada, Masayuki Tachi, Kazuhiro Goi, Takatsugu Yamasaki, Hiroki Iwashita, Sony Semiconductor manufacturing Corporation, Masahiko Nakamizo, Takayuki Ogasahara, Yoshiaki Kitano, Keiji Tatani, Sony Semiconductor Solutions Corporation, Sony Semiconductor Manufacturing Corporation

We created the world's first all PDAF CMOS image sensor using 2x2 on-chip lens architecture. That had 1/2 inch 48M pixels with 0.8µm Quad Bayer coding for high resolution and HDR function, and all PDAF pixels achieved a minimum AF illuminance level of 1 lux.

10:20 AM **16.4** A 2.2µm Stacked Back Side Illuminated Voltage Domain Global Shutter CMOS Image Sensor
Geunsook Park, Alan Hsiung, Keiji Mabuchi, Jingming Yao, Zhiqiang Lin, Vincent Venezia, Tongtong Yu, Yu-Shen Yang, Tiejun Dai, Lindsay Grant, OmniVision

This paper introduces a 2.2µm stacked BSI voltage domain global shutter CMOS image sensor displaying over 100dB shutter efficiency, as well as high NIR-QE of 38% at 940nm, 60% MTF Ny/2 at 940nm with stacked pixel level connections, high density MIM capacitors, and Full back-side Deep Trench Isolations.

11:10 AM **16.5** A Highly Reliable Back Side Illuminated Pixel against Plasma Induced Damage
Yolene Sacchettini, Jean-Pierre Carrère, Célestin Doyen, Stéphane Ricq, Romain Duru, Vincent Goiffon, Pierre Magnan, Kristell Courouble, STMicroelectronics / ISAE-Supaero, STMicroelectronics, Univ. of Toulouse

Plasma process interaction with BSI image sensor is for the first time presented. The backside dielectrics properties modulate the damage, this was characterized by measuring the dielectrics charge and the interface state density. Metal oxides present a better hardiness to plasma damage due to their negative charge even after plasma.

11:35 AM **16.6** Three-layer Stacked Color Image Sensor With 2.0-µm Pixel Size Using Organic Photoconductive Film
Togashi Hideaki, Sony Semiconductor Solutions Corporation

A three-layer stacked color image sensor was formed using an organic film. The sensor decreases the false-color problem as it dose not require demosaicing. Furthermore, with the 2.0-µm pixel image sensor, improved spectral characteristics owing to green adsorption by the organic film above the red/blue photodiode, were successfully demonstrated.

12:00 PM **16.7** High-definition Visible-SWIR InGaAs Image Sensor using Cu-Cu Bonding of III-V to Silicon Wafer
Shuji Manda, Sony Semiconductor Solutions Corporation

We developed a back-illuminated InGaAs image sensor with 1280 x 1040 pixels at 5-um pitch by using Cu-Cu hybridization connecting different materials, a III-V InGaAs/InP of photodiode array, and a silicon readout integrated circuit (ROIC). A prototype device showed high sensitivity at visible to SWIR wavelengths and low dark current.

Session 17 - Microwave, Millimeter Wave and Analog Technology - III-Nitride Devices and Co-Integration
Tuesday, December 10, 9:00 a.m.
Imperial Ballrom A
Co-Chairs: D. Meyer, Naval Research
N. Collaert, imec

9:05 AM **17.1** Deep Submicron III-N HEMTs – Technological Development and Reliability (Invited)
Ruediger Quay, Michael Dammann, Peter Brückner, Maciej Cwiklinski, Dirk Schwantuschke, Sebastian Krause, Stefano Leone, Fraunhofer IAF

This paper gives the state-of-the-art of the technological development and the reliability status of deep-submicron Gallium Nitride high electron mobility transistors with gate lengths of 100 nm or below. Several epitaxial and process options are given. Promising GaN MMIC results are also provided leading to G-band operation near 200 GHz.

9:30 AM **17.2** CMOS-compatible GaN-based devices on 200mm-Si for RF applications: Integration and Performance
Uthayasankaran Peralagu, AliReza Alian, Vamsi Putcha, Ahmad Khaled, Raul Rodriguez, Arturo Sibaya-Hernandez, Shane Chang, Eddy Simoen, imec/KU Leuven, Simeng Zhao, Brice De Jaeger, Daniel Fleetwood, Piet Wambacq, Ming Zhao, Bertrand Parvais, Niamh Waldron, Nadine Collaert, imec, imec/KU Leuven/National Chiao Tung, Vanderbilt University, imec/Vrije Universteit Brussels

We report on the integration, and optimization of Al(Ga,In)N HEMTs, MISHEMTs and MOSFETs on 200-mm Si wafers using Au-free, CMOS compatible processing, and discuss performance tradeoffs, limitations and solutions. We show that MISHEMTs have the potential to outperform the other device types in terms of device scalability for high-frequency operation.

9:55 AM **17.3** 3D Heterogeneous Integration of High Performance High-K Metal Gate GaN NMOS and Si PMOS Transistors on 300mm High-Resistivity Si Substrate for Energy-Efficient and Compact Power Delivery, RF 95G and beyond) and SoC Applications
Han Wui Then, Sansaptak Dasgupta, Marko Radosavljevic, Pavel Agababov, Ibrahim Ban, Robert Bristol, Manish Chandhok, Siddharth Chouksey, Brandon Holybee, Cheng-Ying Huang, Brian Krist, Kimin Jun, Kevin Lin, Nidhi Nidhi, Thoe Michaelos, Brennen Mueller, Rajat Paul, Jason Peck, Willy Rachmady, David Staines, Tushar Talukdar, Nicole Thomas, Tristan Tronic, Paul Fischer, Intel Corporation

We demonstrate industry’s first 300mm 3D heterogeneous integration of high-performance, low-leakage high-K dielectric enhancement-mode GaN-NMOS and Si-PMOS transistors on high-resistivity 300mm-Si(111) substrate, enabled by 300mm GaN MOCVD-epitaxy and 3D layer-transfer, for integration of energy-efficient, compact power-delivery and RF solutions with CMOS circuitries for next-generation power-delivery, RF (5G&beyond) and SoC applications.

10:20 AM *COFFEE BREAK*

10:45 AM **17.4** High-Power-Density AlGaN/GaN Technology for 100-V Operation at L-Band Frequencies
Sebastian Krause, Peter Brückner, Michael Dammann, Ruediger Quay, Fraunhofer IAF

This paper reports on the development of a 0.5 µm AlGaN/GaN on SiC HEMT technology for operation at bias levels of 100 V. Load Pull measurements reveal a power density of more than 17 W/mm and a power-added efficiency in excess of 77 % at 1.0 GHz and 100 V.

11:10 AM **17.5** GaN-based Periodic High-Q RF Acoustic Resonator with Integrated HEMT, Vikrant Gokhale
Brian Downey, D. Scott Katzer, Laura Ruppalt, David Meyer, US Naval Research Laboratory

This work demonstrates the first on-chip integration of a high overtone bulk acoustic resonator (HBAR) with a HEMT using an epitaxial AlGaN/GaN/NbN/SiC heterostructure. This pairing combines the robust structure, periodic mode spacing, high mode density, and high – Q- of the HBAR with the amplification and non-reciprocal characteristics of the HEMT.

11:35 AM **17.6** 452 MHz Bandwidth, High Rejection 5.6 GHz UNII XBAW Coexistence Filters Using Doped AlN-on-Silicon
Jeffrey Shealy, Ya Shen, Pinal Patel, Ramakrishna Vetury, Akoustis Technologies, Inc

5.66GHz XBAW filters, utilizing doped AlN, are reported. The filters exhibit high -3dB bandwidth of 452MHz, a minimum insertion loss of 1.79dB, >50dB rejection and power handling up to 32.5dBm. Resonators show k^2 eff of 10.24%, Qmax of 1479, and FOM of 151 at 5.4GHz.

Sensors, MEMS and BioElectronics - Biomedical Sensors and Neural Interfaces
Tuesday, December 10, 9:00 a.m.
Imperial Ballroom B
Co-Chairs: G. Xu, University of Massachusetts, Amherst
S. Zafar, IBM T.J. Watson Research Center

9:05 AM **18.1** Minimally Invasive Medical Catheter with Highly Flexible FDSOI-based Integrated Circuits
Seung-Yoon Kim, Jae Hoon Bong, Mi Kyung Kim, Wansik Hwang, Hyunjoo Lee, Byeong-Wook Song, Il-Kwon Kim, Byung Jin Cho, KAIST, Korea Aerospace University, International St. Mary's Hospital, Catholic Kwandong University

A highly flexible integrated circuit (IC) composed of sensors and amplifiers using high-performance fully depleted silicon-on-insulator (FDSOI) transistors is demonstrated for bio-medical applications. A catheter with a 1 mm diameter, equipped with this flexible IC, is fabricated and successfully demonstrated for minimally invasive medical instrument applications with good bio-compatibility.

9:30 AM **18.2** Highly Sensitive Silicon Slip Sensing Imager for Forceps Grippers Used under Low Friction Condition
Kanako Ando, Takafumi Yamamoto, Yusaku Maeda, Kyohei Terao, Fusao Shimokawa, Masao Fujiwara, Hidekuni Takao, Kagawa University, Takamatsu Red Cross Hospital

We are reporting the first silicon electron device for the realization of detection in slip of grasping by laparoscopic forceps under very low friction condition. Even under “zero-level” friction, slip of grasping object is detectable with the original algorithm inspired from the finger’s sense of slip.

9:55 AM **18.3** Neural Interfaces Based on Flexible Graphene Transistors: A New Tool for Electrophysiology (Invited)
Anton Guimerà, Eduard Masvidal-Codina, Xavi Illa, Miguel Dasilva, Andrea Bonaccini-Calia, Elisabet Prats-Alfonso, Javier Martínez-Aguilar, Jose De la Cruz, Ramon Garcia-Cortadella, Nathan Schaefer, Almudena Barbero, Philippe Godignon, Gemma Rius, Del Coro, Jessica Clement Hebert, Rob Wykes, Maria V. Sanchez-Vives, Rosa Villa, Antonio Garrido, Institut de Microelectrònica de Barcelona IMB-CNM (CSIC), Institut de Microelectrònica de Barcelona, IMB-CNM, Centro de Investigación Biomédica en Red en Bioingeniería, Biomateriales y Nanomedicina (CIBER-BBN), Institut d’Investigacions Biomèdiques August Pi i Sunyer (IDIBAPS), Catalan Institute of Nanoscience and Nanotechnology (ICN2), CSIC and The Barcelona Institute of Science and Technology (BIST), 2Centro de Investigación Biomédica en Red en Bioingeniería, Biomateriales y Nanomedicina (CIBER-BBN), Institut de Microelectrònica de Barcelona, IMB-CNM (CSIC), UCL, Institute of Neurology, University College London

The use of graphene transistors for transducing neural activity has demonstrated the potential to extend the spatiotemporal resolution of electrophysiological methods to lower frequencies, providing a new tool to understand the role of the infra-slow activity.

10:20 AM **18.4** Design and Fabrication of CMOS-based Neural Probes for Large-scale Electrophysiology (Invited)
Carolina Mora Lopez, Alexandru Andrei, Shiwei Wang, Rita Van Hoof, Simone Severi, Nick Van Helleputte, imec

This paper describes the design and fabrication of the CMOS-based Neuropixels neural probe, which integrates a high-density micro-electrode array and a high channel count to enable large-scale electrophysiology in small rodents. Miniaturization and scalability aspects are also discussed here.

10:45 AM *COFFEE BREAK*

11:10 AM **18.5** Solution Processed Highly Uniform and Reliable Low Voltage Organic FETs and Facile Packaging for Handheld Multi-ion Sensing
Yukun Huang, Yawen Song, Yixiao Tang, Zhe Liu, Lei Han, Qiuqi Zhang, Bang Ouyang, Tang Wei, Linrun Feng, Xiaojun Guo, Shanghai Jiao Tong University, Wuhan LinkZill Technology Co., Ltd.

Organic FETs are fabricated over large area via high throughput coating, and present steep subthreshold, large ON/Off ratio, excellent uniformity and operational stability in all regimes. With a facile packaging approach to connect the device to external test environment, a handheld battery-powered multi-ion sensing system is demonstrated.

11:35 AM **18.6** BioFET Technology: Aggressively Scaled pMOS FinFET as Biosensor
Koen Martens, Sybren Santermans, Mihir Gupta, Geert Hellings, Robin Wuytens, Bert Du Bois, Emmanuel Dupuy, Efrain Altamirano Sanchez, Karolien Jans, Rita Vos, Tim Stakenborg, Liesbet Lagae, Marc Heyns, Simone Severi, Wim Van Roy, imec, imec/KU Leuven

We report for the first time on a BioFET sensor using 10nm wide FinFETs built in a 300 mm pilot line. Median voltage referred 1/f noise is only ~500 $\mu V^2 \mu m^2 Hz$ (@1Hz). pH sensitivity for HfO_2 is near the Nernstian limit. Biomolecular transduction is demonstrated for DNA grafting and PNA-DNA hybridization.

12:00 PM **18.7** Nanopore Digital Counting of Amplicons for Ultrasensitive Electronic DNA Detection
Weihua Guan, Pennsylvania State University

We demonstrate the feasibility of using the single molecule sensing nanopore as a digital counter to enumerate the amplicons for ultrasensitive electronic nucleic acid analysis. The nanopore digital counting approach could capture the DNA replication dynamics and could be used in a qualitative test and in a quantitative test.

Career Luncheon
Tuesday, December 10, 12:25 - 2:10 PM
Grand Ballroom B

Speakers:

Ramune Nagisetty, *Sr. Principal Engineer and Director of Process-Product Integration, Intel Corporation*

Linda K. Somerville, *Ph.D., Corporate Vice President of Technology Strategy and Operations, Micron Technology, Inc.*

In this IEDM Career Luncheon, the IEDM Executive Committee invites student conference attendees, aspiring professionals, and the IEDM community at-large to join the industry veterans in a casual, buffet lunch setting to discuss topics related to their careers and their experience in the semiconductor industry. To facilitate this dialog, two distinguished members of the semiconductor community, Ms. Remune Nagisetty from Intel and Dr. Linda Somerville from Micron, will share their industrial perspectives on the future of the semiconductor industry. We encourage the audience to attend this luncheon and engage with the distinguished speakers as they seek answers to their career development questions and the overall semiconductor industry.

From Datacenters to Wearables: The Continuing Evolution of Moore's Law,

Ramune Nagisetty, Intel Corporation

This talk will discuss a range of inspiring new computing applications from the edge to the cloud, interweaving lessons learned from a career spanning high performance transistor technology development to wearable system integration and the horizon of an emerging industry-scale ecosystem based on chiplets, heterogeneous integration, and advanced packaging.

A Passion for Technology: Memory and Macro Trends,

Linda K. Somerville, Micron Technology, Inc.

We are living in an exciting time, the A.I. revolution, in which the world is unleashing a massive amount of data. Looking back on a career in the memory industry interleaved with macro technology trends in the world, one can observe incremental change accented by such revolutionary inflection points. From there we can examine today’s technology trends and the importance of memory in the data economy.

Advanced Logic Technology - BEOL and 3D Packaging Innovation
Tuesday, December 10, 2:15 p.m.
Grand Ballroom A
Co-Chairs: H. Shang, TSMC
C. Liu, National Taiwan University

2:20 PM **19.1** Buried Power Rails and Back-side Power Grids: Arm® CPU Power Delivery Network Design Beyond 5nm
Divya Prasad, S. S. Teja Nibhanapudi, Shidhartha Das, Odysseas Zografos, Bilal Chehab, Satadru Sarkar, Rogier Baert, Alex Robinson, Alessio Spessot, Peter Debacker, Diederik Verkest, Jaydeep Kulkarni, Brian Cline, Saurabh Sinha, Arm Inc., The University of Texas at Austin, imec

An Arm CPU is designed with buried-power rails (BPR) and back-side power delivery at 3nm node. It is found that careful power-delivery-network design alleviates IR drop but deteriorates the energy with front side power delivery. However, back-side power delivery with BPR eliminates this trade-off demonstrating ~7X improvement in IR drop.

2:35 PM **19.2** Monolithic Heterogeneous Integration of BEOL Power Gating Transistors of Carbon Nanotube Networks with FEOL Si Ring Oscillator Circuits
Chao-Ching Cheng, Chun-Chieh Lu, Tsu-Ang Chao, Ang-Sheng Chou, Tianqi Gao, Jianwen Zhao, Zheng Cui, Hung-Li Chiang, Tzu-Chiang Chen, Lain-Jong Li, H.-S. Philip Wong, Taiwan Semiconductor Manufacturing Company, University of Science and Technology of China, Suzhou Institute of Nanotech and Nanobionics, Chinese Academy of Science

High-performance carbon-nanotube (CNT) network transistors are successfully integrated as BEOL power-gating devices onto Si CMOS wafers manufactured using 28-nm process technology. FEOL Si ring-oscillators with BEOL CNT header transistors achieve a similar quiescent current (I_{DDQ}) and comparable active power consumption as compared to the operation without the CNT header transistors.

3:10 PM **19.3** Three-Layer BEOL Process Integration with Supervia and Self-Aligned-Block Options for the 3 nm Node
Victor-Hugo Vega-Gonzalez, Christopher Wilson, Basoene Briggs, Stefan Decoster, J. J. Versluijs, ,Alicja Lesniewska, Sara Paolillo, Rogier Baert, Harinarayanan Puliyalil, Joost Bekaert, Els Kesters, Quoc Toan, Christophe Lorant, Olalla Varela Pedreira, Lieve Teugels, Nancy Heylen, Zaid El-Mekki, Marleen van der Veen, Tomas Webers, Hemant Vats, Luc Rijnders, Miroslav Cupak, Jae Uk Lee, Youssef Drissi, imec

The integration of a three-layer BEOL process with an intermediate 21 nm pitch level, relevant for the 3 nm node, is demonstrated using full barrier-less Ruthenium dual-damascene metallization. Variations of minimum island, via extension and tip-to-tip were electrically evaluated. Scaling boosters supervia and self-aligned block were investigated. Reliability study included.

3:35 PM *COFFEE BREAK*

4:00 PM **19.4** Heterogeneous Integration Using Omni-Directional Interconnect Packaging
Adel Elsherbini, Shawna Liff, Johanna Swan, Intel Corporation

We present a new packaging building block for 3D integrated circuits; Omni Directional Interconnect (ODI). It enables combining the high bandwidth benefit of 3D stacking with the minimal die area and direct

power delivery of 2D packaging. ODI performance and cost benefits are summarized and the fabrication results are presented.

4:25 PM **19.5** Integrated Deep Trench Capacitor in Si Interposer for CoWoS Heterogeneous Integration
S.Y. Hou, Harry Hsia, C.H. Tsai, K.C. Ting, T.H. Yu, Y.W. Lee, F.C. Chen, W.C. Chiou, C.T. Wang, C.H. Wu, Douglas C.H. Yu, TSMC

High-K based deep trench capacitors have been integrated the first time in the silicon interposer with TSV and fine-pitch interconnects for chip-on-wafer-on-substrate (CoWoS) integration. A specific capacitance density of 340 nF/mm2 is achieved over a large capacitor array, providing a total capacitance of 68 uF per interposer die.

4:50 PM **19.6** Foveros: 3D Integration and the use of Face-to-Face Chip Stacking for Logic Devices (Invited)
Doug Ingerly, Intel Corporation

Presents the key silicon features of Intel's 3D stacking technology, Foveros, as it is used to enable logic-on-logic die stacking. A robust face-to-face die connection is enabled with a high yielding, robust microbump connection. Additionally, we describe the TSVs used for connection to the package along with their electrical properties.

Power Devices and Systems - SiC Power Devices
Tuesday, December 10, 2:15 p.m.
Continental Ballroom 1-3
Co-Chairs: I. Kizilyalli, ARPA-E
D. Hisamoto, Hitachi

2:20 PM **20.1** Suppression of Bipolar Degradation in 4H-SiC Power Devices by Carrier Lifetime Control
H. Tsuchida, K. Murata, CRIEPI

Bipolar degradation phenomenon, in which the on-state forward voltage increases with the expansion of stacking faults, is a significant issue for practical applications of 4HSiC bipolar devices such as PiN diodes and IGBTs. This paper addresses methods realizing suppression of the degradation phenomenon by adopting carrier lifetime control techniques.

2:45 PM **20.2** Low Von 17kV SiC IGBT assisted n-MOS Thyristor
Shinichiro Matsunaga, Tomonori Mizushima, Kensuke Takenaka, Yuji Kiuchi, Akihiro Koyama, Yoshiyuki Yonezawa, Hajime Okumura, Fujielectric. Co., Ltd, National Institute of Advanced Industrial Science and Technology (AIST), New Japan Radio Co., Ltd., Mitsubishi Electric Corporation

The SiC n-MOS thyristor was designed and fabricated. The on-characteristics were improved over IGBTs fabricated under the same wafer conditions and process conditions. The MOS thyristor succeded in switching operation, and the switching speed of the MOS thyristor was equivalent to that of the IGBT in both turn-on and turn-off.

3:10 PM **20.3** Experimental Investigation and Improvement of Channel Mobility in 4H-SiC Trench MOSFETs

Katsuhiro Kutsuki, Eiji Kagoshima, Toru Onishi, Jun Saito, Narumasa Soejima, Yukihiko Watanabe, Toyota Central R&D Labs., Toyota Motor Corp.

The proposed method is used to evaluate the effect of the surface morphology of trench sidewalls on channel mobility in SiC trench MOSFETs for the first time. When the surface is atomically flat, there is a large increase in channel mobility. This is caused by the suppression of Coulomb scattering.

3:35 PM COFFEE BREAK

4:00 PM **20.4** Improvement in the Channel Performance and NBTI of SiC-MOSFETs by Oxygen Doping
Munetaka Noguchi, Toshiaki Iwamatsu, Hiroyuki Amishiro, Hiroshi Watanabe, Koji Kita, Naruhisa Miura, Mitsubishi Electric Corporation, The University of Tokyo

Si-face 4H-SiC MOSFETs with O-doped channel were demonstrated for the first time. The trade-off between specific on resistance and threshold voltage was improved especially in the high threshold voltage region. Furthermore, O-doping showed better performance for the NBTI characterization, being a promising approach to further improve the gate oxide reliability.

4:25 PM **20.5** Physical Modeling of Bias Temperature Instabilities in SiC MOSFETs
Christian Schleich, Judith Berens, Gerhard Rzepa, Gregor Pobegen, Gerald Rescher, Stanislav Tyaginov, Tibor Grasser, Michael Waltl, TU Vienna, kai, Global TCAD Solution, Infineon

The performance of SiC MOSFETs can still not be fully exploited due to defects in the atomic structure giving rise to BTI. We investigate BTI in lateral and vertical channel nMOSFETs. By doing physics based device simulations we extract defect bands which finally enables us to provide accurate lifetime extrapolations

Reliability of Systems and Devices - Emerging Transistor Reliability and Pertinent Strategies
Tuesday, December 10, 2:15 p.m.
Continental Ballroom 4
Co-Chairs: F. Schanovsky, Global TCAD Solutions BmbH
B. Weir, Broadcom

2:20 PM **21.1** Addressing Reliability Challenges in Advance Nodes for Commercial and Automotive Application (Invited)
Tanya Nigam, Peter Paliwoda, Xinggong Wan, Andreas Kerber, GLOBALFOUNDRIES, GLOBALFOUNDRIES Malta Pte. Ltd, Na

Building in reliability is critical during technology development, as we continue scaling or incorporating additional functionality. In this paper Front End Of Line methodologies for DC, Equivalent AC and correlation to RO/SRAM/Logic degradation and failure are presented. Additionally, Self-Heating and Variability characterization for commercial and automotive applications are discussed.

2:45 PM **21.2** A Physics-aware Compact Modeling Framework for Transistor Aging in the Entire Bias Space
Zhicheng Wu, Jacopo Franco, Philippe Roussel, Stanislav Tyaginov, Brecht Truijen, Michiel Vandemaele, Geert Hellings, Nadine Collaert, Guido Groeseneken, Dimitri Linten, Ben Kaczer, KU LEUVEN/IMEC, imec, imec/KU Leuven

A unified compact modeling framework of device aging is proposed and verified on FinFET technology

3:10 PM **21.3** Understanding and Physical Modeling Superior Hot-Carrier Reliability of Ge pNWFETs
Stanislav Tyaginov, Al-Moatasem El-Sayed, Alexander Makarov, Adrian Chasin, Hiroaki Arimura, Michiel Vandemaele, Markus Jech, Elena Capogreco, Liesbeth Witters, Alexander Grill, An De Keersgieter, Geert Eneman, Dimitri Linten, Ben Kaczer, imec, Nanolayers, TU Vienna

We accurately model degradation and the time-to-failure measured during hot-carrier stress in Ge and Si pNWFETs. The superior time-to-failure in Ge devices has been explained by a much higher energy (5.5eV) needed to break Ge-O bonds (precursors) and form O-vacancies (defects) compared to the Si-H bond rupture energy (2.6eV).

3:35 PM *COFFEE BREAK*

4:00 PM **21.4** New Insight into MOS Gate Stack Formations on Ge and SiGe from Thermodynamics
Reaction Kinetics and Nanoscale Engineering, Akira Toriumi, Tomonori Nishimura, The University of Tokyo

Oxidation and thermal robustness of gate stacks in Ge and SiGe are intensively investigated. The key points of new understanding are twofold. One is that GeO_2Ge interface reaction occurs inhomogeneously, and the other is that Si in SiGe is oxidized by GeO_2 and Ge agglomeration also occurs on SiGe surface.

4:25 PM **21.5** Novel Concept of the Transistor Variation Directed Toward the Circuit Implementation of Physical Unclonable Function (PUF) and True-random-number Generator (TRNG)
Y. Xiao, E. R. Hsieh, Steve Chung, T. P. Chen, S. A. Huang, T. J. Chen, Osbert Cheng, National Chiao Tung University, UMC

We use a unique feature of S/D variations of 14nm FinFET to realize PUF and TRNG. The S/D variation was used to design PUF. The defect generated traps was observed from a new Ib-RTN which was used to design TRNG. Reliability tests of array and circuits are presented.

4:50 PM **21.6** Physical Insights on Steep Slope FEFETs including Nucleation-Propagation and Charge Trapping
Yang Xiang, Marie Garcia Bardon, Md Nur Kutubul Alam, Mischa Thesberg, Ben Kaczer, Philippe Roussel, Mihaela Ioana Popovici, Lars-Ake Ragnarsson, Brecht Truijen, Anne S. Verhulst, Bertrand Parvais, Naoto Horiguchi, Guido Groeseneken, imec/KU Leuven,Jan Van Houdt imec, KU LEUVEN/IMEC, imec/KU Leuven, imec/Vrije Universteit Brussel, TU Wien

We present an analysis of steep slope FEFETs including statistical multidomain nucleation-propagation and high-K hafnia-oxide charge trapping, based on a compact model validated on transistor I-V measurement. The proposed field-independent propagation proves key to explaining the steep slope. Trapping is shown to assist polarization-switching and enlarge the detrimental I-V hysteresis

Memory Technology/Emerging Device and Compute Technology - Focus Session: Emerging AI Hardware
Tuesday, December 10, 2:15 p.m.
Continental Ballroom 5
Co-Chairs: C. Petti, Sunrise Memory, Inc.
T-H Hou, National Chiao Tung University

2:20 PM **22.1** Design Considerations for Efficient Deep Neural Networks on Processing-in-Memory Accelerators (Invited)
Tien-Ju Yang, Vivienne Sze, Massachusetts Institute of Technology

This paper describes various design considerations for deep neural networks that enable them to operate efficiently and accurately on processing-in-memory accelerators. We highlight important properties of these accelerators and the resulting design considerations using experiments conducted on various state-of-the-art deep neural networks with the large-scale ImageNet dataset.

2:45 PM **22.2** Towards 10000TOPS/W DNN Inference with Analog in-Memory Computing – A Circuit Blueprint, Device Options and Requirements (Invited)
Stefan Cosemans, Bram Verhoef, Jonas Doevenspeck, Ioannis Papistas, Francky Catthoor, Peter Debacker, Arindam Mallik, Diederik Verkest, imec, imec/KU Leuven

This paper presents a circuit blueprint for a 10000TOPS/W matrix-vector multiplier for neural network inference based on Analog in-Memory Computing, using pulse-width encoded activations and precharge-discharge summation lines. Three suited device options are discussed: SOT-MRAM, IGZO-based 2T1C DRAM gain cell, and projection PCM with separate write path.

3:10 PM **22.3** The Marriage of Training and Inference for Scaled Deep Learning Analog Hardware (Invited)
Tayfun Gokmen, Malte J. Rasch, Wilfried Haensch, IBM Research AI, IBM Research

Here, we show that for large scale deep neural networks (DNNs) the model's parameters (weights) must come from a training procedure that accounts for hardware induced constraints, such as ADC, DAC and noise, for the inference task to be successful when run on analog hardware composed of crossbar arrays.

3:35 PM **22.4** Can in-memory/Analog Accelerators be a Silver Bullet for Energy-efficient Inference? (Invited)
Jun Deguchi, Daisuke Miyashita, Asuka Maki, Sasaki, Kengo Nakata, Fumihiko Tachibana, Kioxia Corporation

Although energy efficiency of in-memory/analog accelerators looks better than that of digital accelerators based on our benchmark, accuracy of in-memory/analog accelerators is usually deteriorated. Then we introduce our proposed quantization technique and a specific hardware architecture. Finally, we discuss whether in-memory/analog accelerators can be a silver bullet for energy-efficient inference.

4:00 PM *COFFEE BREAK*

4:25 PM **22.5** AI Edge Devices Using Computing-In-Memory and Processing-In-Sensor: From System to Device (Invited)
Tzu-Hsiang Hsu, -Cheng Chiu, Wei-Chen Wei, Yun-Chen Lo, Chung-Chuan Lo, Ren-Shuo Liu, Kea-Tiong Tang, Meng-Fan Chang, Chih-Cheng Hsieh, National Tsing Hua University

This paper presents the advanced technologies, including CIS and PIS techniques, for low-power and low-latency AI edge devices. From system perspective, CIM and PIS techniques are effective by reducing power dissipation and data transmission for computations in CNN models. Furthermore, the performance is strongly relied on the corresponding device enhancement.

4:50 PM **22.6** Hybrid Analog-Digital Learning with Differential RRAM Synapses (Invited)
Tifenn Hirtzlin, Marc Bocquet, Maxence Ernoult, Jacques-Olivier Klein, Etienne Nowak, Elisa Vianello, Jean-Michel Portal, Damien Querlioz, Univ Paris-Sud, Aix-Marseille Université, CEA-Leti

Exploiting analog RRAM for learning is compelling, but raises important challenges. Here, we investigate a learning architecture, based on Binarized Neural Networks, which exploits the analog properties of hafnium-oxide RRAM, but avoids these challenges: it uses exclusively low-overhead digital CMOS, is highly resilient to device imperfections, and shows outstanding endurance.

5:15 PM **22.7** Active Memristor Neurons for Neuromorphic Computing (Invited)
Wei Yi, Kenneth K. Tsang, Stephen K. Lam, Xiwei Bai, Jack A. Crowell, Elias A. Flores, HRL Laboratories, LLC.

Memristors provide a new paradigm to realize biomimetic and scalable neuron and synapse neuromorphic computing primitives capable of efficiently emulating the rich dynamics of biological counterparts. Using VO_2 active memristors, we show that memristor neurons possess most of the known biological neuronal dynamics and all three classes of neuron excitability.

5:40 PM **22.8** Towards Large-Scale Photonic Neural-Network Accelerators (Invited)
Ryan Hamerly, Alex Sludds, Liane Bernstein, Mihika Prabhu, Charles Roques-Carmes, Jacques Carolan, Yoshihisa Yamamoto, Marin Soljacic, Dirk Englund, MIT, NTT Research Inc.

We review leading photonic AI platforms based on beamsplitter mesh networks, weight banks, and photoelectric multiplication. Theoretical performance advantages, as well as practical issues of chip area, input / output, and crosstalk, are considered. We address fundamental and near-term limitations to energy efficiency and investigate bandwidth limitations from temporal crosstalk.

Emerging Device and Compute Technology - Emerging Devices for Extending Moore's Law
Tuesday, December 10, 2:15 p.m.
Continental Ballroom 6
Co-Chairs: Y. Chai, The Hong Kong Polytechnic University
T. Mueller, Vienna University of Technology

2:20 PM **23.1** Importance of Interconnects: A Technology System-Level Design Perspective (Invited)
Jie Liang, Aida Todri-Sanial, LIRMM, University of Montpellier, CNRS

For CVD MoS_2 FETs we demonstrate that downscaling the top-contact length to 13nm induces no penalty on the characteristics, experimentally confirming edge injection with I_{on}=250µA/µm for 50nm SiO_2 gate oxide. This is equally valid for thinner 4nm HfO_2 gate oxide, where the switching characteristics improve with SS_{min}=80mV/dec

2:45 PM **23.2** Ultra-scaled MOCVD MoS2 MOSFETs with 42nm Contact Pitch and 250µA/µm Drain Current
Quentin Smets, Goutham Arutchelvan, Julien Jussot, Devin Verreck, Inge Asselberghs, Ankit Nalin Mehta, Abhinav Gaur, Dennis Lin, Salim El Kazzi, Benjamin Groven, Matty Caymax, Iuliana Radu, imec

For CVD MoS_2 FETs we demonstrate that downscaling the top-contact length to 13nm induces no penalty on the characteristics, experimentally confirming edge injection with I_{on}=250µA/µm for 50nm SiO_2 gate

oxide. This is equally valid for thinner 4nm HfO_2 gate oxide, where the switching characteristics improve with SS_{min}=80mV/dec

3:10 PM **23.3** Highly Area-Efficient Low-Power SRAM Cell with 2 Transistors and 2 Resistors
Peng Zhou, Jiayi Li, Jingyu Li, Yi Ding, Chunsen Liu, Xiang Hou, Huawei Chen, Yan Xiong, Yang Chai, David Wei Zhang, Fudan Unveristy, The Hong Kong Polytechnic University

We demonstrate a highly area-efficient 2-transistor/2-resistor static-random-access-memory cell with high read/write stability composed of novel two-surface-channel transistors, using two-dimensional layered MoS_2. The read and write power of the memory devices are 0.035 μW and 0.036 μW, respectively, indicating a promising application in low-power electronics and highly area-efficient chips.

3:35 PM **23.4** Area-Selective-CVD Technology Enabled Top-Gated and Scalable 2D-Heterojunction Transistors with Dynamically Tunable Schottky Barrier
Chao-Hui Yeh, Wei Cao, Arnab Pal, Kamyar Parto, Kaustav Banerjee, University of California Santa Barbara

In this work, graphene source/drain heterojuction 2D FETs enabled by area-selective-CVD technology are demonstrated, in terms of reducing the contact and series resistances. Record-high ON-current (~273 μA/μm) and ultra-low contact resistance (~670 ohm·μm) are achieved in a monolayer 2D-FET. Scaling analysis confirms the sub-10 nm prospect of this device.

4:00 PM *COFFEE BREAK*

4:25 PM **23.5** Transient Negative Capacitance of Silicon-doped HfO2 in MFMIS and MFIS Structures: Experimental Insights for Hysteresis-free Steep Slope NC FETs
Carlotta Gastaldi, Ali Saeidi, Matteo Cavallieri, Igor Stolichnov, Paul Muralt, Adrian Ionescu, EPFL

We experimentally explore the transient negative capacitance effect in ferroelectric high-k gate stacks using multi-ferroelectric domain Si:HFO2 with and without metal plane. We demonstrate that despite the smaller gain, the MFIS structure provides hysteresis-free stable performance boosting in all the regimes of operation of a 14nm UTB SOI MOSFET.

4:50 PM **23.6** Bi-directional Sub-60mV/dec, Hysteresis-Free, Reducing Onset Voltage and High Speed Response of Ferroelectric-AntiFerroelectric Hf0.25Zr0.75O2 Negative Capacitance FETs
Min-Hung Lee, Kuan-Ting Chen, Chun-Yu Liao, Guo-Yu Siang, Chieh Lo, Hong-Yu Chen, Yi-Ju Tseng, Chung-Yu Chueh, Ching Chang, Yen-Yun Lin, Yu-Jun Yang, Fu-Jhu Hsieh, Shu-Tong Chang, Ming-Han Liao, Kai-Shin Li, Chee Wee Liu, National Taiwan Normal University, National Taiwan University, National Chung Hsing University, Taiwan Semiconductor Research Institute (SS_{for}=51mV/dec, SS_{rev}=53mV/dec, ΔV_T<1mV)

First demonstration of quasi-antiferroelertic $Hf_{0.25}Zr_{0.75}O_2$ (QAFE-HZO) NC-FET with non-hysteretic bi-directional sub-60mV/dec (SS_{for}=51mV/dec, SS_{rev}53mV/dec, ΔV_T1mV) for low onset voltage, N-DIBL, NDR, and high speed response. An operation window for non-hysteretic steep SS of QAFE-HZO as compared with accompanying a non-negligible hysteresis of FE-HZO(Zr=50%). NC time is improved 48-77% from transient response.

5:15 PM **23.7** Direct Observation of Interface Charge Behaviors in FeFET by Quasi-Static Split C-V and Hall Techniques: Revealing FeFET Operation
Kasidit Toprasertpong, Mitsuru Takenaka, Shinichi Takagi, The University of Tokyo

Quasi-static split C-V is proposed as a novel method to monitor polarization and charge distribution in FeFETs. Our method, extracting Q-V_g loops directly from FeFET structures, is a powerful tool to understand the real operation and device physics of FeFETs including the memory window and the NC effect.

Modeling and Simulation - Ab Initio Simulation of Materials, Devices, and Interconnects
Tuesday, December 10, 2:15 p.m.
Continental Ballroom 7-9
Co-Chairs: B. Magyari-Kope, TSMC
V. Georgiev, University of Glasgow

2:20 PM **24.1** First-Principles Parameter-Free Modeling of n- and p-FET Hot-Carrier Degradation
Markus Jech, Stanislav Tyaginov, Ben Kaczer, Jacopo Franco, Dominic Jabs, Christoph Jungemann, Michael Waltl, Tibor Grasser, TU Vienna, TU Wien, imec/KU Leuven, imec, RWTH Aachen University

We present and validate a quantum chemistry approach to capture the intricate nature of hot-carrier degradation, which is essentially free of fit parameters. The newly identified resonance scattering mechanism allows us to clearly reveal the differences between degradation in n- and p-channel devices.

2:45 PM **24.2** Computational Study of Spin Injection in 2D Materials, Arnab Pal, Kamyar Parto Kunjesh Agashiwala, Wei Cao, Kaustav Banerjee, University of California Santa Barbara

This work presents the first comprehensive study of spin-injection into 2D materials using ab-initio Density Functional Theory simulations coupled with Non-Equilibrium-Greens-Function formalism, for applications in both spintronics and Magnetic Tunnel Junctions. Our rigorous modeling and simulation framework provide important insights into the relatively unexplored phenomenon of spin-injection into 2D-material systems.

3:10 PM **24.3** Ab initio Simulation of Advanced Materials and Devices: Current Challenges (Invited)
Philippe Blaise, Silvaco Europe

By integrating atomistic tools into the catalogues of TCAD solution providers, simulation is going to take the next step. First, we describe the most promising strategy of atomistic tools usage. Then, we open up new perspectives due to the strong link between electronic devices variability and atomistic modeling.

3:35 PM *COFFEE BREAK*

4:00 PM **24.4** Ab initio Mobility of Single-layer MoS2 and WS2: Comparison to Experiments and Impact on the Device Characteristics
Youseung Lee, Sara Fiore, Mathieu Luisier, ETH-Zurich

We combine the linearized Boltzmann Transport Equation and quantum transport by means of the Non-equilibrium Green's Functions to simulate monolayer MoS_2 and WS_2 ultra-scaled transistors with carrier mobilities extracted from experiments. Electron-phonon, charged impurity, and surface optical phonon scattering are taken into account from ab initio calculations or measurements.

4:25 PM **24.5** Piezoelectric Hetero-junction Tunnel FET with Staggered Gap at off-state and Broken Gap at on-state
Yuxiong Long, Hong-Yu Wen, Shenyuan Yang, Huang, Xiangwei Jiang, Institute of Semiconductors, Chinese Academy of Sciences, MaxLinear Inc.

A novel GaSb/InAs piezoelectric hetero-junction tunnel-FET (PE-H-TFET) which changes band-gap type during switching is proposed, i.e. staggered-gap at OFF-state while broken-gap at ON-state. Numerical simulation suggests that the PE-H-TFET achieves 1.76 times enhancement of I_{ON} and a steep SS of 42 mV/decade. The source overlap obtains 2.5 times I_{ON} enhancement.

4:50 PM **24.6** Large-scale ab initio Quantum Transport Simulation of Nanosized Copper Interconnects: the Effects of Defects and Quantum Interferences
Meng Ye, Xiangwei Jiang, Shu-Shen Li, Lin-Wang Wang, Institute of Semiconductors, Chinese Academy of Sciences, Lawrence Berkeley National Laboratory

A fully ab initio quantum transport simulation of nano-interconnect containing record number of atoms (~5000) is presented for the first time. Various imperfections of the nanosized Cu interconnects are thoroughly investigated. It is suggested that classical description, e.g. Matthiessen's rule, is not valid at nanoscale, due to quantum interference.

Microwave, Millimeter Wave, and Analog Technology - Advanced Si and Packaging Technologies for 5G and Beyond
Tuesday, December 10, 2:15 p.m.
Imperial Ballroom A
Co-Chairs: Y. Sun, IBM
D. Belot, CEA-Leti

2:20 PM **25.1** RF Performance of a Fully Integrated 3D Sequential Technology
Xavier Garros, José Lugo, Laurent Brunet, Riadh Nait Youcef, Perrine Batude, Claire Fenouillet-Beranger, Mikaël Cassé, Benoit Sklenard, Pascal Scheiblin, Joris Lacord, Konstantinos Triantopoulos, François Andrieu, Gerard Ghibaudo, Fred Gaillard, IMEP-LAHC

RF performance of a fully integrated CMOS 3D Sequential Integration is deeply investigated. We highlight that Top Tier PMOS processed at 630°C can feature good RF Figure-Of-Merits with F_t =55GHz and F_{max}=80GHz at V_{DD}=-1V. An improved low temperature process (T<530°C) able to boost this RF performance is also proposed.

2:45 PM **25.2** Record High-performance RF Devices in an Advanced FDSOI Process Enabling Integrated Watt-level Power Amplifiers for WiFi and 5G applications
Thanh Viet Dinh, Bart Hovens, Marina Vroubel, Ihor Brunets, Hans Tuinhout, Luuk Tiemeijer, Nicole Wils, Guido Sasse, Paul Grudowski, Matthias Raucoules-Aime, Stefano Dal Toso, Carla Ghidini, NXP Semiconductors

A Watt-level power amplifier for both WiFi (5GHz) and 5G (28GHz) in sub-28nm FDSOI is enabled by a record high-performance of 3.3V / 5V RF-LDMOS (fT ~ 115GHz) and passive devices including 7V fringe capacitors (Q-factor > 100 at 28GHz and ~ 340 at 5GHz), 2-way transformers and 8-shaped inductors.

3:10 PM **25.3** Fabrication and Characterization of Millimeter Wave 3D InFO Dipole Antenna Array Integrated with CMOS Front-end Circuits
Chung-Hao Tsai, Che-Wei Hsu, Kun-Yao Kao, Tzu-Chun Tang, Chun-Lin Lu, Max Wu, Han-Ping Pu, Kun-You Lin, Huei Wang, Tzong-Lin Wu, Chung-Shi Liu, C.T. Wang, C.H. Yu, Taiwan Semiconductor Manufacturing Company, Ltd., National Taiwan University

A high performance 3D dipole antenna with metal thickness >100 μm for wide bandwidth and lateral radiation is realized on InFO package. 25% wide FBW, 60-77 GHz, has been obtained. The beamforming capability of the system antenna array with 6 dBi gain is measured in 40nm CMOS RFIC co-designed system.

3:35 PM **25.4** Implementation of High Power RF Devices with Hybrid Workfunction and OxideThickness in 22nm Low-Power FinFET Technology
Hyung-Jin Lee, Saurabh Morarka, Said Rami, Yu, Guannan Liu, Mark Armstrong, Chen-yi Su, Dyan Ali, Bernhard Sell, Ying Zhang, Intel Corporation

Unique High-Power FinFET device with multiple workfunction materials and oxide thickness under a common gate, dubbed as HyPowerFF, is introduced. The proposed devices are as reliable as high-voltage IO devices with up to 7.1V of breakdown voltage and equip speedy 290 GHz of f_{MAX} suitable for power-efficient RF power-amplifier (PA) design.

4:00 PM *COFFEE BREAK*

4:25 PM **25.5** A Very Robust and Reliable 2.7GHz +31dBm Si RFSOI Transistor for Power Amplifier Solutions
Xavier Garros, Vincent Knopik, Nathalie Revil, Alexis Divay, Jacques Cluzel, José Lugo, Alexandre Giry, Xavier Federspiel, Guillaume Bertrand, Florian Cacho, Emmanuel Vincent, Eric Granger, Gaillard, ST Microelectronics

A robust and low cost Si RFSOI Power Transistor which deliver +31dBm output power with 74% of PAE and 18dB of Gain is optimized for 5G sub-6GHz Power Amplifier. It is proved that this great performance is achieved while maintaining a high level of reliability of the PA transistor.

4:50 PM **25.6** Is 5G the Killer App for SOI? (Invited)
Pietro Rabbeni, Anirban Bandyopadhyay, Shankaran Janardhanan, GlobalFoundries

5G promises to be as disruptive to wireless communications as data was to voice. Challenges however remain on radio architectures and what technologies will be used to solution them to drive lower cost, lower power and better efficiency. This presentation explores one of those solutions.

Sensors, MEMS, and Bioelectronics - Integrated Energy Devices and Sensors
Tuesday, December 10, 2:15 p.m.
Imperial Ballroom B
Co-Chairs: A. Tixier-Mita, University of Tokyo
X. Wang, Tsinghua University

2:20 PM **26.1** Millimeter Scale Thin Film Batteries for Integrated High Energy Density Storage
Sami Oukassi, Arnaud Bazin, Christophe Secouard, Isabelle Chevalier, Severine Poncet, Sylvain Poulet, Jean-Marc Boissel, Françoise Geffraye, Jean Brun, Raphaël Salot, CEA-Leti

We successfully fabricated miniaturized TFBs integrating 20µm thick positive electrode for the first time. Our devices exhibit the best performances, reaching diacharge capacity of 0.8mAh/cm². The fabrication process is viable for industrial large-scale production. our TFBs have strong potential as integrated energy storage units, in particular for medical applications.

2:45 PM **26.2** Beyond Electrolytic Capacitor: High Frequency On-chip Micro Supercapacitor with Large Capacitance Density
Sixing Xu, Fan Xia, Xiaohong Wang, Tsinghua University

We report on high-frequency micro supercapacitors (MSC) with ultra-high capacitance and chip integratability. Contributed by 3D mesoporous electrodes and novel MXene quantum dots, 9.7/34.2 times of areal/volume capacitance higher than commercial electrolytic capacitors are obtained. The MSC is used in low-pass filtering circuits, showing great advantage in circuit size reduction.

3:10 PM **26.3** Device Engineering for Diamond Quantum Sensors (Invited)
Mutsuko Hatano, Tokyo Institute of Technology

Nitrogen-Vacancy centers in diamond have superior physical properties at room temperature for quantum sensing. We will review the sensor materials, quantum control technology, and applications. The perfectly-aligned NV ensemble formed by CVD-growth can provide high sensitivity. For applications, we will introduce biological imaging, nano-scale NMR, and internal device sensing.

3:35 PM **26.4** Efficient Integration of Si FET-type Gas Sensors and Barometric Pressure Sensors on the Same Substrate
Dongkyu Jang, Gyuweon Jung, Yujeong Jeong, Yoonki Hong, Seongbin Hong, Wonjun Shin, Ki Soo Chang, Chan Bae Jeong, Byung-Gook Park, Jong-Ho Lee, Seoul National University/ Samsung Electronics, Seoul National University, Korea Basic Science Institute

We propose Si FET-type gas sensors and barometric sensors that can be efficiently integrated on the same substrate. The gas sensor has a localized micro-heater capable of heating up to 124ºC. The barometric sensor has a built-in temperature sensor that can simultaneously measure temperature and pressure.

4:00 PM *COFFEE BREAK*

4:25 PM **26.5** A Large-area Curved Pyroelectric Fingerprint Sensor
Jean-François Mainguet, Didier Gallaire, Audrey Martinent, Amélie Revaux, Mohammed Benwadih, Simon Charlot, Albert Breemen, Jan-Laurens van der Steen, Hylke Akkerman, Auke Kronemeijer, Gerwin Gelinck, Marina Pouet, Joël-Yann Fourre, Stefano Sinopoli, Umberto Emanuele, Lionel Fritsch, Judith Liu Jimenez, Johan Karlsson, Florian De Roose, Soeren Steudel, CEA, imec, Netherlands Organisation for Applied Scientific Research (TNO), Idemia, Bioage, Irlynx, Universidad Carlos III de Madrid, Autoliv

We show a thin, flexible and large 500 dpi fingerprint sensor providing better usability than existing sensors with a similar performance. A new process flow, using PVDF-TrFE capacitors on top of an IGZO TFT backplane on a flexible polyimide foil is implemented to create an active thermal fingerprint sensor.

4:50 PM **26.6** Ultrasensitive Flexible Strain Sensor based on Two-Dimensional InSe for Human Motion Surveillance

Li Chen, Dan Liang, Zhigen Yu, Sifan Li, Xuewei Feng, Bochang Li, Yesheng Li, Yongwei Zhang, Kah-Wee Ang, National University of Singapore, A*STAR IHPC

We firstly demonstrate a flexible InSe-based strain sensor for human motion surveillance. Our work reveals a highly tunable piezoresistive effect and low Young's modulus in InSe that is promising for realizing ultrasensitive human motion sensors, and the performance can be further enhanced via gating effect using a three-terminal device configuration.

Session 27 - PANEL SESSION
Tuesday, December 10, 8:00 p.m.

Memory Technology - Charge Based Memory and Emerging Memories
Wednesday, December 11, 9:00 a.m.
Grand Ballroom A
Co-Chairs: P. Kalavade, Intel
Y. Dong, Micron

9:05 AM **28.1** 3D Semicircular Flash Memory Cell: Novel Split-Gate Technology to Boost Bit Density
Makoto Fujiwara, Tetsu Morooka, Kioxia Corporation

Three-dimensional semicircular flash memory cells have been developed for the first time. Properly designed semicircular floating-gate cells achieve superior program/erase characteristics at much smaller cell size relative to circular charge-trap cells. The semicircular floating-gate cell is a promising candidate for higher memory density at a lower number of stacking layers.

9:30 AM **28.2** A Novel Double-Density Hemi-Cylindrical (HC) Structure to Produce More than Double Memory Density Enhancement for 3D NAND Flash
Hang-Ting Lue, Macronix

A novel hemi-cylindrical (HC) 3D NAND Flash is demonstrated. HC 3D NAND squeezes the gate-all-around (GAA) hole , followed by a slit cut to split the GAA device to produce ~ 2.6 times of memory density increase. Good 100K PE cycling endurance and post 10K-cycled 150C retention are demonstrated.

9:55 AM **28.3** Metal-Assisted Solid-Phase Crystallization Process for Vertical Monocrystalline Si Channel in 3D Flash Memory
Yuichiro Mitani, Kioxia Corporation

In order to improve the channel conductance of 3D flash memory cell, metal induced lateral crystallization (MILC) process has been applied to channel Si in a vertical memory holes and demonstrated superior device characteristics and those uniformities with maintaining memory performance and reliability.

10:20 AM **28.4** A Fully Integrated Low Voltage DRAM with Thermally Stable Gate-first High-k Metal Gate Process (Invited)
Sung Ho Jang, Junhee Lim, Joon Han, Juyeon Jang, Jaehyun Yeo, Chanmin Lee, Sungkweon Baek, Jaehoon Lee, Jong-Ho Lee, Satoru Yamada, Kyupil Lee, Semiconductor R&D Center, Samsung Electronics

A 35nm node 4Gbit LPDDR3 prototype with high-k metal gate (HKMG) peripheral transistors is implemented for the first time using processes that are fully compatible with those of conventional commercial DRAMs with poly/SiON (PSiON) transistors. This paper describes that the HKMG transistors in the peripheral circuits drastically reduce operating voltage.

10:45 AM **28.5** First Demonstration of Field-free SOT-MRAM with 0.35 ns Write Speed and 70 Thermal Stability under 400°C Thermal Tolerance by Canted SOT Structure and its Advanced Patterning/SOT Channel Technology

Hiroaki Honjo, Anh Nguyen Thi Van, Toshinari Watanabe, Takashi Nasuno, Chaoliang Zhang, Takaho Tanigawa, Sadahiko Miura, Hirofumi Inoue, Masaaki Niwa, Toru Yoshizuka, Yasuo Noguchi, Mitsuo Yasuhira, Akira Tamakoshi, Masanori Natsui, Yitao Ma, Hiroki Koike, Yu Takahashi, Kaito Furuya, Hui Shen, Shunsuke Fukami, Hideo Sato, Shoji Ikeda, Takahiro Hanyu, Hideo Ohno, Tohoku University

For the first time, we demonstrated field-free 55nm-SOT MRAM with developed canted SOT device and its advanced integration process that achieved write speed of 0.35ns, thermal stability factor of 70 enough for non-volatile memory, and high TMR ratio of 167% under 400℃ thermal tolerance for 300mm full compatible BEOL process.

11:10 AM **28.6** Field-Free Switching of Perpendicular Magnetization through Voltage-Gated Spin-Orbit Torque

Shouzhong Peng, Jiaqi Lu, Weixiang Li, Lezhi Wang, Xiang Li, Kang Wang, Weisheng Zhao, Beihang University, University of California, Los Angeles

We experimentally demonstrate the field-free switching of perpendicular magnetization by the combination of spin-orbit torque (SOT), exchange bias (EB) and voltage-controlled magnetic anisotropy (VCMA) in the IrMn/CoFeB/MgO structure. A high-density and ultra-low-power (6.2 fJ/bit) voltage-gated spintronic memory is proposed and successfully verified by both experiments and simulations.

11:35 AM **28.7** A Multilevel FeFET Memory Device based on Laminated HSO and HZO Ferroelectric Layers for High-Density Storage

Tarek Ali, Patrick Polakowski, Kati Kühnel, Malte Czernohorsky, Thomas Kämpfe, Matthias Rudolph, Björn Pätzold, David Lehninger, Franz Müller, Ricardo Olivo, Maximilian Lederer, Raik Hoffmann, Philipp Steinke, Katrin Zimmermann, Uwe Mühle, Konrad Seidel, Johannes Mueller, Fraunhofer IPMS-Center Nanoelectronic Technologies (CNT), Ferroelectric Memory GmbH

We report 1-3 bit/cell FeFET operation through optimized HSO and HZO ferroelectric laminate layers using alumina interlayers. Memory window up to 3.5V, switching speed of 300ns, 10 years retention, and 10^4 endurance are reported. The gate stack lamination merits are discussed with insight potential of FeFET as an MLC memory.

12:00 PM **28.8** A Novel Ferroelectric Superlattice Based Multi-Level Cell Non-Volatile Memory

Kai Ni, Jeffrey Smith, Huacheng Ye, Benjamin Grisafe, G. Bruce Rayner, Andrew Kummel, Suman Datta, University of Notre Dame, Kurt J. Lesker Co., University of California, San Diego

We demonstrate a novel and scalable approach to implement multi-level cell memory using ferroelectric (FE) superlattice, which outperforms previous multi-state FE memory implemented using partial

polarization switching, from the standpoint of device-to-device variation. We experimentally demonstrate a 2-bit/cell FE superlattice memory and simulate a 3-bit/cell memory with excellent device-to-device variation.

Advanced Logic Technology - High Mobility Ge-Based Channel Devices
Wednesday, December 11, 9:00 a.m.
Grand Ballroom B
Co-Chairs: Y. Zhao, Zhejiang University
T. Yamaguchi, Renesas Electronic Corp.

9:05 AM **29.1** Strain and Surface Orientation Engineering in Extremely-thin Body Ge and SiGe-on-insulator MOSFETs Fabricated by Ge Condensation
Kwang-Won Jo, Cheol-Min Lim, Wu-Kang Kim, Kasidit Toprasertpong, Mitsuru Takenaka, Shinichi Takagi, The University of Tokyo

We demonstrate a new strain control technology to change high compressive strain into tensile strain in GOI, resulting in operation of 2.5-nm-thick tensile strain GOI n-MOSFETs with electron mobility of 777 cm2/Vs. Also, (110)-oriented compressive strain $Si_{0.46}Ge_{0.54}$OI p-MOSFETs with hole mobility of 837 cm2/Vs has been realized by Ge condensation.

9:30 AM **29.2** Ge Oxide Scavenging and Gate Stack Nitridation for Strained Si0.7Ge0.3 pFinFETs Enabling 35% Higher Mobility than Si
Hiroaki Arimura, Kurt Wostyn, Lars-Ake Ragnarsson, Elena Capogreco, Adrian Chasin, Thierry Conard, Stephan Brus, Paola Favia, Jacopo Franco, Jerome Mitard, Steven Demuynck, Naoto Horiguchi, imec

We have demonstrated multiple ways to reduce the D_{IT} of Si-cap-free low-Ge-content (25-30%) SiGe gate stack. The Dit is reduced by Ge oxide scavenging, nitridation and optimized high-pressure anneal. 8-nm-wide strained scaled $Si_{0.7}Ge_{0.3}$ pFinFET with the optimized gate stack demonstrated 35% mobility improvement over Si counterpart.

9:55 AM **29.3** First Vertically Stacked Tensily Strained Ge0.98Si0.02 nGAAFETs with No Parasitic Channel and LG = 40 nm Featuring Record ION = 48 uA at VOV=VDS=0.5V and Record Gm,max(uS/um)/SSSAT(mV/dec) = 8.3 at VDS=0.5V
Chien-Te Tu, Yu-Shiang Huang, Fang-Liang Lu, Hsiao-Hsuan Liu, Chung-Yi Lin, i-Chun Liu, Chee Wee Liu, National Taiwan University

Si incorporation as small as 2% into Ge achieves etching selectivity of Ge over $Ge_{0.98}Si_{0.02}$. The infrared response can confirm the removal of the parasitic channel. Record I_{ON} of 48 μA at $V_{OV}=V_{DS}=0.5V$ and record Q of 8.3 at $V_{DS}=0.5V$ with L_G = 40 nm are achieved among Ge nFETs.

10:20 AM **29.4** Enabling Sub-5nm CMOS Technology Scaling: Thinner and Taller! (Invited)
Julien Ryckaert, Myung Hee Na, Pieter Weckx, Doyoung Jang, Pieter Schuddinck, Bilal Chehab, Sudhir Patli, Satadru Sarkar, Odysseas Zografos, Rogier Baert, Diederik Verkest, imec

Scaling beyond 5nm will bring us into the post FinFET era where new device architectures optimized for CMOS logic scaling will be required. In this paper, the evolution to vertically stacked Nanosheets, Forksheet, and finally CFET are reviewed in conjunction with buried power rails and wrap around contact.

10:45 AM **29.5** First Stacked Ge0.88Sn0.12 pGAAFETs with Cap, LG=40nm, Compressive Strain of 3.3%, and High S/D Doping by CVD Epitaxy Featuring Record ION of 58uA at VOV=VDS= -0.5V, Record Gm,max of 172uS at VDS= -0.5V, and Low Noise
Yu-Shiang Huang, Chung-En Tsai, Chien-Te Tu, Hung-Yu Ye, Yi-Chun Liu, Fang-Liang Lu, Chee Wee Liu, National Taiwan University

Record [Sn]=12% and record compressive strain of 3.3% among GeSn 3D transistors to enhance the I_{ON} are demonstrated by CVD epitaxy. For the first time, in-situ $Ge_{0.95}Sn_{0.05}$ caps are grown on stacked $Ge_{0.88}Sn_{0.12}$ channels to improve interface quality and separate carriers from the interface to achieve high mobility. LG is scaled down to 40nm to further boost the I_{ON}. Low channel doping and high S/D doping ([B]peak~1E21cm-3) can suppress the impurity scattering in the channels and reduce the contact resistivity for the S/D, respectively, to reveal the intrinsic merit of the high mobility of GeSn. The stacked 3 $Ge_{0.88}Sn_{0.12}$ nanosheets achieve record ION of 58μA at $V_{OV}=V_{DS}$= -0.5V and record Gm,max of 172μS at V_{DS}= -0.5V among GeSn pFETs, and the performance is comparable to mature Si FinFETs, stacked Si channels, and stacked Ge channels. The caps as barriers on the $Ge_{0.88}Sn_{0.12}$ channels decrease the low frequency noise by reducing trapping/detrapping between the GeSn channels and the gate dielectrics.

11:10 AM **29.6** First Demonstration of Vertical Ge0.92Sn0.08/Ge and Ge GAA Nanowire pMOSFETs with Low SS of 66 mV/dec and Small DIBL of 35 mV/V
Mingshan Liu, Stefan Scholz, Konstantin Mertens, JinHee Bae, Jean-Michel Hartmann, Joachim Knoch, Dan Buca, Qing-Tai Zhao, Forschungszentrum Juelich, RWTH Aachen University, CEA-Leti

We demonstrate for the first time, vertical $Ge_{0.92S}Sn_{0.08}Ge$ and Ge GAA nanowire pMOSFETs. High performance 20nm diameter NW Ge pFETs exhibit low SS (66 mV/dec), small DIBL (35 mV/V) and high $I_{ON}I_{OFF}$ (3×10⁶). Significant improvements were achieved by adopting $Ge_{0.9}>Sn_{0.08}Ge$ heterostructure showing 32% I_{ON} enhancement compared with Ge device.

11:35 AM **29.7** 300mm Heterogeneous 3D Integration of Record Performance Layer Transfer Germanium PMOS with Silicon NMOS for Low Power High Performance Logic Applications (Late News)
Willy Rachmady, Ashish Agrawal, Seung Hoon Sung, Gilbert Dewey, Siddharth Chouksey, Benjamin Chu-Kung, Giselle Elbaz, Paul Fischer, Cheng-Ying Huang, Kimin Jun, Brian Krist, Matthew Metz, Thoe Michaelos, Brennen Mueller, Adedapo Oni, Rajat Paul, Anh Phan, Paul Sears, Tushar Talukdar, Jessica Torres, Bob Turkot, Larry Wong, Hui Jae Yoo, Jack Kavalieros, Intel Corporation

We report a short channel high performance Ge PMOS integrated with Si NMOS in sequential monolithic 3D stacking. A layer transfer Ge PMOS with record ION = 497 uA/um at IOFF = 8nA/um and ION = 630 uA/um at IOFF = 100nA/um and VDS= -0.5V is achieved.

Reliability of Systems and Devices - Memory Reliability and Applications
Wednesday, December 11, 9:00 a.m.
Continental Ballroom 4
Co-Chairs: K. Cheung, NIST
H. Park, SK Hynix

9:05 AM **30.1** Ultra-Low Power Physical Unclonable Function with Nonlinear Fixed-Resistance Crossbar Circuits
Mohammad Reza Mahmoodi, Hussein Nili, Zahra Fahimi, Shabnam Larimian, Hyungjin Kim, Dmitri Strukov, University of California, Santa Barbara

We present a strong PUF design based on crossbar circuits with fixed nonlinear I-V crosspoint devices. The PUF operation was demonstrated using unformed 64×64 crossbar circuits with passively-integrated ReRAM devices. The results show ~4× better circuit density, ~100x less power consumption, and higher robustness compared to prior-work ReRAM-based PUFs.

9:30 AM **30.2** Formation of High Reliability Hydrogen-free MONOS Cells Using Deuterated Ammonia, Masaki Noguchi, Tatsunori Isogai, Hiroyuki Yamashita, Keiichi Sawa, Ryota Fujitsuka, Takanori Yamanaka, Shunsuke Okada, Tomonori Aoyama, Fumiki Aiso, Junko Abe, Yoshihiro Ogawa, Seiji Nakagawa, Hideshi Miyajima, Kioxia Corporation

For high reliability non-volatile memory cell dielectrics, hydrogen-free deuterated CT-SiN and TNL-SiON films are demonstrated by using deuterated ammonia. An ultra-high D/H ratio has been successfully obtained in both films, and these films showed good endurance for program erase stress and data retention properties in MONOS capacitors.

9:55 AM **30.3** Filamentary Statistical Evolution from Nano-Conducting Path to Switching-Filament for Oxide-RRAM in Memory Applications
Ernest Y. Wu, IBM Research

In this work, we demonstrate the Gumbel statistics, a maxima-value distribution for RRAM conductance as opposed to Weibull model. In contrast to Poisson distribution, we show the underlying spatial statistics for switching-filament is controlled by a binomial distribution. The conglomeration of interacting individual vacancies eventually leads to area-dependent single-filament formation.

10:20 AM **30.4** Pushing On-chip Memories Beyond Safe Reliability Boundaries in Micropower Machine-learning Applications (Invited)
Alfio Di Mauro, Francesco Conti, Luca Benini, ETH-Zurich

In today's Deep-Neural-Network accelerators, memory access dominates
inference energy. We analyze voltage over-scaling for on-chip
memories, and explore the energy efficiency and reliability trade-off. Experimental results on FDX22 silicon demonstrate opportunities to achieve maximum efficiency at negligible end-to-end classification accuracy degradation, operating and designing on-chip memories at heavily-reduced reliability margins.

10:45 AM **30.5** OXRAM for Embedded Solutions on Advanced Node: Scaling Perspectives Taking into Account Statistical Reliability and Design Constraints (Invited)
Jury Sandrini, Laurent Grenouillet, Valentina Meli, Niccolo Castellani, Sophie Bernasconi, François Aussenac, Sophie Van Duijin, Marios Barlas, Jean-Francois Nodin, Olivier Billoint, Gabriel Molas, Richard Fournel, Etienne Nowak, Fred Gaillard, Carlo Cagli, Serma Technologies

To scale OXRAM bitcell, both cell and selector devices must be considered. We studied scaled OXRAM reliability down to 30nm and provide BER reducing strategies. We illustrate how scaled transistors meet OXRAM voltage requirements and demonstrate an OXRAM integration in 28nm-FDSOI. Eventually we present a 32Mb+ECC design solution in 40nm.

Emerging Device and Compute Technology - Focus Session: Quantum Computing Infrastructure
Wednesday, December 11, 9:00 a.m.
Continental Ballroom 5
Co-Chairs: I. Radu, imec
Z. Chen, Purdue University

9:05 AM **31.1** Manufacturing Low Dissipation Superconducting Quantum Processors (Invited)
Ani Nersisyan, Stefano Poletto, Nasser Alidoust, Riccardo Manenti, Russ Renzas, Cat-Vu Bui, Kim Fu, Tyler, Yuvraj Mohan, Eyob Sete, Sam Stanwyck, Andrew Bestwick, Rigetti Computing

Near-term quantum computing applications leverage a hybrid architecture, in which classical and quantum computers work together as co-processors. Here, we provide a framework to analyze application runtime performance on such hardware. We then describe two features of Rigetti's Quantum Cloud Services (QCS) mitigate distinct bottlenecks unlocking state-of-the-art hybrid execution speeds.

9:30 AM **31.2** Scalable Quantum Computing Infrastructure Based on Superconducting Electronics (Invited)
Oleg Mukhanov, Robert McDermott, Britton Plourde, SeeQC, Inc., University of Wisconsin, Syracuse University

Superconducting SFQ circuits proximally located to the qubit or sensor arrays can be the technology of choice due to its low power, 10^{-21} Joule to per switching at 20 mK. These circuits can be engineered to produce the minimal back action to qubits.

9:55 AM **31.3** Silicon Hard-Stop Spacers for 3D Integration of Superconducting Qubits (Invited)
William Oliver, Bethany Huffman, David Kim, Mollie Schwartz, Danna Rosenberg, Greg Calusine, Rabi Das, Alexander Melville, Jason Plant, Livia Racz, Jonilyn Yoder, Donna Ruth-Yost, Massachusetts Institute of Technology, MIT Lincoln Laboratory

We demonstrate improved planarity of bonded superconducting qubit chips by utilizing hard-stop silicon spacer posts. We demonstrate high-quality factor resonators on the etched surface and measure qubit coherence (T_1, $T_{<sub>2,echo}$ > 40 μs) in the presence of silicon posts as near as 350 μm to the qubit.

10:20 AM **31.4** A Sparse Spin Qubit Array with Integrated Control Electronics (Invited)
Jelmer Boter, Juan Pablo Dehollain, Jeroen van Dijk, Toivo Hensgens, Richard Versluis, James Clarke, Menno Veldhorst, Fabio Sebastiano, Lieven Vandersypen, Delft University of Technology, Netherlands Organisation for Applied Scientific Research (TNO), Intel Corporation

10:45 AM **31.5** High Volume Electrical Characterization of Semiconductor Qubits (Invited)
Ravi Pillarisetty, Intel Corporation

Perhaps the greatest challenge facing quantum computing hardware development is the lack of a high throughput electrical characterization infrastructure at the cryogenic temperatures required for qubit measurements. In this article, we discuss our efforts to develop a high volume cryogenic electrical characterization line to guide 300mm spin qubit process development.

11:10 AM **31.6** Qubit read-out in Semiconductor Quantum Processors: Challenges and Perspectives (Invited)
Tristan Meunier, CNRS

We report the efforts dedicated towards building a reliable spin read-out for Si spin qubit systems. We review several strategies that are pursued in the semiconductor quantum circuit community. We discuss their performance and their integration potential. We then address the architecture to read-out spin qubits at large scale.

11:35 AM **31.7** Challenges in Scaling-up the Control Interface of a Quantum Computer (Invited)
David Reilly, The University of Sydney, NSW

Challenges at the quantum-classical interface are examined with the goal of architecting a scaled-up quantum computer comprising many thousands of qubits. We propose an interface that leverages cryo-CMOS in concert with protocols that enable parallel readout of qubits via multiplexing. We discuss these sub-systems and outline their advantages.

12:00 PM **31.8** III-V-on-CMOS Devices and Circuits: Opportunities for Quantum Infrastructure (Invited)
Cezar Zota, Thomas Morf, Peter Mueller, Clarissa Convertino, Stefan Filipp, Walter Riess, Czornomaz, IBM Research – Zurich

We demonstrate 3D-integrated III-V devices and circuits on Si CMOS that offer compact and energy-efficient systems. We also propose novel cryogenic III-V LNAs using quantum confinement that operate with orders of magnitude reduction of power dissipation. Applications in quantum infrastructure are explored, where form-factors and power dissipation are key constraints.

Modeling and Simulation - Modeling of Emerging Memory Systems
Wednesday, December 11, 9:00 a.m.
Continental Ballroom 6
Co-Chairs: N. Xu, Samsung
B. Gao, Tsinghua University

9:05 AM **32.1** Quantitative 3-D Model to Explain Large Single Trap Charge Variability in Vertical NAND Memory
Devin Verreck, Antonio Arreghini, Joao Bastos, Franz Schanovsky, Ferdinand Mitterbauer, Christian Kernstock, Markus Karner, Robin Degraeve, Geert Van den bosch, Arnaud Furnemont, imec, Global TCAD Solutions

We present a TCAD model that reproduces large single trap V_T-shifts (>100mV) in 3-D NAND through targeted charge placement based on linear response. With this model, we investigate worst-case V_T-shifts in terms of bias conditions and junction position and we outline a sampling strategy that allows to reproduce experimental distributions.

9:30 AM **32.2** A Comprehensive Modeling Framework for Ferroelectric Tunnel Junctions
Hsin-Hui Huang, Tzu-Yun Wu, Yueh-Hua Chu, Ming-Hung Wu, Chien-Hua Hsu, Heng-Yuan Lee, Shyh-Shyuan Sheu, Wei-Chung Lo, Tuo-Hung Hou, National Chiao Tung University, Industrial Technology Research Institute

A modeling framework for ferroelectric tunnel junctions(FTJs) that considers nonpolar interfacial layers(ILs), multi-domain polarization, and complete ferroelectric/capacitive/tunneling currents is proposed. This FTJ model explains read and write operations of various switching polarities, and provides optimization guidelines where IL location and effective thickness ratio between ferroelectric and IL are most critical.

9:55 AM **32.3** Modeling of Switching Speed and Retention Time in Volatile Resistive Switching Memory by Ionic Drift and Diffusion
Wei Wang, Erika Covi, Yu-Hsuan Lin, Elia Ambrosi, Daniele Ielmini, Politecnico di Milano

We investigated the switching dynamics of Ag filament based volatile switching devices through the switching-on speed and retention time. The surface ionic drift and diffusion mechanism are proposed and confirmed by experimental data. The ionic mobility and diffusivity can be theoretically connected through Einstein relation.

10:20 AM **32.4** A Physics-based Model of RRAM Probabilistic Switching for Generating Stable and Accurate Stochastic Bit-streams
Yudi Zhao, Wensheng Shen, Peng Huang, Weijie Xu, Mengqi Fan, Xiaoyan Liu, Jinfeng Kang, Peking University

A physics-based probabilistic switching model for RRAM stochastic number generator (SNG) is developed to quantify the stochastic bit-streams and evaluate the accuracy of stochastic computing. The model can be used to design the operation scheme of SNG and choose appropriate bit-stream length to achieve target system performance.

10:45 AM **32.5** DNN+NeuroSim: An End-to-End Benchmarking Framework for Compute-in-Memory Accelerators with Versatile Device Technologies
Xiaochen Peng, Shanshi Huang, Yandong Luo, Xiaoyu Sun, Shimeng Yu, Georgia Institute of Technology

DNN+NeuroSim is an integrated framework to benchmark compute-in-memory accelerators for deep neural networks, with hierarchical design options from device-level, circuit-level and up to algorithm-level. With a python wrapper (Pytorch and Tensorflow), this framework supports automatic algorithm to hardware mapping, and evaluates both chip-level performance and inference accuracy with hardware constraints.

Optoelectronics, Displays, and Imagers - Silicon Photonics
Wednesday, December 11, 9:00 a.m.
Continental Ballroom 7-9
Co-Chairs: A. Giesecke, AMO
S. Matsuo, NTT

9:05 AM **33.1** A Silicon Photonics Technology for 400 Gbit/s Applications
Frederic Boeuf, Antonio Fincato, Luca Maggi, Jean Francois Carpentier, Patrick Lemaitre, Mark Shaw, Sebastien Cremer, Nathalie Vulliet, Charles Baudot, Stephane Monfray, Sebastien Jan, Claire Deglise, Jean-Robert Manouvrier, Cedric Durand, Angelica Simbula, Dimitri Goguet, Pierre Bar, Delia

Ristoiu, Francois Leverd, Laurene Babaud, Alessio Daverio, Marco Binda, Adamo Bazzoti, Antonio Canciamilla, STMicroelectronics

A Si-Photonics platform operating at 100 Gbit/s per lane is demonstrated. Integration of 60 GHz photodiode and efficient phase modulator into a 400G-DR4 test chip is shown. Extension towards 400G-FR4 is addressed by the introduction of a SiN layer allowing wideband fiber to the chip optical coupling and polarization management.

9:30 AM **33.2** Silicon Nitride Waveguide Coupled 67+ GHz Ge Photodiode for non-SOI PIC and ePIC Platforms
Stefan Lischke, Dieter Knoll, Christian Mai, Anne Hesse, Anna Peczek, Aleksandra Kroh, Galina Georgieva, Marco Lisker, Detlef Schmidt, Mirko Fraschke, Harald Richter, Andreas Krüger, Georg Winzer, Katrin Schulz, Philipp Kulse, Andreas Trusch, Lars Zimmermann, IHP – Leibniz-Institut für innovative Mikroelektronik, Technical University Berlin, IHP Solutions GmbH

A silicon nitride waveguide coupled Ge photodiode, showing more than 67 GHz bandwidth is demonstrated for the first time, which paves the way for utterly new SiN waveguide platform based applications. The new photodiode can also be a key enabler for a bulk-Si based, monolithically integrated electronic-photonic integrated circuit platform.

9:55 AM **33.3** High-performance Hybrid Silicon and Lithium Niobate Mach–Zehnder Modulators for over 100 Gbit/s (Invited)
Xinlun Cai, Sun Yat-sen University

Based on a Silicon and Lithium Niobate hybrid integration platform, we demonstrate Mach–Zehnder modulators that feature low insertion loss, low drive voltage, large modulation bandwidth, high linearity, compact footprint and low manufacturing cost. The hybrid platform demonstrated here opens up new avenues for future high-speed and energy efficient networks.

10:20 AM **33.4** Integrated DFB Laser Diode and High-efficiency Mach-Zehnder Modulator using Membrane III-V Semiconductors on Si Photonics Platform
Tatsurou Hiraki, Takuma Aihara, Takuro Fujii, Koji Takeda, Takaaki Kakitsuka, Tai Tsuchizawa, Shinji Matsuo, NTT Device Technology Labs

A distributed feedback laser diode and InGaAsP Mach-Zehnder modulator are heterogeneously integrated on Si waveguide circuits. The integrated device shows a fiber output power of 2.9 mW with a laser current of 70 mA, $V\pi L$ of 0.4 Vcm, and an eye opening at 28 Gbit/s with 4.2 Vpp.

10:45 AM **33.5** 2D-3D Integration of High-κ Dielectric with 2D Heterostructures for Opto-electronic Applications
Frank Koppens, ICFO

11:10 AM **33.6** First Demonstration of Waveguide-Integrated Black Phosphorus Electro-Optic Modulator for Mid-Infrared Beyond 4 μm, Li Huang, Bowei Dong, Yiming Ma, Chengkuo Lee, Kah-Wee Ang, National University of Singapore

We demonstrate the first black phosphorus electro-optic modulator integrated with Si waveguide for the mid-infrared spectrum from 3.85 to 4.1 μm. With a gate bias of -4 V, a modulation depth of ~5 dB was achieved with a small active footprint of 225 μm^2 at room temperature.

Sensors, MEMS, and Bioelectronics - Micro and Nano-electromechanical Resonant Sensors and Relays
Wednesday, December 11, 9:00 a.m.
Imperial Ballroom B
Co-Chairs: R. Kumar, Globalfoundries
N. Tas, Univerisity of Twente

9:05 AM **34.1** Phase Change NEMS Relay, James Best
Mohammad Masud, Maarten de Boer, Gianluca Piazza, Carnegie Mellon University

First demonstration of a highly scalable non-volatile mechanical relay (Phase Change NEMS Relay) based on the mechanical expansion of GeTe phase change material. Scaling analysis shows a path towards 20 nm x 5 nm size devices with an actuation voltage and energy of 500 mV and 70 fJ, respectively.

9:30 AM **34.2** Ultra-Low-Voltage Operation of MEM Relays for Cryogenic Logic Applications
Xiaoer Hu, Sergio Almeida, Zhixin Ye, Tsu-Jae King Liu, University of California Berkeley

Operation of micro-electro-mechanical relays at temperatures down to 4K is demonstrated for the first time. Due to dramatically reduced hysteretic switching behavior and elimination of contact oxidation, relays can be operated reliably with sub-25mV voltage signals at <100K. This makes them advantageous for digital logic circuits in cryogenic applications.

9:55 AM **34.3** Monolithic 180nm CMOS Controlled GHz Ultrasonic Impedance Imaging and Sensing
Mamdouh Abdelmejeed, Amit Lal, Yutong Liu, Adarsh Ravi, Justin Kuo, Jaibir Sharma, Srinivas Merugu, Navab Singh, Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR)

For the first time we demonstrate monolithically integrated piezoelectric AlN (aluminum nitride) thin film transducers on 180nm CMOS wafers to realize CMOS GHz ultrasonic transducers. The GHz reflectometer pixels are driven by integrated CMOS circuits, to sense different concentrations of electrolytes, and image surface acoustic impedance demonstrated by fingerprint imaging.

10:20 AM **34.4** MEMS Resonant Microphone Array for Lung Sound Classification
Hai Liu, Song Liu, Anton Shkel, Yongkui Tang, Eun Sok Kim, University of Southern California

This paper presents piezoelectric MEMS microphone arrays for detection of wheezing in lung sound. Very high unamplified sensitivities of 36.3 – 78.2 mV/Pa have been obtained within frequencies 200-500 Hz where wheezing is typically prominent. Consequently, the wheezing was distinguished better and as high as 97.44% identification accuracy was achieved.

10:45 AM **34.5** Extremely High Q AlN Lamb Wave Resonators Implemented by Weighted Electrodes
Anming Gao, Jie Zou, University of Illinois at Urbana-Champaign, University of California Berkeley

This paper presents unprecedentedly high Q AlN S0 Lamb wave resonators achieved by introducing two half-width top interdigitated transducers. The high-Q AlN resonator is experimentally shown with Q of 5500 in room temperature, which is the highest Q ever reported for all reported AlN S0 Lamb wave resonators.

11:10 AM **34.6** Galfenol-Ti-Diamond Multilayer MEMS Resonator for Magnetic Sensor Working up to 773 K

Zilong Zhang, Liwen Sang, Haihua Wu, Jian Huang, Linjun Wang, Satoshi Koizumi, Yasuo Koide, Meiyong Liao, National Institute for Materials Science, Shanghai University

We demonstrate a novel high-temperature magnetic sensor based on the hybrid structure of Galfenol/Ti/single crystal diamond (SCD) MEMS resonators up to 773K. The developed magnetic sensor exhibits a stable high-sensitivity and low noise level ~247 pT/√Hz at 773 K, which exceeds those of reported magnetic sensors at high temperatures.

Memory Technology - Selectors and RRAM: Technology and Computing
Wednesday, December 11, 1:30 p.m.
Grand Ballroom A
Co-Chairs: H-Y Cheng, Macronix International Co., Ltd.
S. Spiga, CNR-IMM

1:35 PM **35.1** Composition Optimization and Device Understanding of Si-Ge-As-Te Ovonic Threshold Switch Selector with Excellent Endurance

Daniele Garbin, Wouter Devulder, Robin Degraeve, Gabriele Luca Donadio, Sergiu Clima, Karl Opsomer, Andrea Fantini, Daniel Cellier, Wan Gee Kim, Mahendra Pakala, Andrew Cockburn, Christophe Detavernier, Romain Delhougne, Ludovic Goux, Gouri Sankar Kar, imec, Applied Materials, Inc., Ghent University

We explore the composition space of the Si-Ge-As-Te based ovonic threshold switch selector device. We optimize the composition to increase the crystallization temperature T_x >450°C and achieve stable endurance of more than 10^{11} cycles. We propose a switching model that predicts the distribution of the threshold voltage, drift and time-dependent instabilities.

2:00 PM **35.2** Endurance Improvement of More than Five Orders in GexSe1-x OTS Selectors by using a Novel Refreshing Program Scheme

Firas Hatem, Zheng Chai, Weidong Zhang, Andrea Fantini, Robin Degraeve, Sergiu Clima, Daniele Garbin, John Robertson, Yuzheng Guo, Jian Fu Zhang, John Marsland, Pedro Freitas, Ludovic Goux, Gouri Sankar Kar, imec, Liverpool John Moores University, University of Cambridge, Wuhan University

OTS degradation and the endurance can be therefore improved by more than five orders without adding additional material elements or process steps, based on understanding of the recoverable (slow delocalized defects) and non-recoverable (Ge-Se segregation/crystallization) degradation mechanisms.

2:25 PM **35.3** Reliability and Variability of 1S1R OxRAM-OTS for High Density Crossbar Integration

Diego Alfaro Robayo, Gilbert Sassine, Joel Minguet Lopez, Laurent Grenouillet, Anthonin Verdy, Gabriele Navarro, Mathieu Bernard, Eduardo Esmanhotto, Cathy Carabasse, Damien Deleruyelle, Elisa Vianello, Niccolo Castellani, Lorenzo Ciampolini, Bastien Giraud, Carlo Cagli, Gérard Ghibaudo, Etienne Nowak, Gabriel Molas, CEA Leti, INL CNRS, IMEP-LAHC

HfO_2-OxRAM was co-integrated with optimized OTS selector in 1S1R arrays. Up to 3 decades of current window margin and 5 decades of selectivity were achieved. More than 10^6 programming, and 10^9 read-disturb cycles were demonstrated. 1Gb bank size is envisaged. Semi-analytical model of OTS was developed to analyze stochastic switching.

2:50 PM **35.4** Learning with Resistive Switching Neural Networks (Invited)
Mingyi Rao, Zhongrui Wang, Can Li, Hao Jiang, Rivu Midya, Peng Lin, Daniel Belkin, Wenhao Song, Shiva Asapu, Qiangfei Xia, Joshua Yang, University of Massachusetts, Amherst, Yale University, MIT

Processing-in-memory with RRAMs or memristors is a potential solution to accelerate machine learning in hardware neural networks, which may drastically improve the energy-area efficiency. Here, we discuss three major types of learning, namely the supervised, reinforcement, and unsupervised learning implemented with various 1T1R based neural networks.

3:15 PM **35.5** Novel 1T2R1T RRAM-based Ternary Content Addressable Memory for Large Scale Pattern Recognition
Denys R. B. Ly, Jean-Philippe Noel, Bastien Giraud, Pablo Royer, Eduardo Esmanhotto, Niccolo Castellani, Thomas Dalgaty, Jean-Francois Nodin, Claire Fenouillet-Beranger, Etienne Nowak, Elisa Vianello, CEA-Leti

Resistive-Memories (RRAMs) enable implementations of area-and-energy-efficient Ternary-Content-Addressable-Memories (TCAMs). However, the low RRAM resistance ratio limits the word length of RRAM-based TCAMs hindering the parallel search of large volumes of data for data-intensive applications. Here, we propose a new 1-transistor-2-RRAMs-1-transistor TCAM insensitive to RRAM resistance ratio allowing searches of large pattern.

3:40 PM **35.6** High-Density Multiple Bits-per-Cell 1T4R RRAM Array with Gradual SET/RESET and its Effectiveness for Deep Learning
E. R. Hsieh, M. Giordano, B. Hodson, Akash Levy, S. K. Osekowsky, R. M. Radway, Y. C. Shih, W. Wan, T. F. Wu, Xin Zheng, M. Nelson,. B. Q. Le, H. -S. Philip Wong, S. Mitra, S. Wong, Stanford University, SkyWater Technology Foundry

We present the first demonstration of 1T4R Resistive RAM (RRAM) array storing two bits per RRAM cell. Our HfO_2-based RRAM is built using a logic foundry technology that is fully compatible with the CMOS back-end process.

4:05 PM **35.7** Metal-oxide Based, CMOS-compatible ECRAM for Deep Learning Accelerator
Seyoung Kim, Teodor Todorov, Murat Onen, Tayfun Gokmen, Douglas Bishop, Paul Solomon, Ko-tao Lee, Matt Copel, Damon Farmer, John Ott, Takashi Ando, Hiroyuki Miyazoe, Vijay Narayanan, John Rozen, IBM Research

We demonstrate a CMOS-compatible, metal-oxide based Electro-Chemical Random-Access Memory (MO-ECRAM) featuring symmetric and linear conductance update and selector-less parallel array operations while withstanding high temperature treatments necessary for BEOL compatibility. For the first time, we experimentally show a successful stochastic gradient descent algorithm demonstration using an MO-ECRAM array.

4:30 PM **35.8** Co Active Electrode Enhances CBRAM Performance and Scaling Potential
Attilio Belmonte, Janaki Radhakrishnan, Ludovic Goux, Gabriele Luca Donadio, Augusto Redolfi, Romain Delhougne, Laura Nyns, Wouter Devulder, Thomas Witters, Angelo Covello, Alexis Franquet, Valentina Spampinato, Shreya Kundu, Ming Mao, Hubert Hody, Gouri Sankar Kar, Guy Vereecke, imec, Università della Calabria

We report for the first time the low-current performance enhancement combined with the improvement of the scaling potential in CBRAM devices by adopting Co as active electrode. Co is proven to yield, with respect to Cu, faster/lower voltage switching and more stable conductive filaments.

Advanced Logic Technology - CMOS Platform Technologies
Wednesday, December 11, 1:30 p.m.
Grand Ballroom B
Co-Chairs: C. Chu, Applied Materials
Y. Li, Lam Research

1:35 PM **36.1** Design-Technology Co-Optimization of Anti-Fuse Memory on Intel 22nm FinFET Technology
Yu-Lin Chao, Sarvesh H. Kulkarni, Soonwoo Cha, Leif R. Paulson, Salil M. Rajarshi, Jason Bloomstrom, Guannan Liu, Mark Armstrong, Jiabo Li, Chen-Yi Su, Stephen M. Ramey, Uddalak Bhattacharya, Bernhard Sell and Ying Zhang Logic Technology Development, Intel Corporation

An in-depth study of Intel's first FinFET anti-fuse memory is reported. Improvement on gate oxide integrity, source/drain resistance optimization, careful layout design on both bitcell and array, and smart selection of synthesis in combination can offer an array yield exceeding 99.9% without redundancy scheme and at no added process cost.

2:00 PM **36.2** Variability Sources in Nanoscale Bulk FinFETs and TiTaN- a Promising Low Variability WFM for 7/5nm CMOS Nodes
Mandar S. Bhoir, Thomas Chiarella, Lars-Ake Ragnarsson, Jerome Mitard, Naoto Horiguchi, Nihar Ranjan Mohapatra, IIT Gandhinagar, imec

An experimental methodology to segregate variability sources in FinFETs (W_{fin} <10nm) is proposed. The V_t variation, from gate work-function metal (WFM) and oxide charge variations, is the major contributor to in-wafer variability. The FER, GER, RDF contribution to V_t variability is negligible. TiTaN, low variability WFM, for future gate-stack, is introduced.

2:25 PM **36.3** Key Technology Enablers of Innovations in the AI and 5G Era (Invited)
Shien-Yang Wu, Taiwan Semiconductor Manufacturing Company

The proliferation of AI and the deployment of 5G networks accelerate the transformation of our society into a highly connected world. Semiconductors are the indispensable elements in realizing all the product

innovations. The progress and challenges of the state of art CMOS technology and advanced packaging will be reviewed.

2:50 PM **36.4** Ultra-scaled Conformal Scavenging Electrode with Superior Tunability for Short-channel RMG FinFET Workfunction and all-ALD 3D-compatible ReRAM
John Rozen, Yohei Ogawa, Takashi Ando, Ruqiang Bao, Eduard Cartier, Kazuhiro Honda, Keon-Chang Lee, John Bruley, Hiroyuki Miyazoe, Koukou Suu, Masanobu Hatanaka, Vijay Narayanan, ULVAC Inc., IBM Research

A baseline TiAl-containing ALD workfunction electrode is established. Furthermore, a novel ALD metal-compund material, MX, yields at least 10Å further scaling of the electrode stack in RMG FinFETs due to its superior scavenging power. For the first time, using MX, we demonstrate an all-ALD ReRAM compatible with 3D architectures.

3:15 PM **36.5** Novel Forksheet Device Architecture as Ultimate Logic Scaling Device Towards 2nm
Pieter Weckx, Julien Ryckaert, Eugenio Litta, Dmitry Yakimets, Philippe Matagne, Pieter Schuddinck, Doyoung Jang, Bilal Chehab, Rogier Baert, Mohit Gupta, Yusuke Oniki, Lars-Ake Ragnarsson, Naoto Horiguchi, Alessio Spessot, Diederik Verkest, imec

Due to CPP scaling slowdown below 42nm, several scaling boosters are needed to reduce the logic standard cell height. Limited scaling can be achieved using FinFET and nanosheets due integration limits for PN separation. A novel forksheet device is proposed achieving extremely scaled PN space using limited additional processing complexity.

3:40 PM **36.6** Machine Learning-enhanced Multi-dimensional Co-Optimization of Sub-10nm Technology Node Options
Ahmet Ceyhan, Jonathan Quijas, Saurabh Jain, Hung-Yi Liu, William E. Gifford, Sourav Chakravarty, Intel Corporation

This paper introduces a machine-learning-enhanced multi-objective, multi-domain co-optimization framework. It presents a holistic approach to define a technology node by co-optimizing its options from the transistor to system level and demonstrates 10X improvement in turn-around time with better quality of results compared to human-optimized CPU implementations in Intel's 10nm technology.

4:05 PM **36.7** 5nm CMOS Production Technology Platform featuring full-fledged EUV, and High Mobility Channel FinFETs for Mobile SoC and High Performance computing Applications (Late News)
Geoffrey Yeap, TSMC

Industry-leading 5nm CMOS technology features, for the first time, full-fledged EUV, and high mobility channel finFETs, offering ~1.84x logic density, 15% speed gain or 30% power reduction over 7nm. This true 5nm technology successfully passed qualification with high yield, and targets for mass production in 1H 2020.

Emerging Device and Compute Technology - Nano Devices for Low-Power Technologies
Wednesday, December 11, 1:30 p.m.

Continental Ballroom 4
Co-Chairs: H. Fukutome, Samsung
F. Schwierz, Technical University Ilmenau

1:35 PM **37.1** Sub-Thermionic Scalable III-V Tunnel Field-Effect Transistors Integrated on Si (100)
Clarissa Convertino, Cezar Zota, Yannick Baumgartner, Philipp Staudinger, Marilyne Sousa, Svenja Mauthe, Daniele Caimi, Lukas Czornomaz, Adrian Ionescu, Kirsten Moselund,IBM Research - Zurich, EPFL

We present scalable III-V tunnel FETs fabricated using a Si CMOS-compatible FinFET process flow and integrated on Si (100) substrates. The devices exhibit a minimum SS of 47 mV/decade, an I_{ON} of 1.5 µA/µm at I_{OFF} = 1 nA/µm and V_{DD} = 0.3 V, and I_{60} of 10 nA/µm.

2:00 PM **37.2** Co-integrated Subthermionic 2D/2D WSe2/SnSe2 Vertical Tunnel FET and WSe2 MOSFET on same flake: towards a 2D/2D vdW Dual-Transport Steep Slope FET
Nicolo Oliva, Luca Capua, Matteo Cavalieri, Adrian Ionescu, EPFL

In this work we report the fabrication, co-integration and resulting performance of 2D/2D van der Waals (vdW) Vertical p-type Tunnel FETs and p-MOSFETs in a WSe_2SnSe_2 material system. We report the best ever reported combined performance in terms of subthermionic subthreshold swing for a 2D/2D vertical Tunnel FET.

2:25 PM **37.3** Experimental Demonstration of Integrated Magneto-electric and Spin-orbit Building Blocks Implementing Energy-efficient Logic
Chia-Ching Lin, Tanay Gosavi, Dmitri Nikonov, Yen-Lin Huang, Bhagwati Prasad, WonYoung Choi, Van Tuong Pham, Jun-Yang Chen, Mahendra DC, Huichu Liu, Kaan Oguz, Emily Walker, John Plombon, Benjamin Buford, Carl Naylor, Jian-Ping Wang, Felix Casanova, Ramamoorthy Ramesh, Ian Young, University of California, Berkeley, Intel Corporation, CIC nanoGUNE, University of Minnesota

600 mV magneto-electric switching in 30 nm La-doped $BiFeO_3$ multiferroic oxide and a proof of concept 7 µV spin-orbit signal output in Pt / CoFe local spin injection device with 100 µA supply current were experimentally demonstrated at room temperature for the 1st time. Also demonstrated was a path towards 70 mV spin orbit output using Bi_2Se_3 in a local spin injection device. These are key accomplishments for WRITE and READ building blocks, respectively, toward realization of a magneto-electric spin-orbit (MESO) energy efficient logic device. Moreover, the 1st generation of a MESO logic device with a functional READ unit is demonstrated.

2:50 PM **37.4** Self-organized Pairs of Ge Double Quantum Dots with Tunable Sizes and Spacings Enable Room-Temperature Operation of Qubit and Single-Electron Devices
Kang-Ping Peng, Ching Lun Chen, Ying-Tsan Tang, David M. T. Kuo, Thomas George, Horng-Chih Lin, Pei-Wen Li, National Chiao Tung University, Taiwan Semiconductor Research Institute, National Central University

We report paired Ge double QDs using spacer technology in combination with oxidation of $Si_{0.85}Ge_{0.15}$ in a self-organization approach. Process-controlled tunability of Ge QD diameters (5–20nm) and spacings (12nm) were achieved. We demonstrated room-temperature operation of Ge qubit devices, within which one QD encodes charges with a proximal QD-SET reads-out.

3:15 PM **37.5** A Probabilistic Approach to Quantum Inspired Algorithms (Invited)
Shuvro Chowdhury, Supriyo Datta, Kerem Yunus Camsari, Purdue University

We describe Probabilistic Computing, based on probabilistic or p-bits that fluctuate between 0 and 1, that are in between digital and quantum mechanical bits. Compact, energy efficient hardware p-bits realized from present-day spintronic building blocks can be interconnected into p-circuits to implement a host of quantum computing inspired algorithms.

3:40 PM **37.6** High-speed Low-energy Heat Signal Processing via Digital-compatible Binary Switch with Metal-insulator Transitions
Takeaki Yajima, Takahisa Tanaka, Yusuke Samata,Ken Uchida,Akira Toriumi, The University of Tokyo

The binary thermistor using the VO_2 metal-insulator transition enables the direct conversion of heat signal to the digital bits with high speed (sub-ns) and low energy (sub-pJ), promising for microscopic heat management. The binary thermistor also enables the high-speed and low-energy heat-mediated data transfer as a basis for non-charge-based functionalities.

4:05 PM **37.7** Gate Reflectometry for Probing Charge and Spin States in Linear Si MOS Split-gate Arrays
Louis Hutin, Benoit Bertrand, Emmanuel Chanrion, Heorhii Bohuslavskyi, Fabio Ansaloni, Tsung-Yeh Yang, John Michniewicz, David Niegemann, Cameron Spence, Theodor Lundberg, Anasua Chatterjee, Alessandro Crippa, Jing Li, Romain Maurand, Xavier Jehl, Marc Sanquer, Fernando Gonzalez-Zalba, Ferdinand Kuemmeth, Yann-Michel Niquet, Silvano De Franceschi, Matias Urdampilleta, Tristan Meunier, Maud Vinet, CEA Leti, CNRS Institut Néel, University of Copenhagen, University of Cambridge, CEA IRIG, Hitachi Cambridge Laboratory

We fabricated a 2×N array of individually controllable Si quantum dots (QDs) with nearest neighbor coupling. We implemented two different gate reflectometry-based readout schemes to either probe spin-dependent charge movements by a coupled electrometer with single-shot precision, or directly sense a spin-dependent quantum capacitance.

4:30 PM **37.8** Experimental Demonstration of Phase Transition Nano-Oscillator Based Ising Machine
Sourav Dutta, Abhishek Khanna, Jorge Gomez, Kai Ni, Zoltan Toroczkai, Suman Datta, University of Notre Dame

Finding the ground state of Ising model maps to various combinatorial optimization problems. Here, we experimentally demonstrate an Ising machine using coupled phase transition metal-to-insulator nano-oscillators (IMT-NO). Compared to other implementations, our hardware provides advantage from the standpoint of room-temperature operation, programmable coupling scheme, compactness and ease of scalability.

Memory Technology - Memory for Neural Network
Wednesday, December 11, 1:30 p.m.
Continental Ballroom 5

Co-Chairs: M. Liu, Chinese Academy of Science
Q. Ren, UNIC Memory Technology Co., Ltd

1:35 PM **38.1** Optimal Design Methods to Transform 3D NAND Flash into a High-Density, High-Bandwidth and Low-Power Nonvolatile Computing in Memory (nvCIM) Accelerator for Deep-Learning Neural Networks (DNN)
Hang-Ting Lue, Macronix

We propose optimal design methods of 3D NAND Flash to achieve high-density, high-bandwidth and low-power nvCIM. The proposed 3D NAND nvCIM can produce TOPS/W ~40 (4I4W), and achieve 74.6 frame/sec for a heavy VGG16 network. It is potential to provide high-density and low-power accelerator for deep-learning neural network.

2:00 PM **38.2** Storage Reliability of Multi-bit Flash Oriented to Deep Neural Network
Yachen Xiang, Peng Huang, Haozhang Yang, Kunliang Wang, Runze Han, Wensheng Shen, Yulin Feng, Chen Liu, Xiaoyan Liu, Jinfeng Kang, Peking University

The storage reliability of multi-bit flash is of vital importance for the flash based deep neural network (DNN). In this work, the critical concerns correlated with the storage reliability (I_d) distribution and data retention) of multi-bit flash and its impacts on the DNN are investigated for the first time.

2:25 PM **38.3** A 3D NAND Flash Ready 8-Bit Convolutional Neural Network Core Demonstrated in a Standard Logic Process
Minsu Kim, Muqing Liu, Luke Everson, Gyusung Park, Younghee Jeon, Sihwan Kim, Sang-Soo Lee, Seung-hwan Song, Chris Kim, University of Minnesota, Anaflash

A convolutional neural network (CNN) core that can be readily mapped to a 3D NAND flash array was demonstrated in a standard 65nm CMOS process. Logic-compatible embedded flash memory cells were used for storing multi-level synaptic weights while a bit-serial architecture enables 8 bit multiply-and-accumulate operation.

2:50 PM **38.4** High-Density and Highly-Reliable Binary Neural Networks Using NAND Flash Memory Cells as Synaptic Devices
Sung-Tae Lee, Hyungsu Kim, Jong-Ho Bae, Honam Yoo, Nag Yong Choi, Dongseok Kwon, Suhwan Lim, Byung-Gook Park, Jong-Ho Lee, Seoul National University

A novel synaptic architecture based on NAND cell strings is proposed as a high-density synapse capable of XNOR operation for binary neural networks (BNNs) for the first time. By changing the threshold voltage of NAND flash cells and input voltages in complementary fashion, the XNOR operation is successfully demonstrated.

3:15 PM **38.5** Complementary Memory Cell Based on Field-Programmable Ferroelectric Diode for Ultra-Low Power Current-SA Free BNN Applications
Qing Luo, Bing Chen, Rongrong Cao, Xiaoyong Xue, Keji Zhou, Jianguo Yang, Xu Zheng, Yu, Jie Yu, Tiancheng Gong, Xiaoxin Xu, Peng Yuan, Xiaoyan Li, Lu Tai, Qi Liu, Hangbing Lv, Ming Liu, Institute of Microelectronics of Chinese Academy of Sciences, Zhejiang University, Fudan University

We proposed a complementary memory cell with 2T4D XNOR structure for computing in memory (CIM) applications. Firstly, a field-programmable diode (FPD) was demonstrated with a W/HZO/W structure. For BNN application, a 2T4D XNOR cell-based CSA-free BNN architecture is proposed with small cell area (16 F^2) and superior efficiency (387 TOPS/W).

3:40 PM **38.6** A 2TnC Ferroelectric Memory Gain Cell Suitable for Compute-in-memory and Neuromorphic Application
Stefan Slesazeck, Taras Ravsher, Viktor Havel, Evelyn Breyer, Halid Mulaosmanovic, Thomas Mikolajick, NaMLab gGmbH, NaMLab gGmbH and TU Dresden

A 2TnC ferroelectric memory gain cell is proposed, that can be operated either in FeRAM or FTJ mode. The internal gain of the cell mitigates the need for 3D integration of the FeCAPs, making the concept very attractive for embedded memories, compute-in-memory and neuromorphic applications.

4:05 PM **38.7** Memory-Logic Hybrid Gate with 3D-Stackable Complementary Latches for FinFET-based Neural Networks
Chieh Lee, Yue-Der Chih, Jonathan Chang, Chrong Jung Lin, Ya-Chin King, National Tsing Hua University, Taiwan Semiconductor Manufacturing Company, Ltd.

A memory-logic hybrid gate with complementary resistive switching pairs on vias in BEOL FinFET technologies with an area-efficient, 3D-stackable structures is proposed. Stable output logic stages enabled by the complementary states on the RRAM pair have been demonstrated. Through stacked-vias architectures, logic operations based on multiple non-volatile states are achieved.

Modeling and Simulation - Multiscale Modeling of Devices and Circuits
Wednesday, December 11, 1:30 p.m.
Continental Ballrom 6
Co-Chairs: W. Vandenberghe, University of Texas, Dallas
C. Weber, Intel

1:35 PM **39.1** State-of-the-art TCAD: 25 Years Ago and Today Invited)
Mark Stettler, Intel Corporation

This talk contrasts Intel’s TCAD environment of 25 years ago with today’s, which has shifted steadily from more applications-oriented work towards research, and gives examples of studies which illustrate the evolution.

2:00 PM **39.2** Efficient Variability- and Reliability-aware Device-Circuit Co-Design: From Trap Behaviors to Circuit Performance
Wangyong Chen, Linlin Cai, Gang Du, Xiaoyan Liu, Peking University

An efficient variability- and reliability- aware solution is proposed to achieve the device-circuit co-design. STIM method links the charge distributions to the time-dependent variability and reliability. A variation-aware model based on the database is proposed to predict the time-dependent delay degradation and potential critical paths in the digital circuits.

2:25 PM **39.3** Role of Correlation in Systematic Variation Modeling
Ananda Roy, Sourabh Dongaonkar, Sivakumar Mudanai, Intel Corporation

In this work, we show the important, and so far, unrecognized, role that the fine structure of parameter correlations plays in accurate modeling of random variable based systematic variation. We provide an intuitive statistical model to go beyond simple correlation coefficient and accurately capture distribution of measured electrical quantities.

2:50 PM **39.4** An Empirically Validated Virtual Source FET Model for Deeply Scaled Cool CMOS

Wriddhi Chakraborty, Kai Ni, Jeffrey Smith, Arijit Raychowdhury, Suman Datta, University of Notre Dame, Georgia Institute of Technology

We conclude that while ballistic efficiency of nanoscale MOSFETs degrade in linear region as we approach cryogenic temperature, its ballistic efficiency improves in the saturation region at low temperature. The model is used to project performance of Cool CMOS technology for 15nm channel length FETs at deeply scaled nodes.

3:15 PM **39.5** Multiphysics Simulation & Design of Silicon Quantum Dot Qubit Devices

Fahd Ayyalil Mohiyaddin, George Simion, Nard Dumoulin Stuyck, Roy Li, Florin Ciubotaru, Geert Eneman, Fabian Bufler, Stefan Kubicek, Julien Jussot, BT Chan, Tsvetan Ivanov, Alessio Spessot, Philippe Matagne, James Lee, Bogdan Govoreanu, Iuliana Radu, imec, KU Leuven

Silicon qubits are strong contenders for building a large-scale quantum processor. Here, we combine several multiphysics simulation methods to assemble a design methodology for silicon qubit devices. We summarize key device parameters, dimensions and voltages based on detailed models that consider device electrostatics, stress, micro-magnetics, band-structure and spin dynamics.