Focused Call for Papers

IEDM is pleased to announce increased technical focus in the area of:

**Advanced Logic Technology (ALT)**

Topics

Papers are solicited in the following themes of interest:

- CMOS platform technologies
- Logic devices performance and circuit design challenges & opportunities
- Advanced, novel process integration schemes and (applications-driven) scaling approaches
- Process module innovations and progresses in process control & process metrology
- Device technology co-optimization (DTCO)

New or trending areas include:

- Si1-xGex channels, GAA (vertically stacked) nanowires and nanosheets based devices and circuits
- Sequential, monolithic 3D integration, heterogenous chiplets, 2.5/3D integration
- Interconnects (TSV, BEOL, Frontside and Backside connectivity)
- BEOL compatible transistors

Paper Submission

Submission deadline: July 23rd
Single submission of final, four-page paper