Processes and Materials Engineering Innovations for Advanced Logic Transistor Scaling

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Abstract: AI computing workloads require demanding semiconductor solutions at a time when traditional Moore's Law scaling is slowing down. The drive to continue improving semiconductor power, performance, area and cost scaling (PPAC) is enabled by new architectures, new structures for 3D devices, new materials, new ways to shrink, and advanced packaging. In this short course, we will first discuss process technology and materials engineering approaches used to extend FinFET scaling more specifically for critical FEOL modules (channel, junction, gate and contact). As gate length must continue scaling, new architecture Gate All Around Nanosheet is being pursued to alleviate FinFET electrostatics limitation. We will discuss benefits and challenges of GAA Nanosheet architecture for forthcoming generation of advanced CMOS and highlight how novel co-optimized processes and materials innovations play a critical role to address integration and device performance challenges.

Dr. Benjamin Colombeau is a Sr Director at Applied Materials in charge of FEOL Integration. He obtained his PhD in Materials Science and Engineering in 2001 at CNRS Toulouse, France. His PhD thesis received the French award of best PhD thesis in Materials Science, Technology and Electronics, Toulouse 2001. He was a research fellow in the Advanced Technology Institute (ATI) at University of Surrey (UK) within European projects IST/FRENDTECH/ARTEMIS. In 2005, Dr. Colombeau joined Chartered Semiconductor Singapore as Project Leader in the Technology Development. Since 2008, Dr. Colombeau is working for Applied Materials first in Varian then moved to Applied SCLA Headquarter in charge of Front-End transistor formation. He is a well-recognized expert in FEOL Technology for advanced CMOS devices and has given invited speeches/lectures at many international conferences/workshops including VLSI TSA, MRS, IEEE IWJT, IEEE IIT, ECS etc. He has been in the organizing committee of several international conferences and since 2018, Dr Colombeau is an active member of IEEE VLSI conference technical committee. Dr. Colombeau has published numerous papers (> 150 papers) in refereed journals (IEEE IEDM/VLSI/EDL/TED etc.) and is holder of numerous US and UK patents. He is active reviewer for IEEE EDL, TED, and APL.