Beyond FinFET Devices: GAA, CFET, 2D Material FET

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Abstract: With the introduction of FinFET technology on Intel's 22nm process node in 2011, the three-dimensional channel structure unleashed a new era of design-technology co-optimization for both high performance and low power workloads. In FinFETs, transistor density and performance scaling are driven by Fin geometry optimization, high-mobility channel materials and contact resistance reduction with scaled Contacted Poly Pitch (CPP) and gate length. As FinFET scaling comes to an end, there are several innovative device architectures for next generation technologies: from gate-all-around (GAA) transistor, complementary FET (CFET), to atomic channel FET with 2D materials. The GAA transistor is the most pragmatic architecture in the near term to enable incremental CPP and gate length scaling because of its limited perturbation to a conventional FinFET process integration and design flows. CFET (3D stacking) technology brings additional cell level area scaling benefit as well as heterogeneous integration benefit for high mobility channel enablement. 2D material FET provides the ultimate gate length scaling with high mobility channel capability. In this short course, we will focus on the status of these innovations with the corresponding engineering opportunities and challenges for high volume manufacturing.

Chung-Hsun Lin is Senior Director and Technology Performance Manager on leading edge technologies in Logic Technology Development at Intel. His current role is in the overseeing the development and performance of Intel's RibbonFET and PowerVia. His team is responsible for technology definition, transistor performance, test chip integration, PDK model targets, and customer engagement. Before he joined Intel, Chung-Hsun led several advanced technology development and exploratory device research projects at GlobalFoundries and IBM, including the delivery of 22nm Planar SOI and 14nm FinFET on SOI technologies for high performance computing. Chung-Hsun received his Ph.D. degree in electrical engineering and computer sciences from the University of California, Berkeley and his B.S/M.S degrees in electrical engineering from National Taiwan University, Taiwan. His Ph.D. work contributed to the first industrial standard FinFET compact model: BSIM-CMG. Chung-Hsun holds over 135 US patents and has published over 70 papers in accredited journals and international conferences in semiconductor technology.