

Heterogeneous Integration Using Chiplets & Advanced Packaging

Madhavan Swaminathan, Georgia Tech

Abstract: The semiconductor industry is moving towards heterogeneous integration for three primary reasons namely, 1) monolithic integration using large dies in advanced nodes is becoming uneconomical, 2) time to market using monolithic integration is becoming long because of design, yield and integration complexity, and 3) systems today are driven by heterogeneity where use of a single transistor process alone is insufficient to meet the requirements. But how does the landscape look like for heterogeneous integration? What are the advanced packaging platforms available for both 2.5D and 3D integration? What are the technologies available today and what are the emerging technologies? How does one compare the various technologies? What is the minimum chiplet size that can be assembled and the largest package size that can be supported? How does heterogeneity affect signal integrity and power delivery? In this presentation these questions will be answered where the various categories of advanced packaging technologies will be described and compared along with details on construction, line dimensions, form factor, bandwidth density, data rate, power delivery metrics, thermal management solutions, and system integration potential. Details on emerging technologies such as glass interposer will also be presented.

Madhavan Swaminathan is the John Pippin Chair in Microsystems Packaging & Electromagnetics in the School of Electrical and Computer Engineering (ECE), Professor in ECE with a joint appointment in the School of Materials Science and Engineering (MSE), and Director of the 3D Systems Packaging Research Center (PRC), Georgia Tech (GT). He also serves as the Site Director for the NSF Center for Advanced Electronics through Machine Learning and Theme Leader for Heterogeneous Integration, at the SRC JUMP ASCENT Center. Prior to joining GT, he was with IBM working on packaging for supercomputers.

He is the author of 500+ refereed technical publications and holds 31 patents. He is the primary author and co-editor of 3 books and 5 book chapters, founder and co-founder of two start-up companies, and founder of the IEEE Conference on Electrical Design of Advanced Packaging and Systems (EDAPS), a premier conference sponsored by the IEEE Electronics Packaging Society (EPS). He is an IEEE Fellow and has served as the Distinguished Lecturer for the IEEE Electromagnetic Compatibility (EMC) society. He received his MS and PhD degrees in Electrical Engineering from Syracuse University in 1989 and 1991, respectively.