Design-Technology Co-Optimization / System-Technology Co-Optimization

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Abstract: Lithographic feature scaling pace started to slow down at 10nm node and is expected to stop scaling after 2nm node. Despite that, we see Moore's law continuing at least for the next 10 years with annualized transistor density increase of ~20% and annualized reduction of cost per transistor of ~15%. This progress is enabled by increasingly sophisticated DTCO (Design-Technology Co-Optimization) and STCO (System-Technology Co-Optimization) methodologies. This work illustrates DTCO and STCO methodologies applied to advanced CMOS logic and SRAM to explore and quantify different innovations in design and technology. One illustration is about operating CMOS at cryogenic temperatures. It requires significant reduction (over 300 mV) of threshold voltage, which is challenging for HKMG process, but can provide dramatic improvements in power consumption (close to 10x) or performance (over 40%). Another illustration is about the role of transistor variability as the driving force behind industry transitions from planar MOSFET to FinFET to GAA technologies. Besides these DTCO examples, we apply STCO analysis to 3D heterogeneous integration, which enables additional boost of transistor density and reduction of cost per function, but requires resolving multiple inter-related electrical, thermal, stress, and power delivery challenges. We share design and technology innovations that address these challenges.

Victor Moroz received M.S. degree in Electrical Engineering from Novosibirsk Technical University in Siberia and Ph.D. degree in Applied Physics from the University of Nizhny Novgorod. After engaging in technology development at several semiconductor manufacturing companies and teaching semiconductor physics at the University, Dr. Moroz joined a Stanford spin-off Technology Modeling Associates in 1995.After IPO in 1997, the TMA TCAD team became part of Avanti in 1998, and in 2002 it became a key part of Synopsys, connecting a synthesis company to the manufacturing. Currently Dr. Moroz is a Synopsys Fellow, engaged in a variety of projects on modeling advanced CMOS with over 300 granted and pending US and international patents, and serving as an Editor of IEEE Electron Device Letters.