13th MRAM Global Innovation Forum 2021

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Sessions		Topics	Speakers	
08:45-09:00 Welcome & Introduction (Bernard Dieny and Kevin Garello)				
MRAM in the foundries (chair: Daniel Worledge)	09:00 09:30	Embedded STT-MRAM Development for Frame Buffer Memory Application with CIS-compatible Process	Kilho Lee (Samsung)	
	09:30 10:00	Global Foundries MRAM Solutions for IoT and Industrial Applications	Pedro Pachuca (Global Foundries)	
	10:00 10:30	N16 Embedded MRAM Technology for Reflow Application and Beyond	Yuan-Jen Lee (TSMC)	
10:30-11:00 Break				
MRAM in the Industry (chair: Jordan Katine)	11:00 11:30	Spin-Transfer Torque MRAM Technology For Low-Latency Industrial Applications	Dimitri Houssameddine (Everspin)	
	11:30 12:00	MRAM for IBM Flash Core modules	Brent Yardley (IBM)	
	12:00 12:30	3D stacked CIS compatible 40nm embedded STT-MRAM for buffer memory	Kazuhiro Bessho (Sony)	
12:30-14:00 Break				
Applications and testing (chair: K. Garello)	14:00 14:30	Test architecture addressing MRAM specificities for High Volume Manufacturing	Siamak Salimy (HPROBE)	
	14:30 15:00	Technology transfers into the defense industry: implications for spintronics in the future of national security	Michael Burkland (Raytheon Tech.)	
New spintronic concepts beyond STT (chair: Luc Thomas)	15:00 15:30	Voltage Control of Magnetic Anisotropy for Voltage-Controlled MRAM	Shinji Yuasa (AIST)	
	15:30 16:00	Energy Efficient and Intelligent Processing-In-Memory for Data-Intensive Applications From Device to Algorithm	Deliang Fan (Arizona Uni.)	
	16:00 16:30	Magnetic Tunnel Junctions for Electromagnetic Energy Harvesting and computing	Giovanni Finocchio (Messina Uni.)	
16:30-17:00 Break				
Panel Discussion	17:00 18:00	**Current MRAM wide adoption: what is holding it back?** Moderator: Jack Guedj (Numem) Panelists: Scott Hanson (Ambiq), Zhao Wang (META/Facebook), Thomas Jew (NXP), Nilesh Gharia (Numem), Tetsuo Endoh (Tohoku Uni.)		
18:00 Closing remarks				

Kilho Lee

Principal Engineer,

Samsung Semiconductor

Dr. Kilho Lee is Principal Engineer of Advanced Technology Development Team in Samsung Semiconductor R&D center, leading the development of STT-MRAM products. He has been working on the research of various new memories such as MRAM, PRAM, RRAM and FRAM. He received Ph.D. degree in Materials Science and Engineering from POSTECH (Pohang University of Science and Technology) in South Korea in 2005. He was a post-doctoral researcher in UC Berkeley from 2005 to 2007, studying multiferroic materials. Since he joined Samsung Electronics in 2007, he has contributed to the development of MRAM and PRAM. His specialty is to integrate new memory devices and establish new characterization method and reliability standards

Embedded STT-MRAM Development for Frame Buffer Memory Application with CIS-compatible Process

Unlike conventional memories such as SRAM, eDRAM and eFlash, STT-MRAM covers a wide spectrum of applications. One of the unique and fascinating features of MRAM technology is the systematic tunability of major properties, such as switching current, retention and endurance. From this point of view, we successfully present eMRAM as a frame buffer memory solution for future mobile and wearable applications by developing reliable fast switching property with superior endurance. We demonstrate embedded STT-MRAM fully integrated onto 28nm CIS logic platform, highlighting the world-best macro density of 13.94 Mb/㎟. The macro provides 55% area saving over 28nm SRAM. The MTJ processes are compatible with standard 3D-stacked CIS integration processes that require sufficient 400℃ heat budget. For fast write operation (<50ns) and high endurance property (>1E10 cycles) with 400℃ BEOL compatibility, each ultra-thin magnetic layers have been systematically re-designed. Furthermore, we have confirmed superior scalability of MTJ processes beyond 28nm. With advanced MTJ patterning processes, we have verified that MTJ short failure rate can be suppressed below 1ppm even at a 40% smaller pitch as compared to the current MTJ pitch at 28nm. This result reveals that our frame-buffer STT-MRAM technology is scalable to 14nm FinFET node. These achievements provide a substantial progress of eMRAM towards wide-range applications, and eMRAM solution will provide differentiated benefits with power-saving and low cost.

Pedro Pachuca

Director,

GLOBALFOUNDRIES

Pedro Pachuca is the director of the global microcontroller business line at GLOBALFOUNDRIES, Pedro brings more than 25 years of experience in the semiconductor industry. Prior to GLOBALFOUNDRIES Pedro held multiple business and technical positions at Freescale semiconductor, Silicon laboratories and Renesas electronics, deeply involve in architecture definition of embedded systems with Non-Volatile Memory (eNVM).

Global Foundries MRAM Solutions for IoT and Industrial Applications

With eFlash reaching its economic scaling limit at the 28nm node, MRAM has emerged as the technology of choice to meet AI, IoT, Industrial, and Automotive application requirements. With the increasing functionality and data requirements for today's applications, embedded memory has need to not only demonstrate cost scaling but has also been challenged to improve performance metrics. Memory is being pushed to support very high endurance and excellent retention under harsh environmental conditions while simultaneously increasing memory capacity. The drive towards faster CMOS logic is pushing for improved read/write latencies, and the pervasiveness of mobile processing drives the need to support ultra-low leakage and low power modes. In this session, we will describe how GlobalFoundries is meeting our customer's requirements with production-ready industrial grade MRAM solutions as well as the opportunities and challenges facing MRAM towards empowering the continued development of differentiated, feature-rich products.

Yuan-Jen Lee

Technical Manager,

TSMC

Yuan-Jen Lee is a Technical Manager of MRAM Program at TSMC. He has 16 years of professional experiences in the research and development MRAM. Prior to joining TSMC, he was a Senior Manager in the STT-MRAM team at TDK-Headway Technologies. He received Ph.D. degree in Physics from National Taiwan University in 2003. He has published 30+ MRAM relative papers and holds 20+ issued U.S. patents.

N16 Embedded MRAM Technology for Reflow Application and Beyond

Embedded MRAM (eMRAM) is expected to replace embedded Flash (eFlash) for microcontroller unit (MCU) applications beyond the 28 nm technology node. Compared to eFlash, eMRAM not only excels in write endurance and write speed, it also provides significant cost advantage as fewer masks are required to integrate memory device. This quick process turnaround is also a boon in the current semiconductor chip shortage environment. The N16 solder-reflow-capable eMRAM can operate up to 150°C for automotive grade-1 applications. The memory cell area of the reflow eMRAM is 0.033 um2, a 28% reduction in area versus the 22nm eMRAM cell. While the critical dimension (CD) of MTJ is reduced vs. MTJ in 22nm eMRAM cell, it continues to achieve good data retention and reflow yield. The MTJ film stack is optimized to achieve sufficient read margin and high reliability yield at 150°C.

In addition to the cell optimized for reflow and automotive usage, a high-yielding MRAM cell with 0.018 um2 area is demonstrated on 16nm technology with shorter write time and low write power to support RAM-like applications where MTJ optimization focus on improving write speed and higher memory density compared to SRAM.

Dimitri Houssameddine

Senior Director,

Everspin Technologies

Dimitri Houssameddine is Senior Director of Product Characterization and Reliability at Everspin Technologies, where he focuses on bringing new MRAM products to market. He has extensive experience on STT-MRAM technology development with a focus on product and device characterization. Throughout his career with Everspin, GLOBALFOUNDRIES and IBM, he has been an integral member of teams commercializing STT-MRAM for standalone and embedded applications. Dimitri received his Ph.D. in Physics from Joseph Fourier University, Grenoble, France.

Spin-Transfer Torque MRAM Technology For Low-Latency Industrial Applications

STT-MRAM technology is gaining traction in the market and being used in an increasing number of applications such as for data centers, industrial products, wearable devices, or aerospace. Successful adoption of an emerging memory product requires careful co-optimization of the technology and circuit design. This presentation introduces the next generation of Everspin's MRAM technology optimized for low-latency industrial applications. We will cover the evolution of our technology to address the stringent performance and reliability requirements of the industrial market. We have achieved high speed reliable switching over the full operating temperature range from -40°C to +85°C with data retention of more than 10 years at +105°C and endurance of greater than 1e15 cycles at -40°C. This advanced STT-MRAM technology will be deployed in an upcoming line of Serial Peripheral Interface (SPI) products, delivering the highest performance SPI STT-MRAM on the market.

Brent Yardley

Senior Technical Staff Member,

IBM

Brent Yardley is a Senior Technical Staff Member and Master Inventor with IBM Systems, where he focuses on developing All Flash Arrays (AFAs). Brent is currently the overall Chief Hardware Engineer responsible for the hardware architecture, design, and integration of IBM's storage hardware products and planning future generation storage platforms. He specializes in system designs that integrate multiple I/O protocols, FPGAs, and ASICs, and is an expert in both hardware and software design and system integration. A 21-year veteran of IBM, Brent holds multiple patents focused on storage architectures and solutions. He has an extensive background and understanding of the architecture, design, and implementation of highly available storage-based systems and solutions. He has earned BS degrees in both Software and Hardware Engineering from the Oregon Institute of Technology.

MRAM for IBM FlashCore modules

Solid State Devices (SSDs) are prolific in the all flash array enclosures. Power loss protect for these devices can be implemented in a number of ways. IBM FlashCore Modules has taken a unique approach to this design, by using STT-MRAM as a form of power loss protection media, which allows for the reduction of the total energy needed one when of these events occurs. This presentation covers the use of STT-MRAM in the IBM FlashCore Module to assist in data protection of the device during power loss use cases.

Kazuhiro Bessho

Senior Manager,

SONY

Kazuhiro Bessho is a Senior Manager at Sony Semiconductor Solutions Corporation currently engaged in STT-MRAM development. He joined Sony in 1992 and started the research on analyses of magnetic films

and nanostructures. After studying on GMR/TMR materials at Stanford University in 1996-1997 as a visiting researcher, he launched the development of MRAM at Sony in the early 2000s.

3D stacked CIS compatible 40nm embedded STT-MRAM for buffer memory

STT-MRAM has attracted increasing attention to replace embedded-flash memory and SRAM [1-6] owing to its high-performance operation and CMOS compatible process. Compared with SRAM, STT-MRAM has the advantage of not only achieving non-volatile data retention but also possessing smaller bit cells that enable larger capacity of buffer memory. In this work, we demonstrate a 40nm 30Mbit embedded STT-MRAM for buffer memory, that is compatible with the 3D stacked CMOS image sensor (CIS) process. We optimized a CoFeB-based perpendicular magnetic tunnel junction (p-MTJ) to suppress degradation of the magnetic properties caused by the 3D stacked wafer process. With improved processes, we achieved high speed write operation below 40 ns under typical operation voltage conditions at -30 ℃, endurance up to 1E+10 cycles at 105 ℃ and 1 s data retention at 85 ℃ required for a buffer memory. In addition, to broaden the applications of embedded MRAM (eMRAM), we propose a novel fusion technology integrating embedded non-volatile memory (eNVM) and buffer memory type embedded MRAM on the same chip through p-MTJ size modulation. We achieved a data retention of 1 s to >10 years with a sufficient write margin using the fusion technology.

[1] J.G. Alzate et al., IEDM, 2019, [2] S. H. Han et al., IEDM, 2020
[3] T. Y. Lee et al., IEDM, 2020, [4] V. B. Naik et al., IEDM, 2019
[5] O. Golonzka et al., IEDM, 2018, [6] Yi-Chun Shih et al., IEDM, 2020.

Siamak Salimy

CTO,

HPROBE

Dr. Siamak Salimy is founder and CTO of Hprobe, a company providing Automated Test Equipment (ATE) for High Volume Manufacturing (HVM) of MRAM and magnetic sensor. He has more than 15 years experiences in semiconductor test development and implementation for chip products and device technologies (CMOS, BCD, MEMS sensors, RF-MEMS and Spintronics) dedicated to large scale deployments on both consumers and automotive applications. He is currently leading Hprobe technology and products development. Prior to that, he oversaw back-end test implementation at Delfmems (France) where he released in production a competitive process for RF-MEMS devices targeting mobile phone market. Prior to that he developed advanced BCD/CMOS device technology at Atmel's analog and mixed-signal foundry in France and at the Semiconductor Division of Teledyne Dalsa in Canada, where he also led MEMS inertial sensors test development for mass production. He holds a Ph.D. from the University of Nantes, and he is Engineer from Polytech Nantes School of Engineering.

Test architecture addressing MRAM specificities for High Volume Manufacturing

Replacement of transistor-based memories by MRAM is on the way of being proven with the recent commercial introduction of Spin Transfer Torque (STT)-MRAM for eFlash applications at 22nm and 28nm technological nodes. The promising next steps for MRAM in the coming years are to overcome SRAM issues on power consumption and integration density at single digit technological nodes. Since MRAM are introduced at back-end-of-line (BEOL), excelling on process control and yield performances are crucial for High Volume Manufacturing (HVM) as the largest part of the manufacturing process is already executed when building the MTJ, including the front end of line (FEOL) most expensive steps. Indeed, when the wafer is ready to be tested with BEOL MTJs, the fab process cost ratio is at 70-90% of the final chip cost. Therefore, accurate metrics to determine "good die" or fabrication issues are essential to secure the remaining test and assembly process cost. The designed test flow of eMRAM chip should be at the same time cost efficient (high throughput) and consider STT-MRAM specificities at each test stages (MTJ, arrays and chip). Hence, a metrology flow smartly designed at the utmost with consideration of the Magnetic Tunnel Junctions (MTJ) and writing mechanisms physics involved (STT, SOT…) are key to ensure that chip product meet the target specifications.

Even though STT-MRAM use in final product is purely electrical, the stored information is magnetic and the programming (state switching of the MTJ) can be triggered from electrical current, temperature or magnetic field. Because of this, magnetic and temperature simultaneously used during electrical test are introduced at the Wafer Acceptance Test (WAT), Wafer Sort (WS) and Final Test (FT) to establish secured foundation to support STT-MRAM ramp-up in HVM. In this presentation, I will discuss the testing requirements for HVM of STT-MRAM in the back end and assembly process and analysis the test architectures compared to traditional purely electrical 'CMOS like' manufacturing processes. I will present state of the art solutions test cases of WAT and WS, and envisioned solutions by Hprobe to improve testing speed.

Michael Burkland

RMD JUMP Liaison,

Raytheon Technologies

Mike Burkland has been with Raytheon in Tucson, AZ since 1999. He currently facilitates the identification and creation of technologies to support innovative solutions for Raytheon Missiles & Defense business needs. A primary focus is directing development of advanced microelectronics technologies through Raytheon's participation in the Semiconductor Research Corporation JUMP and nCORE university research programs. From Purdue University Mike earned a bachelor's degree in physics and mathematics, and a Ph.D in physics with a minor in quantum optics from the University of Arizona.

Since 2015 Mike has represented Raytheon in SRC research, first in the STARnet program and continuing into JUMP and nCORE. From this history of engagement, a number of DARPA contracts have been awarded to Raytheon in partnership with academic researchers for further maturation of SRC research products. Over the course of his career, Mike has authored over ten patents and has publications spanning research in Meteoritics to Electro-Optics.

Technology transfers into the defense industry: implications for spintronics in the future of national security

President Eisenhower, in his 1961 farewell address to the nation, warned "against the unwarranted influence, whether sought or unsought, by the Military-Industrial Complex." The concern of excessive government spending on defense continues to be a contentious issue today. However, coupled with President Kennedy's plan to put a (US) man on the moon, government investment in microelectronics continued through the 1980's and helped position the United States as the only super power to emerge from the Cold War – with the defense and aerospace industries driving innovation.

By mid-1990 the tide had shifted with commercial electronics as the market driver of design and applications. In 2014, William Lynn III, the former Deputy of Defense, wrote of "The End of the Military-Industrial Complex," emphasizing the need of the defense industry to work with, and incorporate from, the commercial sector [1].

While the collaboration of the Defense Industrial Base (DIB) with the domestic commercial microelectronics sector has been sufficient to meet the demand, the cost and time of development of advanced microelectronics has dramatically increased while the supply from domestic foundries has become limited with industry consolidation. Additionally, the time delay in adoption of new technologies into defense products can take a decade or more, governed by a prescribed maturation process utilized within the industry, the Technology Readiness Level (TRL) scale. The rate limiting processes within the TRL lifetime are usually paced by qualification, the degree of disruption to existing systems of adoption, as well as the establishment of a reliable and affordable supply chain.

The hopeful light at the end of the tunnel may be with the development of low temperature Back-End-Of the Line (BEOL) fabrication of novel memory and logic technologies; specifically vertical CMOS and beyond CMOS devices, with lower fabrication cost. For instance, non von Neumann architectures are being investigated using STT-RAM for high throughput, low energy and latency processing [2]. However, further opportunities emerging from domestic research, such as university research sponsored by the Semiconductor Research Corporation [3], can only be transferable by a robust industrial base supporting successful rapid prototyping and sustained production. Cognizant of these issues, the United States has recently increased investment in on-shore advanced microelectronics development and manufacturing via the recently passed $52B CHIPS Act. Thus, a pivot by existing commercial microelectronics suppliers, especially those with magnetic-based device fabrication, in support of low volume (compared to commercial) specialized BEOL microelectronics in the near-term would provide for emerging defense needs while laying a foundation for a larger commercial market demand anticipated in the coming five to ten years [3]. As well, opportunities for emerging spintronic-based suppliers could address a market segment of TRL 4-6 range of near-term DIB development needs.

[1] W. J. Lynn III, "The End of the Military-Industrial Complex", Foreign Affairs Magn., Nov/Dec (2014).

[2] K. Kim et al., "MRAM-based Deep In-memory Architectures", GOMACTech21, (2021).

[3] J. Neuffrer et al., "Decadal Plan for Semiconductors", Semiconductor Research Corp., (2021).

Shinji Yuasa

Professor,

AIST

Shinji Yuasa received a PhD in Physics from Keio University (Yokohama, Japan) in 1996. After receiving his doctorate, he served as a staff scientist at the National Institute of Advanced Industrial Science and Technology (AIST). Since 2010, he has been a Director of research center at AIST and a Professor at University of Tsukuba. Since 2000, he has been studying thin film magnetism and spintronics, more specifically the tunnel magnetoresistance (TMR) effect and spin-transfer torque (STT) in magnetic tunnel junctions (MTJs) and their applications to various devices such as magnetic

sensors and magnetoresistive random-access-memory (MRAM). His most important scientific achievements are the development of MgO-based MTJs including CoFeB/MgO/CoFeB-type MTJs and their applications to read heads of hard disk drives and STT-MRAM. For his pioneering contributions to the MgO-based MTJs, he has been awarded or co-awarded more than 20 awards and prizes, including the Asahi Award in 2008 and IEEE Fellow in 2021.

Voltage Control of Magnetic Anisotropy for Voltage-Controlled MRAM

Giant tunnel magnetoresistance (TMR) effect and spin-transfer torque (STT) in MgO-based magnetic tunnel junctions (MTJs) are the key technologies in magnetoresistive random access memory (MRAM) [1]. STT-MRAM has been commercialized as embedded non-volatile memory for system LSI. For MRAM to replace SRAM, however, MRAM needs to have higher speed and lower energy consumption for writing. For developing such advanced MRAM, we have been working on new writing technology as well as MTJs with materials. Voltage-induced dynamic switching based on voltage control of magnetic anisotropy (VCMA) is expected to be an ultimate writing technology with ultra-low power consumption. By doping 5d elements into Fe electrode of MgO-based MTJ, we have achieved very high VCMA coefficient (>300 fJ/Vm) [2], which is sufficient for cache memory application. The biggest remaining issue for developing novel voltage-controlled MRAM (VC-MRAM) is the high write error rate (WER) of the dynamic switching [3]. By controlling the spin dynamics induced by ultra-fast voltage pulses, we have successfully suppressed WER below 10-6 [3-6], which is sufficiently low for some applications. Aiming at more reliable voltage-induced switching, we have also been working on new writing methods based on VCMA [7,8]. In our talk, we will review recent progress on VCMA and discuss perspectives of VC-MRAM.

[1] S. Yuasa, K. Hono, G. Hu, D. C. Worledge, MRS Bulletin 43, 352 (2018), [2] T. Nozaki et al., NPG Asia Materials 9, e451 (2017), [3] T. Nozaki et al., Micromachines 10, 327 (2019), [4] T. Ikeura et al., Jpn. J. Appl. Phys. 57, 040311 (2018), [5] T. Yamamoto et al., Phys. Rev. Appl. 11, 014013 (2019), [6] T. Yamamoto et al., J. Phys. D: Appl. Phys. 52, 164001 (2019), [7] T. Yamamoto et al., Nano Letters 20, 6012 (2020), [8] R. Matsumoto et al., Appl. Phys. Express 12, 053003 (2019).

Deliang Fan

Assistant Professor,

Arizona State University

Dr. Deliang Fan is currently an Assistant Professor in the School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ, USA. Before joining ASU in 2019, he was an assistant professor in Department of Electrical and Computer Engineering at University of Central Florida, Orlando, FL, USA. He received his M.S. and Ph.D. degrees, under the supervision of Prof. Kaushik Roy, in Electrical and Computer Engineering from Purdue University, West Lafayette, IN, USA, in 2012 and 2015, respectively.

Dr. Fan's primary research interest includes Energy Efficient and High Performance Processing-In-Memory Circuit, Architecture and Algorithm cross-layer software & hardware co-design, with applications in Deep Neural Network, Data Encryption, Graph Processing and Bioinformatics; Hardware-aware deep learning optimization; Adversarial AI security; Brain-inspired (Neuromorphic) Computing. He has authored and co-authored 130+ peer-reviewed international journal/conference papers in above area. He is the receipt of best paper award of 2019 ACM Great Lakes Symposium on VLSI, 2018 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), and 2017 IEEE ISVLSI. His research paper was also nominated as best paper candidate of 2021 Design Automation Conference (DAC), 2019 Asia and South Pacific Design Automation Conference and 2019 International Symposium on Quality Electronic Design (ISQED). He is also the technical area chair of DAC 2021, GLSVLSI 2019/2020/2021, ISQED 2019/2020/2021, and the financial chair of ISVLSI 2019. He served as technical reviewers for over 30 international journals/conferences, such as Nature Electronics, IEEE TNNLS, TVLSI, TCAD, TNANO, TC, TCAS, etc. He also served as the Technical Program Committee member of DAC, ICCAD, HPCA, MICRO, WACV, GLSVLSI, ISVLSI, ASP-DAC, etc. Please refer to https://dfan.engineering.asu.edu/ for more details.

Energy Efficient and Intelligent Processing-In-Memory for Data-Intensive Applications - From Device to Algorithm

In-memory computing is becoming a promising solution to overcome the well-known 'memory-wall' challenge, through directly processing the data within memory where data is stored. Therefore, it will reduce massive power hungry data traffic between computing and memory units, leading to significant improvement of entire system performance and energy efficiency. Many different memory technologies have been explored for the design of processing-in-memory (PIM) or in-memory computing (IMC), such as emerging post-CMOS Magnetic Random Access Memory (MRAM), Static Random Access Memory (SRAM) or Dynamic RAM (DRAM), etc. In this talk, Prof. Deliang Fan, from Arizona State University (ASU), will present his recent research in energy efficient and intelligent cross-layer processing-in-memory design for data-intensive applications, spanning from MRAM memory device &circuit to in-

memory computing architecture & algorithm co-optimization, to intrinsically integrate memory and processing units. In this talk, Dr. Fan will present the software-hardware co-design of PIM for different data-intensive applications, including deep neural network, data encryption, graph processing and bioinformatics.

Giovanny Finnocchio

Professor,

Messina University

Giovanni Finocchio received the Ph.D. degree in advanced technologies in optoelectronic, photonic and micromagnetic modeling from the University of Messina, Italy, in 2006. Since 2010, he is now Associate professor now with the Department of Mathematical and Computer Sciences, Physical Sciences and Earth Sciences at the University of Messina. He is director of the laboratory PETASPIN (Petascale computing and Spintronics). His research interests include spintronics, skyrmions, and computing (https://scholar.google.co.uk/citations?user=eKDbn-oAAAAJ&hl=en). In the last 10 years, he served on many technical program committees of international conferences and organized more than 10 international conferences and workshops as Chair, Program Committee Member, or in other positions. He is regularly invited at conferences in Magnetism and Spintronics. He is also president of Petaspin association (www.petaspin.com), chair of the IEEE Magnetics Italy chapter, AdCOM member of the IEEE Magnetics society and chair of the TC-16 on Quantum, neuromorphic and unconventional computing of the IEEE Nanotechnology council.

Magnetic Tunnel Junctions for Electromagnetic Energy Harvesting and computing

The spintronic technology takes advantage of the manipulation of the electron spin together with its charge. This technology potentially combines important characteristics such as ultralow power needs, compactness (nanoscale size) and it is CMOS-compatible. Microwave detectors based on the spin-torque diode effect are among the key emerging spintronic devices. Those devices realized with magnetic tunnel junctions working in active regime exhibit high-detection sensitivity >200kV/W at room temperature, without any external bias fields, and for low-input power (micro-Watts or lower), [1] [2] value which can reach more than 1MV/W in presence of field and an additional bolometric effect. [3] On the other hand, when working in passive regime those devices can be used as electromagnetic energy harvesting. We have shown that those devices can exhibit resonant rectification at sub-nW power working at input power smaller than the one used for Schottky diodes. However, from a technological point of view one wish a broadband response for energy harvesting in order to collect energy from different source. In our recent work, we have experimentally demonstrated that this broadband detection can be achieved by exciting nonlinear dynamics, i.e. large amplitude magnetization precession. In particular, this has been achieved with a bias-field-free spin-torque diodes having a canted magnetization in the free layer as equilibrium state. We have shown an efficient harvester of broadband ambient RF radiation to power a black phosphorous nanodevice. [4] Recently, it has been also shown that those devices when connected in series can supply also a LED. [5] I will also discuss briefly how the frequency response of spin-torque diodes and their current tunability can be also used as building blocks of the hardware realization of neurons and synapses in neuromorphic applications and fort hardware implementation of analog multiplication. In the last part of the talk, I will show potential implementations of THz detectors based on antiferromagnets which can be used as wake-up receiver. [6]

[1] B. Fang et. al, *Giant Spin-Torque Diode Sensitivity in the Absence of Bias Magnetic Field*, Nat. Commun. 7, (2016),

[2] L. Zhang et. al, *Ultrahigh Detection Sensitivity Exceeding 10 5 V/W in Spin-Torque Diode*, Appl. Phys. Lett. 113, 102401 (2018), [3] M. Goto et. al, *Uncooled Sub-GHz Spin Bolometer Driven by Auto-Oscillation*, Nat. Commun. 2021 121 12, 1 (2021),

[4] B. Fang et. al, *Experimental Demonstration of Spintronic Broadband Microwave Detectors and Their Capability for Powering Nanodevices*, Phys. Rev. Appl. 11, 014022 (2019),

[5] R. Sharma et. al, *Electrically Connected Spin-Torque Oscillators Array for 2.4 GHz WiFi Band Transmission and Energy Harvesting*, Nat. Commun. 2021 121 12, 1 (2021),

[6] A. Safin et. al, *Electrically Tunable Detector of THz-Frequency Signals Based on an Antiferromagnet*, Appl. Phys. Lett. 117, 222411 (2020).

PANEL DISCUSSION:

Current MRAM wide adoption: what is holding it back?

Moderator: Jack Guedj (CEO, Numem)

Panelists:

Scott Hanson

Chief Technology Officer,

Ambiq

Scott Hanson is the Chief Technology Officer and founder of Ambiq. Scott invented SPOT, Ambiq's core sub-threshold technology platform, to enable the world's most energy-efficient chips during his PhD studies at the University of Michigan. He founded

Ambiq in 2010 and led the development of the world record-setting Apollo, Ambiq's first flagship processor. Under Scott's leadership, Ambiq has shipped more than 100 million chips to the world's top brands and has grown into the global leader in ultra-low power solutions.
In addition to his role as CTO, he has variously played roles leading product definition and development, managing production test, and, most importantly, spending a great deal of time with customers to understand their needs and their vision. As a widely recognized innovator in low power circuits, Scott today leads the development of Ambiq's technology roadmap.
Scott's pioneering work in sub-threshold design and picowatt processors has been widely published, with more than 30 leading publications, more than 20 patents on related technology, and a wide variety of speaking engagements. Scott's work was honored by the University of Michigan with the 2014 Arbor Networks PhD Research Impact Award and the 2020 ECE Alumni Rising Star Award and was honored by Ernst & Young as an Entrepreneur of the Year 2020 finalist.

Zhao Wang

Research scientist

META/Facebook

Dr. Wang received his PhD in Electrical Engineering from University of Texas at Dallas in 2012. He has worked in TI, Qualcomm, Apple, TSMC and Facebook in different areas of custom chips design. Currently he is a research scientist and chip lead in camera sensor research group in Meta RL research. His current research interests include computing in memory, non-volatile memory applications, novel sensor chip architectures etc.

Thomas Jews

CTO,

NXP

Thomas Jew is a Fellow in NXP's CTO, Front End Innovation group and currently leads Non-Volatile Memory development for Advanced Microcontroller and Microprocessor applications. He has worked on discrete non-volatile memory products and embedded memory designs including traditional flash and disruptive memory technologies integrated in microcontrollers for IOT and automotive applications for ~29 years. Prior to joining NXP by way of Freescale Semiconductor/Morotola, he worked for Texas Instruments, designing discrete flash memories. Thomas received his BS and MS degrees in Electrical Engineering from Texas A&M University in 1988 and 1991 respectively.

Nilesh Gharia

CTO,

Numem

Nilesh has 20+ years of experience in the semiconductor industry with a diverse background in semiconductor design and product development. Nilesh was part of the startup team at NetLogic Microsystems which went IPO in 2004, and was later acquired by Broadcom in 2012 for $3.7B, which in turn was acquired by Avago in 2016 for $37B. He was also the 1st Engineer at Lanstar Semiconductor, which also went IPO. Nilesh worked in Virtual Silicon Technology, and was responsible for team development and product design. His expertise includes startups, emerging memories, memory compiler development, MRAM technologies, semiconductor IP development, network processors, and team/project management. Nilesh holds a Masters in Electrical Engineering from the New Jersey Institute of Technology and has a portfolio of 13 US issued patents.

Testuo Endho

Professor,

Tohoku University

Tetsuo Endoh joined ULSI Research Center Toshiba Co. in 1987 and was engaged in the R&D of NAND Memory. He became a lecturer at the Research Institute of Electrical Communication, Tohoku University in 1995. He is a professor at the Department of Electrical Engineering, the Graduate School of Engineering, Tohoku University and director of the Center for Innovative Integrated Electronic Systems (CIES). His current interests are novel 3D structured device technology, such as Vertical MOSFETs; high-density memory, such as SRAM, DRAM, 3D-NAND memory and STT-MRAM; and beyond-CMOS technology, such as spintronics-based non-volatile Logic for ultralow power systems such as mobile systems, AI systems and IoT systems. He is also interested in power-management technology, such as GaN on Si based power devices and power integrated circuits with low energy loss and low power consumption for automotive applications. He received the 14th Prime Minister's Award for his Contribution to Industry-Academia-Government Collaboration in 2016.
He received 2017 National Invention Award "the 21st century Encouragement of Invention Prize" on June 12th for his contribution of the invent of 3D-NAND Memory technology.

13th MRAM Global Innovation Forum

San Francisco, 16 December 2021

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