Session 1: Plenary
Monday, December 5, 9:00 AM
Grand Ballroom B
Co-Chairs: Barbara DeSalvo, Facebook
Dina Triyoso, TEL Technology Center, America, LLC

1.1 Celebrating 75 years of transistor innovation by looking ahead to the next set of industry grand challenges (Invited), Ann Kelleher, Executive Vice President and General Manager of Technology Development, Intel

1.2 Expanding Human Potential through Imaging and Sensing Technologies (Invited), Yusuke Oike, General Manager, Sony Semiconductor

1.3 Enabling full fault tolerant quantum computing with silicon based VLSI technologies (Invited), Maud Vinet, Quantum Hardware Program Manager, CEA Leti

Session 2: EDT - Neuromorphic and In-Memory Compute Technologies
Monday, December 5, 1:30 p.m.
Grand Ballroom A
Co-Chairs: Han Wang, TSMC
Eric Vogel, Georgia Tech

1:35 p.m.
2.1 Novel a-IGZO Anti-Ferroelectric FET LIF Neuron with Co-Integrated Ferroelectric FET Synapse for Spiking Neural Networks, C. Sun, X. Wang, H. Xu, J. Zhang, Z. Zheng, Q. Kong, Y. Kang, K. Han, L. Jiao, Z. Zhou, Y. Chen, Z. Dong, G. Liu, L. Liu, X. Gong, National University of Singapore

A novel amorphous-Indium-Gallium-Zinc-Oxide (*a*-IGZO) anti-ferroelectric field-effect transistor (AFeFET)-based leaky integrate-and-fire (LIF) neuron is experimentally demonstrated, emulating both excitatory and inhibitory input connections with capacitor-free neuron design. By co-integrating (*a*-IGZO) ferroelectric field-effect transistors (FeFETs) as synapses, spiking neural networks (SNNs) with high biomimetic and low hardware costs could be implemented.

2:00 p.m.
2.2 Highly Scalable (30 nm) and Ultra-low-energy (~ 5 fJ/pulse) Vertical Sensing ECRAM with Ideal Synaptic Characteristics Using Ion-permeable Graphene Electrodes, J. Lee, R. Nikam, D. Kim, H. Hwang, Pohang University of Science and Technology

We demonstrated a vertical sensing Electro-Chemical Random-Access Memory with excellent synaptic behaviors using ion-permeable graphene electrodes. By utilizing a vertical channel structure ($4F^2$ of cell layout), ideal synaptic behavior was confirmed in a 30×30 nm^2 device with improved read latency and ultra-low energy consumption (~ 5 fJ/pulse).

2:25 p.m.
2.3 Experimental Demonstration of High-order In-memory Computing based on IGZO Charge Trapping RAM Array for Polynomial Regression Acceleration, L. Bao, Z. Wang*, Y. Shi**, Y. Ling, Y. Yang, L. Shan, S. Bao, C. Wang*, Q. Zheng, J. Kim**, H. Hosono**, Y. Cai, R. Huang*, Peking University, *also with Beijing Advanced Innovation Center for Integrated Circuits, **Tokyo Institute of Technology

We demonstrate a novel IGZO-based CT-RAM that can accomplish ternary computation by utilizing inherent non-linear dynamics. Excellent analog transconductance modulation (> 64 levels) enables first-order linear and second-order quadratic drain responses. A complementary CT-RAM array is proposed and experimentally demonstrated to implement polynomial regression computation engines with reduced hardware overhead.

3:15 p.m.
2.4 Application-Hardware Co-Design: System-Level Optimization of Neuromorphic Computers with Neuromorphic Devices (Invited), C. Schuman, J. Plank, G. Rose, University of Tennessee

The design of neuromorphic computers offers the opportunity to innovate across the entire compute stack, from materials and devices, to algorithms and applications. Here, we provide a discussion of challenges associated with full-stack co-design and how we have addressed those challenges with a few use cases for particular neuromorphic devices.

3:40 p.m.
2.5 Demonstration of Analog Compute-In-Memory Using the Charge-Trap Transistor in 22 FDX Technology, S. Qiao, S. Moran, D. Srinivas, S. Pamarti, and S.S. Iyer University of California Los Angeles

We demonstrate a 4-ENOB analog CIM based on the CTT using 22 FDX technology. The CTT has 10^{11} off-state resistance and 10^5 on-off ratio, and exhibits <2% VMM error with negligible retention loss up to 85°C. Weights can be accurately programmed within 3% of target.

4:05 p.m.
2.6 Dynamics of PSG-Based Nanosecond Protonic Programmable Resistors for Analog Deep Learning, M. Onen, J. Li, B. Yildiz, and J. A. del Alamo, Massachusetts Institute of Technology

We present the real-time dynamics of a new class of CMOS- and BEOL-compatible nanoscale protonic programmable resistors based on PSG electrolyte for energy-efficient analog deep-learning hardware accelerators. Results show impulse-like non-volatile conductance modulation with nanosecond-range pulses, reveal the detailed physics of proton transport, and provide guidance for future optimization.

4:30 p.m.
2.7 BEOL-Compatible High-Performance a-IGZO Transistors with Record high Ids,max = 1207 μA/μm and on-off ratio exceeding 10^{11} at V_{ds} = 1V, Q. Li, C. Gu*, S. Zhu*, Q. Hu, W. Zhao*, X. Li*, R. Huang, Y. Wu, Peking University, *Huazhong University of Science and Technology

We demonstrated high-performance a-IGZO TFTs with optimized ITO interlayer contact. 60 nm long IGZO transistor shows a record low R_c of 278 Ω×mm, high I_{on} of 1207 μA/μm and g_m of 637 μS/μm with a high on-off ratio above 10^{11} providing the best performance among short channel IGZO transistors.

Session 3: ALT – Focus Session - Advanced Heterogeneous Integration: Chiplets and System-in-Packaging
Monday, December 5, 1:30 p.m.
Grand Ballroom B
Co-Chairs: Chih-Hao Chang, TSMC
Xiao Gong, National University of Singapore

1:35 p.m.
3.1 Advanced System in Package Enabled by Wafer Level Heterogeneous Integration of Chiplets(Invited), S. Bhattacharya, T. G. Lim, D. Ho, K. J. Chui, X. W. Zhang, M. D. Rotaru, B. G. Sajay,

T. C. Chai, S. C. Chong, H. Y. Li, S. Lim, X. Y. Wang, M. C. Jong, V. N. Sekhar, R. Dutta, Vempati S. Rao, Institute of Microelectronicx, A*Star

Wafer level Heterogeneous Integration (HI) has allowed the semiconductor industry to continue packing increasing functionality into power-performance-form factor-cost (PPFC) optimized advanced System in package (SiP) in 5G/AI-ML/DC/Automotive applications. This paper presents overview of our advanced SiP solutions to address the challenges of current and next generation semiconductor systems.

2:00 p.m.
3.2 Heterogeneous and Chiplet Integration Using Organic Interposer (CoWoS-R) (Invited), S-P Jeng, M. Liu, TSMC

Interposer technology is successfully adopted for heterogeneous and chiplet integration because of its advantages in electrical performance, warpage control, yield and reliability. Organic interposer (CoWoS-R) technology is a new integration interposer platforms, providing low RC interconnect with good signal isolation and design scalability.

2:25 p.m.
3.3 Advanced Packaging Technology Platforms for Chiplets and Heterogeneous Integration (Invited), L. Cao, ASE (US) Inc

A series of RDL based ViPack solutions have been introduced for chiplets and heterogeneous integration to meet market demands. These include Fan-Out Chip-on Substrate (FOCoS), FOCoS embedded Bridge and FO PoP. The electrical performance, warpage and reliability validation for chiplets integration among different FOCoS solutions are presented in this paper.

3:15 p.m.
3.4 Advanced Substrate Packaging Technologies for Enabling Heterogeneous Integration (HI) Applications (Invited), G. Duan, Y. Kanaoka, R. McRee, Y. Li, M. L. Liu, H. S. Yeon, J. Jones, H. Tanaka, A. May, R. Ranjan, O. Ozkan, A. Lehaf, S. Cho, J. Zhang, R. Manepalli, R. Mahajan, H. Azimi, Intel Corporation

With significantly rising demand in high performance computing (HPC), HI has become a crucial performance enabler in the microelectronics industry by providing the flexibility of die disaggregation, and the ability to mix/match different IP blocks optimized on different Si nodes in a single package. The key focus in HI scaling has been to push interconnect density with increased bandwidth and improved power efficiency. In this paper, we share the recent progress on Embedded Multi-Interconnect Bridge (EMIB) technology bump pitch scaling and discuss key considerations for advanced substrate packaging technologies to enable heterogeneous integration applications.

3:40 p.m.
3.5 Hybrid Substrates for Chiplet Design and Heterogeneous Integration Packaging (Invited), J. H. Lau, G. Chen, C. Yang, A. Peng, J. Huang, C. Peng, C. Ko, H. Yang, Y. Chen, and T. Tseng, Unimicron Technology Corporation

The fan-out panel-level chip-last method for chiplet design and heterogeneous integration packaging is presented. Emphasis is placed on the design, materials, process, fabrication and reliability of: (a) heterogeneous integration of chips; (b) fine metal redistribution-layer (RDL)-substrates, (c) hybrid substrates, and (d) chips to hybrid substrate bonding and underfilling.

4:05 p.m.
3.6 Advanced Package FAB Solutions (APFS) for Chiplet Integration (Invited), Seung Wook Yoon, Samsung Electronics Corp.

Advanced Package FAB Solutions (APFS) will be introduced and discussed in terms of challenges and opportunities for emerging high-end computing as chiplet and heterogeneous integration such as 2.5D and 3D, Fanout PKG, and Integrated Stacked Capacitor (ISC).

Session 4: MAT - Devices for Emerging RF Applications
Monday, December 5, 1:30 p.m.
Continental Ballroom 1-3
Co-Chairs: Grace Xing, Cornell University
Kim Sanghyeon, KAIST

1:35 p.m.
4.1 Thermally Resilient Microwave Switch and Power Limiter based on Insulator-Metal Transition of Lanthanum Cobalt Oxide, R. Bhattacharya, A. Khanna*, B. Bosworth***, N. Orloff***, V. Gambin*, D. Streit, P. Fay**, and S. Datta**, University of California Los Angeles, *Northrop Grumman, **University of Notre Dame, ***National Institute of Standards and Technology

A microwave switch and shunt power limiter based on $LaCoO_3$ is demonstrated for the first time. The limiter achieves power limiting over the broadest temperature range ever reported for an insulator-to-metal transition (IMT) based device, from 25°C to 125°C. We additionally present a three-dimensional simulation that accurately predicts device performance.

2:00 p.m.
4.2 Scaling Surface Acoustic Wave Filters on LNOI Platform for 5G Bands, R. Su, S. Fu, Z. Lu*, J. Shen, H. Xu, P. Liu, Z. Xu*, H. Wang**, S. Zhang**, R. Wang, C. Song, F. Zeng, W. Wang***, F. Pan, Tsinghua University, *Southeast University, **Jiangnan University, ***SHOULDER Electronics Limited

We demonstrate SAW filters for 5G bands through LNOI platform. 3.8 GHz resonator simultaneously possesses large (K^2) of 24.1% and high (Qmax) of 2987. Filters over 3.5 GHz were realized, and the fractional bandwidth reaches 28.2% and 20.4%, which meets the requirement of n77 and n78 full band.

2:25 p.m.
4.3 First Demonstration of BEOL-Compatible Ultrathin Atomic-Layer-Deposited InZnO Transistors with GHz Operation and Record High Bias-Stress Stability, D. Zheng, A. Charnas, J. Anderson, H. Dou, Z. Hu, Z. Lin, Z. Zhang, J. Zhang, P.-Y. Liao, M. Si, H. Wang, D. Weinstein and P. D. Ye, Purdue University, Purdue University, Purdue University, Purdue University, Purdue University

This work reports for the first time ultrathin atomic-layer-deposited InZnO as a novel back-end-of-line transistor with GHz operation and record-high bias-stability. 3.5-nm-thick, 100-nm-channel-length InZnO transistors can achieve excellent 65 mV/dec SS, ~10^{11} on-off-ratio, and ~1.33 A/mm on-current (V_{DS}=1 V), surprising high PBS stability (ΔV_T = -16mV @V_{Bias}=3.5 V for 1500s).

3:15 p.m.
4.4 Resonant Tunneling Diode Technology for Future Terahertz Applications (Invited), S. Suzuki, Tokyo Institute of Technology

In the beyond 5G system, the terahertz (THz) band will be used for high data rate communication and sensing applications. Oscillators using resonant tunneling diodes (RTDs) are a candidate of THz sources and suitable for these applications. In this paper, recent developments of RTD oscillators are reported.

3:40 p.m.
4.5 3D Stackable Cryogenic InGaAs HEMT-Based DC and RF Multiplexer/Demultiplexer for Large-Scale Quantum Computing, J. Jeong, S. Kwang Kim, J. Kim*, J. Lee**, J. Pyo Kim, B. Ho Kim, Y-J Suh, D-M Geum, S-Y Park**, S. Kim, Korea Advanced Institute of Science and Technology (KAIST), *Korea Advanced Nano Fab Center (KANC), **Korea Basic Science Institute (KBSI)

We demonstrate 3D stackable cryogenic LNA-oriented InGaAs HEMTs and InGaAs HEMT-based multiplexer/demultiplexer for RF and DC signal routing. Our devices show the record-high faverage of 497 GHz with the smallest power consumption ever reported in cryogenic RF transistors. In addition, the 3D stackable multiplexer/demultiplexer exhibit excellent routing capabilities at 5K.

4:05 p.m.
4.6 Cryogenic InGaAs HEMT-Based Switches For Quantum Signal Routing, A. Ferraris, E. Cha, P. Mueller, T. Morf, M. Prathapan, M. Sousa, H.-C. Han*, C. Enz* , C. B. Zota, IBM Research, *École polytechnique fédérale de Lausanne

We demonstrate cryogenic switching devices based on HEMT technology for quantum computer (QC) signals that exhibit attractive performance with cryogenic subthreshold swing of ~5 mV/decade. The results indicate that HEMT-based switching circuits could offer advantages over standard CMOS at cryogenic temperatures for future integrated low-power QC signal routing applications.

Session 5: RSD - Reliability of Memory Technologies and Systems
Monday, December 5, 1:30 p.m.
Continental Ballroom 4
Co-Chairs: Carmine Miccoli, Micron Technology
Marina Yamaguchi, KIOXIA

1:35 p.m.
5.1 Understanding the Cycling-Dependent Threshold Voltage Instability in OTS Devices, M. Yamaguchi*, R. Degraeve, D. Garbin, S. Clima, T. Ravsher**, D. Matsubayashi*, T. Tsukamoto, R. Delhougne, L. Goux, Gouri S. Kar, imec, *KULeuven,** KIOXIA Corporation

We bring new understanding to reliability of SiGeAsTe-based OTS devices: the impact of cycling stress on (Vth) relaxation. (Vth) relaxation becomes faster after cycling. We clarified the mechanism on the basis of an extended defect model. We propose the driving force and the improvement guideline through the detailed electrical characterization.

2:00 p.m.
5.2 Systematic multiple filament statistical methodology using a successive varying-voltage technique for series resistance effect in post-breakdown (forming) characterization, E. Y. Wu, B. Li, T. Ando, IBM

A successive varying-voltage stress methodology is developed to investigate multiple BD (or filaments) statistics for realistic applications where series resistance can play an important role in the post-BD regime. This methodology is generic for any dielectrics or thickness range and most relevant for on-chip decoupling capacitor applications and ReRAM devices.

2:25 p.m.
5.3 Reliability of Computing-In-Memory Concepts Based on Memristive Arrays (Invited), D. J. Wouters, L. Brackmann, A. Jafari*, C. Bengel, M. Mayahinia*, R. Waser, S. Menzel**, M. Tahoori*, RWTH Aachen, *Karlsruhe Institute of Technology, **Forschungszentrum Juelich

Memristive Computing-in-Memory (CIM) allows for very dense and fast parallel data processing. Operation variability and inherent memristive device variabilities are currently limiting the computing correctness. We review the current situation of reliability studies in memristive CIM and propose a novel framework for estimating operation failures in VCM-ReRAM based CIM-concepts.

2:50 p.m.
5.4 Design Guidelines of Thermally Stable Hafnia Ferroelectrics for the Fabrication of 3D Memory Devices, G. Kim, H. Shin, T. Eom, M. Jung, T. Kim, S. Lee, M. Kim, Y. Jeong, J-S Kim*, K-J Nam*, B. J. Kuh*, S. Jeon, Korea Advanced Institute of Science and Technology, *Samsung Electronics

In this work, We reveal the origins for the thermal instability of hafnia ferroelectric (FE) materials in kinetics and material science aspects. Additionally, to improve the thermal stability of hafnia FE materials, we propose a viable alternative, adopting dopants with a relatively small ionic radius in the FE matrix.

3:40 p.m.
5.5 Retention Improvement in Vertical NAND Flash Memory Using 1-bit Soft Erase Scheme and its Effects on Neural Networks, S.-H. Park, D. Kwon, H-N Yoo, J-W Back, J. Hwang, Y. Yang*, J-J Kim, J-H Lee, Seoul National University, *SK Hynix

We propose a selective 1-bit soft erase scheme in vertical NAND (V-NAND) flash memory that improves retention characteristics. Compared to conventional methods, the proposed method improves retention characteristics by ~40% and the distribution of (Vth) is narrowed to less than 30%.

Session 6: MT - Ferroelectric Memory
Monday, December 5, 1:30 p.m.
Continental Ballroom 5
Co-Chairs: Sou-Chi Chang, Intel
Sven Beyer, GlobalFoundries

1:35 p.m.
6.1 First Demonstration of Ultra-low D_{it} Top-Gated Ferroelectric Oxide-Semiconductor Memtransistor with Record Performance by Channel Defect Self-Compensation Effect for BEOL-Compatible Non-Volatile Logic Switch, CK Chen, Z. Fang, S. Hooda, M. Lal, U. Chand, Z. Xu, J. Pan, SH Tsai, E. Zamburg, A. Thean, National University of Singapore

We demonstrate, for the first time, 40nm BEOL TG/DG FeFETs with ultra-low Dits~ $10^{11}cm^{-2}eV^{-1}$, a large MW~2.1V, nearly-ideal *S.S.*~ 62 mV/dec., and the record-low read-after-write delay of 200 ns based on the defect self-compensation effect, pushing the boundary of BEOL FeFETs toward future dense non-volatile logic applications.

2:00 p.m.
6.2 Ferroelectric and interlayer co-optimization with in-depth analysis for high endurance FeFET, Y. Zhou, Z. Liang, W. Luo, M. Yu, R. Zhu, X. Lv, J. Li, Q. Huang*, F. Liu*, K. Tang*, R. Huang*, Peking University, *also with Beijing Advanced Innovation Center for Integrated Circuits.

We co-optimize the ferroelectric materials and interlayer in FeFET. The novel combination of Hf0.95Al0.05O2+Al2O3 enhances the endurance to 5×10^9 cycles while maintaining a retention > 10 years. Analysis based on DFT and DQSCV reveal mechanism of optimization. We develop a interface trap model to correlate different trapping dynamics .

2:25 p.m.
6.3 *In-situ* atomic-level observation of reversible first-order transitioning $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric film, Y. Zheng, T. Xin, J. Yang, Y. Zheng, Z. Gao, Y. Wang, Y. Xu, Y. Cheng, K. Du*, D. Su*, R. Shao**, B. Zhou, Z. Yuan, Q. Zhong, C. Liu, R. Huang, X. Tang, C. Duan, S. Song***, Z. Song, H. Lyu, East China Normal University, *Huawei Technologies Co., **Beijing Institute of Technology, ***Shanghai Institute of Microsystem and Information Technology

We revealed the dynamic process of atomic structure transitions in ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ films across Curie temperature in Cs-TEM with in-situ controlled heating up and cooling down process. The monoclinic phase contributes to stable ferroelectric orthorhombic structure by introducing the local compressive stress, resulting in different Curie temperaturein local regions.

2:50 p.m.
6.4 High performance La-doped HZO based ferroelectric capacitors by interfacial engineering, M. Popovici, J. Bizindavyi, P. Favia, S. Clima, M. Alam, R. Ramachandran*, A. Walke, U. Celano, A. Leonhardt**, S. Mukherjee, O. Richard, A. Illiberi*, M. Givens*, R. Delhougne, J. Houdt, G. Sankar Kar, imec, *ASM Belgium, **ASM Microchemistry Oy, KU Leuven/imec

Capacitors based on trilayer stacks of TiO_2/La-doped hafnium zirconate/Nb_2O_5 show record high remnant polarization 2Pr of 66.5 μC/cm^2 after $3x10^6$ cycles at 3 MV/cm or an endurance of up to 10^{11} cycles with a final $2P_R$ of ~30 μC/cm^2 at 1.8 MV/cm depending on the Hf and Zr precursors used.

3:40 p.m.
6.5 Record-high 2Pr = 60 μC/cm2 by Sub-5ns Switching Pulse in Ferroelectric Lanthanum-doped HfO2 with Large Single Grain of Orthorhombic Phase > 38 nm, T. Fu, M. Zeng*, S. Liu, H. Liu*, R. Huang, Y. Wu, Peking University, *Huazhong University of Science and Technology

We systematically characterized the excellent ferroelectricity in La-doped HfO2 devices. A large single grain of o-phase over 38 nm is observed. Ultra-fast and high-reliability polarization switching is realized. Record-high 2Pr = 60 μC/cm$_2$ is achieved under 5 ns pulse, realizing record low switching time required for 2028 IRDS standard.

4:05 p.m.
6.6 A c-axis aligned crystalline IGZO FET and a 0.06-μm^2 HfO_2-based Capacitor 1T1C FeRAM with High Voltage Tolerance and 10-ns Write Time, M. Endo, S. Numata, K. Ohshima, Y. Egi, F. Isaka, T. Ohno, S. Tezuka, T. Hamada, K. F., K. Tsuda, T. Matsuzaki, T. Onuki, T. Murakawa, H. Kunitake, M. Kobayashi*, S. Yamazaki, Semiconductor Energy Laboratory Co, Ltd., *The University of Tokyo

We fabricated ferroelectric memories using oxide semiconductor field-effect transistors and HfO_2-based capacitors. A damascene-processed bottom electrode eliminated leakage and endurance issues at the capacitor edge. The fabricated memory, with 1T1C configuration including the 0.06-μm^2 capacitor, achieves non-volatility, reliability comparable to prior arts, high-speed operation, and lower voltage.

4:30 p.m.

6.7 Hafnia-Based FeRAM: A Path Toward Ultra-High Density for Next-Generation High-Speed Embedded Memory (Invited), N. Haratipour, S-C Chang, S. Shivaraman, C. Neumann, Y-C Liao, B. Granados Alpizar, I-C Tung, H. Li, V. Kumar, B. Doyle, S. Atanasov, J. Peck, N. Kabir, G. Allen, T. Hoff, A. Oni, S. Dutta, T. Tronic, A. Roy, F. Hamzaoglu, R. Bristol, M. Metz, I. Young, J. Kavalieros, U. Avci, Intel Corporation

FeRAM is a promising candidate for next generation embedded DRAM and has attracted significant attention with the advancements in hafnia-based ferroelectric research. In this work, we will review record specifications achieved for implementing FeRAM as an embedded memory such as 2 ns switching speed, $>10^{12}$ read/write endurance cycles, low-voltage operation.

Session 7: EDT - 2D Channel Technology
Monday, December 5, 1:30 p.m.
Continental Ballroom 6
Co-Chairs: Eric Pop, Stanford University
Nicolas Loubet

1:35 p.m.
7.1 High-Performance Bilayer WSe2 pFET with Record Ids = 425 µA/µm and Gm = 100 µS/µm at Vds = -1 V By Direct Growth and Fabrication on SiO2 Substrate, X. Shi, X. Wang, S. Liu, Q. Guo, L. Sun, X. Li, R. Huang, Y. Wu, Peking University, Huazhong University of Science and Technology

We demonstrate pFETs based on CVD-grown bilayer WSe_2 with EOT scaling. The transistors exhibit contact resistance of 0.65 kΩ·µm. Record high I_{ds} of 425 µA/µm and g_m of 100 µS/µm are achieved at V_{ds} = -1 V. This work providing new solutions for promoting the development of 2D CMOS devices.

2:00 p.m.
7.2 High-Performance Monolayer WSe_2 p/n FETs via Antimony-Platinum Modulated Contact Technology towards 2D CMOS Electronics, A-S Chou, Y-T Lin, Y. Cosmi Lin*, C-H Hsu, M-Y Li, S-L Liew, S.A. Chou, H-Y Chen, H-Y Chiu, P-H Ho, M-C Hsu, Y-W Hsu, N. Yang, W-Y Woon, S. Liao, D-H Hou, C-H Chien, W-H Chang, I P. Radu, C-I Wu, H.-S. Philip Wong, H. Wang, TSMC, *National Taiwan University, **National Yang Ming Chiao Tung University

This work presents a novel Sb-Pt modulated contact technology which can alleviate the pinning effect, leading to exceptional ohmic contacts of 0.75 kΩ·µm and demonstrating remarkable on-state p/n current ~150 µA/µm at |VD| = 1 V for both p-/n-type WSe_2 FETs, indicating the potential of WSe2 for CMOS applications.

2:25 p.m.
7.3 pMOSFET with CVD-grown 2D semiconductor channel enabled by ultra-thin and fab-compatible spacer doping, T. Hung, M-Z Li, W-S Yun, S. A. Chou, S-K Su, E. Chen, S-L Liew*, Y-M Yang**, K-I Lin**, D-H Hou*, T.Y. Lee, H. Wang, C-C Cheng, M-T Lin*, H.-S. PhilipWong, I P. Radu, TSMC, *National Cheng Kung University, **National Taiwan University

We present the first demonstration of p-MOSFET with a high ON current 10^{-5} A/um and good S.S.80 mV/dec. MOSFETs have the advantage of lower access resistance compared to Schottky barrier FETs. Here, we introduce a self-limiting, fab-compatible process which consists of WO_x obtained from WSe_2 by O_2 plasma conversion.

3:15 p.m.

7.4 Nearly Ideal Subthreshold Swing in Monolayer MoS_2 Top-Gate nFETs with Scaled EOT of 1 nm, T-E Lee, E. Su, B-J Lin, Y-X Chen**, W-S Yun, P-H Ho, J-F Wang, S-K Su, C-F Hsu, P-S Mao*, Y.C. Chang*, C-H Chien*, B-H Liu**, C-Y Su**, C-C Kei**, H. Wang, H.-S. Philip Wong, T.Y. Lee, W-H Chang*, C-C Cheng, I. P. Radu, TSMC, *National Yang Ming Chiao Tung University, **Taiwan Instrument Research Institute, ***National Applied Research Laboratories

Transistor scaling enabled by L_G scaling requires EOT scaling. This work successfully integrates ALD higher-*k* dielectrics with CVD-grown 1L-MoS_2 to build top-gate nFET with EOT ~1 nm with nearly ideal S.S. of 68 mV/dec. The gate stack described here achieves high e_{eff} ~13.53, a large E_{BD}~12.4 MV/cm, and excellent J_G.

3:40 p.m.
7.5 Gate length scaling beyond Si: Mono-layer 2D Channel FETs Robust to Short Channel Effects, C. Dorow, A. Verma Penumatcha, A. Kitamura, C. Rogan, K. O'Brien, S. Lee, R. Ramamurthy, C-Y Cheng, K. Maxey, T. Zhong, T. Tronic, B. Holybee, J. Richards, A. Oni, C.-C. Lin, C. Naylor, N. Arefin, M. Metz, R. Bristol, S. Clendenning, Y. Avci, Intel Corporation

We explore 2D transistor scaling down to $L_{S\text{-}D}$ of 25 nm, comparable to Si state-of-the-art. Single-gated devices show increased SS_{sat} below $L_{S\text{-}D}$ = 34 nm, while double-gate achieves steep SS_{sat} of 75 mV/dec, low DIBL for long $L_{S\text{-}D}$. BTI shows reliability improvement needed. TCAD confirms 2D channels robust to SCEs.

4:05 p.m.
7.6 Crystalline Complex Oxide Membrane: Sub-1 nm CET Dielectrics for 2D Transistors (Invited), L. Li, The University of Hong Kong

2D FETs with sub-1-nm CET are demonstrated through integrating single-crystal SrTiO3 dielectrics with a monolayer MoS_2, where the optimized $SrTiO_3$ gate stack exhibits leakage below the low-standby-power limit. Short-channel devices manifest good reliability and performance, including the steep SS of ~75 mV/dec and a large ON/OFF current ratio of 10^6.

4:30 p.m.
7.7 Dielectric Interface Engineering for High-Performance Monolayer MoS_2 Transistors via hBN Interfacial Layer and Ta Seeding, H.-Y. Lan, J. Appenzeller, Z. Chen, Purdue University

We developed innovative approaches for dielectric interface engineering in monolayer MoS_2 transistors via hBN interfacial layer and Ta seeding. Our devices exhibit a record high *I*ON of 598 μA/μm at V_{DS} = 0.65 V and the lowest *SS* of 62 mV/dec, exceeding IRDS 2028 HD spec.

Session 8: MS - Advancing Moore's Law
Monday, December 5, 1:30 p.m.
Continental Ballroom 7-9
Co-Chairs: Hemant Dixit, Wolfspeed
Roza Kotlyar, Intel

1:35 p.m.
8.1 Compact Modeling of Emerging IC Devices for Technology-Design Co-development (Invited), G. Pahwa, A. Dasgupta*, C-T Tung, M-Y Kao, C. Kumar Dabhi, S. Sarker*, S. Salahuddin, C. Hu, University of California Berkeley, *Indian Institute of Technology Roorkee

This paper presents compact models of GAA, MRAM, ferroelectric logic, memory devices, as well as cryogenic CMOS that supports quantum computing. These compact models achieve microseconds fast simulation of the charge and current of devices using analytical functions as solutions to complex device physics problems aided by adjustable parameters.

2:00 p.m.
8.2 Direct Extraction of Density of Tail States from Split C-V Characteristics and their Impacts on Sub-threshold Swing of Si n- and p-MOSFETs at Cryogenic Temperatures, M-S Kang, H. Oka*, T. Mori*, K. Toprasertpong, M. Takenaka, S. Takagi, The University of Tokyo, *National Institute of Advanced Industrial Science and Technology (AIST)

We proposed a novel method to evaluate the tail state density in Si n- and p-MOSFETs by using split C-V characteristics at low temperatures and successfully extracted the density of tail states, which can quantitatively represent the behaviors of sub-threshold swing at temperatures from 4 to 300 K.

2:25 p.m.
8.3 On the universality of drain-induced-barrier-lowering in field-effect transistors, S-M Choi, H-B Jo, D-Y Yun, J-G Kim, W-S Park, J-M Baek, I-G Lee, J-K Shin, H-M Kwon*, T. Tsutsumi**, H. Sugiyama**, H. Matsuzaki**, J-H Lee, D-H Kim, Kyungpook National University, *Korea Polytech, **NTT Corporation

We revisited on the extraction of drain-induced-barrier-lowering *(DIBL)* in various types of devices with L_g ranging from several mm to sub-30 nm and from planar to *GAA* architectures. We herein proposed how to accurately extract *DIBL* and how to correct reported values of *DIBL* that were extracted in the conventional manner.

2:50 p.m.
8.4 Mitigating Impact of Defects On Performance with Classical Device Engineering of Scaled Si/SiGe Qubit Arrays, R. Kotlyar, Intel

We model an impact on Si/SiGe devices from low DIT densities. We discuss a spurious dot formation and the impact of defects on noise and two-qubit gate fidelity. We show that scaling pitch, dielectric thickness, using deeper buffers, screening gates allow to mitigate the impact of defects on quantum performance.

3:40 p.m.
8.5 Theoretical and Empirical Insight into Dopant, Mobility and Defect States in W Doped Amorphous In_2O_3 for High-Performance Enhancement Mode BEOL Transistors, Y. Hu, H. Ye*, K. A. Aabrar*, S. Gopal Kirtania*, W. Chakraborty*, S. Datta*, K. Cho, University of Texas at Dallas, *University of Notre Dame

Tungsten doped amorphous In_{2O3} enable BEOL-compatible enhancement-mode nFETs with record performance such as I_{ON} ~500μA/μm, I_{ON}/I_{OFF} ~10^9 and near-ideal SS ~60mV/dec. The tungsten doping role is revealed as precise control of doping, maximization of mobility, suppression of oxygen-vacancy, and stabilization of threshold-voltage, through which enhancement-mode oxide channel FETs are realized.

4:05 p.m.
8.6 OTS Physics-based Screening for Environment-friendly Selector Materials, D. Matsubayashi*, S. Clima, T. Ravsher**, D. Garbin, R. Delhougne, G. Sankar Kar, G. Pourtois***, imec, *KIOXIA Corporation, **KULeuven, ***UAntwerp

For sustainable developments, we performed systematic, and fully ab-initio screening for new ovonic threshold switching (OTS) materials, excluding toxic elements. We introduced OTS physics-based material parameters like material stability, electronic properties, or polarizability change (OTS gauge), and extracted 11 promising ternary compositions of As/Se-free OTS selector materials for RRAM applications.

Session 9: PDS - Recent Advancements in Power Semiconductor Devices
Monday, December 5, 1:30 p.m.
Imperial Ballroom A
Co-Chairs: Don Disney, Infineon Technologies
Akira Nakajima, AIST

1:35 p.m.
9.1 Scalable Ultrahigh Voltage SiC Superjunction Device Technologies for Power Electronics Applications (Invited), R. Ghandi, C. Hitchcock, S. Kennerly, M. Torky*, P. Chow*, GE Research, *Rensselaer Polytechnic Institute

We comparatively review charge-balanced and conventional superjunction SiC power device structures, with particular emphasis on implementations using high-energy (MeV) implantations. These superjunction diodes and MOSFETs offer specific on-resistance below the SiC limit. We demonstrate 3.8kV deep-implanted SiC superjunction diodes formed with only two rounds of epitaxial overgrowth and high-energy implantations.

2:00 p.m.
9.2 Design guidlines for SBD integration into SiC-MOSFET breaking RonA- diode conduction capability trade-off, S. Asaba, Y. Kusumoto, M. Furukawa, R. Iijima, H. Kono, Toshiba Electronic Devices & Storage Corporation

An effective design of embedding SBD into SiC-MOSFET was proposed. Superior parasitic body p-n diode clamping effect 2 times better than did the conventional SBD pattern was demonstrated. Moreover, low on-resistance was also realized thanks to increased channel density due to reduced area penalty for SBD integration.

2:25 p.m.
9.3 Design and Characterization of the Junction Isolation Structure for Monolithic Integration of Planar CMOS and Vertical Power MOSFET on 4H-SiC up to 300 ℃, B-Y Tsui, T-K Tsai, C-L Hung, Y-X Wen, National Yang Ming Chiao Tung University

Design criteria of the P-type junction isolation (P-iso) structure for SiC CMOS and 600-V-class power MOSFET integration are investigated for the first time. With proper design, the P-iso structure achieves breakdown voltage higher than 800 V and functions at 300 ℃ with substrate bias at 600 V.

2:50 p.m.
9.4 41% Reduction In Power Stage Area On Silicon-On-Insulator Bipolar-CMOS-DMOS-IGBT Platform With Newly Developed Multiple Deep-Oxide Trench Technology, L. Zhang, J. Ma, Y. Gu, S. Liu, J. Wei, S. Li, W. Sun, S. Zhang*, Southeast University, CSMC Technologies Corporation

MDOT technology is demonstrated for BCDI platform in this paper. MDOT can realize area saving through assisting in voltage blocking. At the voltage of 500V, the area of power stage in the single-chip intelligent power IC can be shrunk by 41.1%, allowing significant reduction in chip size and cost.

3:40 p.m.

9.5 High-Performance Vertical β-Ga2O3 Schottky Barrier Diodes Featuring P-NiO JTE with Adjustable Conductivity, W. Hao, F. Wu, W. Li*, G. Xu, X. Xie, K. Zhou, W. Guo, X. Zhou, Q. He, X. Zhao, S. Yang, S. Long, University of Science and Technology of China, *University of California, Berkeley

We demonstrate a novel conductivity-controlled JTE technique using p-type NiO-a key element for potential commercialization of β-Ga_2O_3 power devices without common reliability concerns. The β-Ga_2O_3 SBD with an optimized hole concentration about $10^{17}cm^{-3}$ exhibits a $R_{on,sp}$ of $2.9m\Omega\cdot cm^2$ and a high V_{br} of 2.1kV, yielding a high PFOM of $1.52GW/cm^2$.

4:05 p.m.
9.6 GaN Field Emitter Arrays with JA of 10 A/cm2 at VGE = 50 V for Power Applications, P-C Shih, T. Zheng*, M. Josefina Arellano-Jimenez**, B. Gnade*, A. Akinwande, T. Palacios, Massachusetts Institute of Technology, *Southern Methodist University, **University of Texas at Dallas

III-Nitrides are attractive as field emission devices. GaN vertical field emitter arrays with uniform sub-10 nm tip radius are demonstrated. The best GaN device has a current density of 10 A/cm^2 at V_{GE} = 50 V, which is better than the state-of-the-art Si devices at the same bias condition.

¶Session 10 - MT: MRAM
Tuesday, December 6, 9:00 a.m.
Grand Ballroom A
Co-Chairs: Hyungsung Jung, Samsung
Xinyu Bao, TSMC

9:05 a.m.
10.1 First demonstration of full integration and characterization of $4F^2$ 1S1M cells with 45 nm of pitch and 20 nm of MTJ size, S. Seo, H. Aikawa*, S. Kim*, T. Nagase*, Y. Ito*, T.J. Ha, K. Yoshino*, B.K. Jung, T. Oikawa*, K. Y. Jung, H.I. Moon, B.S. Kim, F. Matsuoka**, K. Hatsuda**, K. Hoya**, S. Kim, S-HY Lee, M-H Na, S.Y. Cha, SK hynix Inc., *Kioxia Korea Corporation

The authors report for the first time the performance of 1 selector-1 MTJ (1S1M) cells integrated in 45 nm of pitch and 20nm of MTJ CD on CMOS circuit using As-doped SiO2 selector. This paper shows the potential of the cross-point MRAM for the application of high-density and low-cost memory.

9:30 a.m.
10.2 Double spin-torque magnetic tunnel junction devices for last-level cache applications, G. Hu, C. Safranski, J. Sun, P. Hashemi, S. Brown, J. Bruley, L. Buzi, C. Demic, E. Galligan, M. Gottwald, O. Gunawan, J. Lee, S. Karimeddiny, P. Trouilloud, D. Worledge, IBM Research

We experimentally demonstrate reliable 300 ps switching in arrays of 35 nm double spin-torque magnetic tunnel junctions (DS-MTJs) and also demonstrate a new free-layer design with improved activation energy and magnetoresistance. We establish a new method to characterize the DS-MTJ devices, by introducing and experimentally verifying a simple device-physics model.

9:55 a.m
10.3 25 nm iPMA-type Hexa-MTJ with solder reflow capability and endurance $>10^7$ for eFlash-type MRAM, H. Honjo, K. N., S. Miura, H. Naganuma, T. Watanabe, T. Nasuno, T. Tanigawa, Y. Noguchi, H. Inoue, M. Yasuhira, S. Ikeda, T. Endoh, Tohoku University

We developed solder reflow capable i-PMA-type Hexa-MTJ with BEOL process compatibility down to 25nm. The 25nm iPMA-type Hexa-MTJ simultaneously realized a small temperature dependence of thermal stability factor Δ, a sufficiently large iPMA, a large TMR ratio with low resistance, and a write endurance $>10^7$ with 100 ns write pulse.

10:20 a.m.
10.4 High-Speed (400MB/s) and Low-BER STT-MRAM Technology for Industrial Applications, S. Ikegawa, K. Nagel, F. Mancoff, S. Alam, M. Arora, M. DeHerrera, H. K. Lee, S. Mukherjee, G. Shimon, J. Sun, I. Rahman, F. Neumeyer, H.Y. Chou, CH Tan, A. Shah, S. Aggarwal, Everspin Technologies, Inc.

We describe the MTJ technology and reliability for a new 64Mb STT-MRAM targeted at industrial applications. The part features an xSPI interface with a throughput of 400MB/s, a temperature range from -40°C to 85°C, a BER of less than 1e-15, and 10 years data retention at 105°C.

11:10 a.m.
10.5 Device Variation-Aware Adaptive Quantization for MRAM-based Accurate In-Memory Computing Without On-chip Training, Z. Xiao, V. Bharat Naik*, S.K. Cheung, J.H. Lim*, J-H Kwon, Z. Ren, Z. Wang***, Q. Shao, The Hong Kong University of Science and Technology, AI Chip Center for Emerging Smart Systems, *Globalfoundries, ***The University of Hong Kong

This work showed the unique feature of device variations in foundry STT-MRAM array and proposed a software-hardware cross-layer co-design scheme for MRAM IMC. The proposed method allows NN applications to reach in-situ training accuracy without on-chip training cycles that can extend the MRAM device's endurance for IoT/ edge applications.

11:35 a.m.
10.6 Highly reliable STT-MRAM adopting advanced MTJs with controlled domain wall pinning, J-H Park, J Kim, JMK Kim, J. Kim, D. Apalkov, A. Okada, H. Sato, J. H. Jeong, Y. J. Cho, U. Pi, Y. Kim, Y. Park, K. M. Song, K. Kim, Dae E. Jeong, D. Kim, C. Kim, I. H. Kim, K. Lee, S. H. Han, K. Lee, J-H Lee, Y. J. Song, G. H. Koh, B. J. Kuh, J. M. Lee, J. Song, Samsung Electronics Co.

We demonstrate highly reliable STT-MRAM whose array-level write error has been eliminated by lowering the density of domain wall pinning sites in the MTJs. By controlling the domain wall pinning, we obtain high-density MTJ array having superior reliability without notable trailing bits of write fail.

12:00 p.m.
10.7 World-most energy-efficient MRAM technology for non-volatile RAM applications, T. Y. Lee, J. M. Lee, M. K. Kim, J. S. Oh, J. W. Lee, H. M. Jung, P. H. Jang, M. K. Joo, K. Suh, S. H. Han, D. E. Jeong, K. Kai, J. H. Jeong, J-H Park, K. Lee, J. H. Lee, Y. H. Park, E. B. Chang, Y. K. Park, H. J. Shin, Y. S. Ji, S. H. Hwang, K. T. Nam, B. S. Kwon, M. K. Cho, B. Y. Seo, Y. J. Song, Samsung Electronics Co.

We present the most energy-efficient 16-Mb nvRAM product with high endurance over 1E14 cycles by using 28-nm eMRAM technology. Extending to 14-nm FinFET resulted in 33% area scaling and 2.6× faster read cycle time. This proves the potential of eMRAM technology as a low-leakage working memory solution for SoC applications.

Session 11: MAT - Advanced Devices for High RF and THz Applications
Tuesday, December 6, 9:00 a.m.
Continental Ballroom 1-3
Co-Chairs: Pascal Chevalier, STMicroelectronics
Takuya Tsutumi, NTT

9:05 a.m.
11.1 FerroHEMTs: High-Current and High-Speed All-Epitaxial AlScN/GaN Ferroelectric Transistors, J. Casamento, K. Nomoto, T-S Nguyen, H. Lee, C. Savant, L. Li, A. Hickman, T. Maeda, J. Encomendero, V. Gund, A. Lal, J. Hwang, G. Xing, D. Jena, Cornell University

We report the first observation of ferroelectric gating in epitaxial AlScN barrier nitride transistors. These FerroHEMTs deliver the highest on-currents at 4 A/mm, and highest speed with fMAX > 150 GHz observed in any ferroelectric transistor. The FerroHEMTs exhibit hysteretic Id −Vgs loops with subthreshold slopes below the Boltzmann limit.

9:30 a.m.
11.2 Record 94 GHz performance from N-polar GaN-on-Sapphire MIS-HEMTs: 5.8W/mm and 38.5% PAE, W. Li, B. Romanczyk, E. Akso, M. Guidry, N. Hatui, C. Wurm, W. Liu, P. Shrestha, H. Collins, C. Clymore, S. Keller, U. Mishra, University of California Santa Barbara

In this paper, N-polar GaN-on-sapphire MIS-HEMTs with breakthrough performance is reported. Devices show a high 8.8dB linear gain at 94GHz, enabling excellent power density of 5.83W/mm with record 38.5% power-added efficiency at 14V. Furthermore, at 12V the device demonstrated record PAE of 40.2% with an 4.85 W/mm power dentistry.

9:55 a.m.
11.3 First Demonstration of State-of-the-art GaN HEMTs for Power and RF Applications on A Unified Platform with Free-standing GaN Substrate and Fe/C Co-doped Buffer, M. Wu, M. Zhang, L. Yang, B. Hou, Q. Yu, S. Li, C. Shi, W. Zhao, H. Lu, W. Chen, Q. Zhu, X. Ma, Y. Hao, Xidian University, China Academy of Space Technology (Xi'an)

We report excellent power and RF performances of GaN-on-GaN HEMTs with high reliability using the Fe/C co-doped GaN buffer. This technology provides a unified design of material and process for GaN power and RF devices with high performance, promoting the integration of GaN-based devices on the same platform.

10:45 a.m.
11.4 Terahertz In0.8Ga0.2As quantum-well HEMTs toward 6G applications, W-S Park, H-B Jo, H-J Kim, S-M Choi, J-H Yoo, J-H Kim, H-S Jeong, S. George, J-M Baek, I-G Lee, T-W Kim*, S-K Kim**, J. Yun**, T. Kim**, T. Tsutsumi***, H. Sugiyama***, H. Matsuzaki***, J-H Lee, D-H Kim, Kyungpook National University, *University of Ulsan, **NTT Corporation

We present the systematic analysis of L_g scaling behavior and the impact of the side-recess spacing (L_{side}) on DC and high-frequency characteristics of $In_{0.8}Ga_{0.2}As$ QW HEMTs with L_g from 10 μm to 20 nm, aiming to explore the scaling limit of f_{max} and thereby demonstrate THz devices.

11:10 a.m.
11.5 III-V/III-N technologies for next generation high-capacity wireless communication (Invited), N. Collaert, A. Alian, A. Banerjee, G. Boccardi, P. Cardinael, V. Chauhan, C. Desset, R. ElKashlan, A. Khaled, M. Ingels, B. Kunert, Y. Mols, B. O'Sullivan, U. Peralagu, N. Pinho, R. Rodriguez, A. Sibaja-Hernandez, S. Sinha, X. Sun, A. Vais, B. Vermeersch, S. Yadav, D. Yan, H. Yu, Y. Zhang, M. Zhao, J. Van Driessche, imec

In this paper, we will discuss the progress that has been made in upscaling GaN and InP to a Si platform as well as making them CMOS and 3D compatible to enable the heterogeneous systems that will be needed for 5G mm-wave and 6G sub-THz frequencies for high-capacity wireless communication.

11:35 a.m.
11.6 415/610GHz f_T/f_{MAX} SiGe HBTs Integrated in a 45nm PDSOI BiCMOS process, V. Jain, J. Pekarik, C. Kenney, J. Holt, C. Durcan, J. Johnson, S. Saroop, M. Nafari, V. Ruparelia, S. Gedela, P. Sharma, V. Ontalus, V. Vanukuru, A. Joseph, Globalfoundries

HP SiGe HBTs integrated in 45nm PDSOI BiCMOS with peak f_T/f_{MAX} 415/610GHz are reported. These are the highest /f_{MAX} silicon devices demonstrated in any SOI platform. The process co-integrates RF N/P FETs with f_T/f_{MAX} 270/355GHz and 240/295GHz. Simple cascode powercells show >23dB gain at 70GHz and >18dB gain at 100GHz.

12:00 p.m.
11.7 0.13 µm HR SiGe BiCMOS Technology exhibiting 169 fs Ron x Coff Switch Performance targeting WiFi 6E Fully-Integrated RF Front-End-IC Solutions, F. Gianesello, C. Charbuillet, N. Derrier, D. Muller, C. Diouf, D. Ney, C. Deglise-Favre, I. Sicard, M. Ali Nsibi, R. Debroucke, M. Buczko, C.A. Legrand, Ph. Cathelin, F. Paillardet, J.C. Mas, P. Chevalier and D. Gloria, STMicroelectronics

In this paper, we review the optimization of an HR SiGe BiCMOS technology. State of the art RF switch performances have been achieved with $R_{ON} \times C_{OFF}$ of 169 fs and WiFi SPDT exhibiting insertion loss of ~0.8 dB @ 5.5 GHz and power handling capability exceeding 31 dBm.

Session 12: ALT - Advanced Metalization & BEOL Device Technology

Tuesday, December 6, 9:00 a.m.
Continental 4
Co-Chairs: Youseok Suh, Qualcomm
Dechao Guo, IBM

9:05 a.m.
12.1 Subtractive Ru Interconnect Enabled by Novel Patterning Solution for EUV Double Patterning and TopVia with Embedded Airgap Integration for Post Cu Interconnect Scaling, C. Penny, K. Motoyama, S. Ghosh, T. Bae, N. Lanzillo, S. Sieg, J. Lee, C. Park, L. Zou, H. Lee, D. Metzler, J. Lee, S. Cho, M. Shoudy, S. Nguyen, A. Simon, K. Park, L. Clevenger, B. Anderson, C. Child, T. Yamashita, J. Arnold, T. Wu, T. Spooner, K. Choi, K-I Seo, D. Guo, IBM ReseaRch, *Samsung

Fully subtractive TopVia Ru interconnects with embedded airgap have been demonstrated. We demonstrate 18nm pitch structures patterned with spacer assisted litho-etch litho-etch. We also demonstrate a novel "TopVia" structure where the metallization for the via is performed together with the metallization for the line below, combined with an integrated airgap.

9:30 a.m.
12.2 Low-Thermal-Budget BEOL-Compatible Beyond-Silicon Transistor Technologies for Future Monolithic-3D Compute and Memory Applications (Invited), A. Thean, S. H. Tsai, C. K. Chen, M. Sivan, B. Tang, S. Hooda, Z. Fang, J. Pan, J. Feng Leong, H. Veluri, E. Zamburg*, National University of Singapore, *SHINE

If Si CMOS for massive M3D is difficult due to need for high-thermal-budget processes, are there solutions that are beyond Si? In this article, we discuss two low-thermal-budget approaches: Oxide Semiconductor and 2D Materials for M3D integration.

9:55 a.m
12.3 First Demonstration of BEOL-Compatible 3D Fin-Gate Oxide Semiconductor Fe-FETs, Q. Kong, L. Liu, Z. Zheng, C. Sun, A. Kumar, R. Shao, Z. Zhou, L. Jiao, J. Zhang, H. Xu, Y. Chen, G. Liu, Z. Dong, X. Wang, B-Y, X. Gong*, National University of Singapore, *also with Soitec

We report back-end-of-line (BEOL)-compatible 3D fin-gate oxide semiconductor (OS) ferroelectric field-effect-transistors (Fe-FETs) featuring ALD-deposited ZnO channel and Zr-doped HfO_2 (HZO) ferroelectric dielectric with a channel length (L_{ch}) as small as 50 nm. The fin-gate OS Fe-FETs show excellent electrical characteristics together with the capability to suppress the device-to-device $_{V}th$) variation.

10:20 a.m.
12.4 Transient Thermal and Electrical Co-Optimization of BEOL Top-Gated ALD In_2O_3 FETs on Various Thermally Conductive Substrates Including Diamond, P-Y Liao, S. Alajlouni, Z. Zhang, Z. Lin, M. Si, J. Noh, T. Feygelson*, M. Tadjer*, A. Shakouri, P. Ye, Purdue University, *United States Naval Research Laboratory

In this work, we co-optimize the transient thermal and electrical characteristics of top-gated, ultrathin, atomic-layer-deposited, back-end-of-line compatible indium oxide transistors on various thermally conductive substrates by visualization of the self-heating effect utilizing an ultrafast high-resolution thermo-reflectance imaging system and overcome the thermal challenges through substrate thermal management and short-pulse measurement.

11:10 a.m.
12.5 First Demonstration of Dual-Gated Indium Tin Oxide Transistors with Record Drive Current ~2.3 mA/μm at L ≈ 60 nm and VDS = 1 V, S. Wahid, A. Daus, A. Kumar, H. S. Philip Wong, E. Pop, Stanford University

We report the first dual-gated indium tin oxide (ITO) transistors with record-high drive current ~2.3 mA/μm for L ~ 60 nm at V_{DS} = 1 V. We study Ni vs. Pd contacts, achieving good R_C ~300 Ω·μm and minimized threshold voltage shift at shorter channels with Pd contacts.

11:35 a.m.
12.6 MOL Local Interconnect Innovation: Materials, Process & Systems Co-optimization for 3nm Node and Beyond, A. Pal, G. Thareja, S. Dag, G. Costrini, V. Reddy, Y. Xu, Y. Lei, A. Zhang, G. Shen, A. Jansen, Z. Chen, M. Gage, J. Tang, Y-C Yang, S. Deshpande, S. Huey, R. Hung, H. Jiang, M-P Cai, Y. Abramovitz, L. Engel, M. Naik, R. Wang, S. Kesapragada, B. Ayyagari-Sangamalli, X. Tang, E. Mehdi Bazizi, Applied Materials

We present a new selective tungsten gap-fill process offering liner-less, bottom-up, seamless tungsten growth with 40% via-resistance reduction over traditional CVD tungsten vias. Our ring-oscillator modeling projects a 6% and 13% ring-oscillator performance benefit at 7nm and 3nm technology nodes respectively and a 4% processor-level performance benefit at 7nm node.

Session 13: MS - Ferroelectrics: From Modeling of Wake-up and Endurance to Novel Circuits
Tuesday, December 6, 9:00 a.m.
Continental Ballroom 5
Co-Chairs: Darsen Lu, National Cheng Kung University

Francois Triozon, CEA-Leti

9:05 a.m.
13.1 Multi-domain Phase-field Modeling of Polycrystalline Hafnia-based (Anti-)ferroelectrics Capable of Representing Defects, Wake-up and Fatigue, S-C Chang, K. Chae, M. Popovici*, C-C Lin, S. Siddiqui, I-C Tung, J. Bizindavyi*, B. Granados Alpizar, N. Haratipour, M. Metz, J. Kavalieros, G. Sankar Kar*, A. Kummel**, K. Cho***, U. Avci, Intel, *imec, **University of California, San Diego, ***University of Texas at Dallas

For the first time, this paper presents a multi-domain phase-field framework capable of representing the mixture of phases, phase transitions during wake-up and fatigue, and defect-driven cycling behavior such as imprint in hafnia-based (anti-)ferroelectric thin films. This work opens new opportunities for device designs with mixed phases in hafnia.

9:30 a.m.
13.2 Quantitative study of EOT lowering in negative capacitance HfO_2-ZrO_2 superlattice gate stacks, M. Hoffmann, S. Cheema, N. Shanker, W. Li, S. Salahuddin, University of California Berkeley

Fluorite-structure gate oxides with negative capacitance (NC) are promising for EOT scaling, but a quantitative understanding of their behavior is needed. Here we combine pulsed-voltage and impedance measurements with compact modeling and 2D phase field simulations to model experimental data and show how substantially further EOT scaling could be achieved.

9:55 a.m.
13.3 Deep insights into the Interplay of Polarization Switching, Charge Trapping, and Soft Breakdown in Metal-Ferroelectric-Metal-Insulator-Semiconductor Structure: Experiment and Modeling, X. Wang, C. Sun, Z. Zheng, L. Jiao, Z. Zhou, Z. Dong, G. Liu, Q. Kong, J. Zhang, H. Xu, K. Han, Y. Kang, L. Liu, X. Gong, National University of Singapore

We perform comprehensive experiment and modeling to understand the influence of ferroelectric (FE) polarization switching, charge trapping (CT) in floating gate (FG) from both control gate (CG) and channel, and soft breakdown (SBD) on the characteristics of the Fe-FETs having a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure.

10:45 a.m.
13.4 Monte-Carlo Modeling and Characterization of Switching Dynamics for Antiferroelectric/Ferroelectric HZO considering Mechanisms of Fatigue, Y-C Chen, K-Y Hsiang, M-H Lee, P. Su, National Yang Ming Chiao Tung University, *National Taiwan Normal University

We conduct an NLS-based Monte-Carlo modeling and characterization for switching dynamics of fatigued antiferroelectric/ferroelectric HZO. We model the domain pinning probability considering fatigue mechanisms mediated by oxygen-vacancy and charge-injection for each orthorhombic-phase and tetragonal-phase grains. Our model has been verified with experimental data, and can be beneficial for memory applications.

11:10 a.m.
13.5 Modeling Fatigue-Breakdown Dilemma in Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ and Optimized Programming Strategies, H-H Huang, C-Y Cho, T-Y Lin, T-S Huang, M-H Wu, I-T Wang, Y-K Chang**, C-H Chou**, P-J Liao**, H-Y Yang*, Y-D Lin*, P-C Yeh*, S-S Sheu*, T-H Hou, National Yang Ming Chiao Tung University, *TSMC, **Industrial Technology Research Institute

The fatigue-breakdown dilemma that prevents prolonged endurance in the $Hf_{0.5}Zr_{0.5}O_2$(HZO) ferroelectric(FE) capacitor is modeled. A multi-domain FE-switching model considering local charge trapping/detrapping, strong depolarization field, and defect generation at interfacial layers successfully simulates domain pinning, recovery, and breakdown. Programming strategies using different recovery schemes and a triangular pulse are discussed.

11:35 a.m.
13.6 On the Write Schemes and Efficiency of FeFET 1T NOR Array for Embedded Nonvolatile Memory and Beyond, Y. Xiao, Y. Xu, Z. Jiang*, S. Deng*, Z. Zhao*, A. Mallick**, L. Sun***, R. Joshi#, X. Li***, N. Shukla***, V. Narayanan, K. Ni*, Pennsylvania State University, *Rochester Institute of Technology, **University of Virginia, ***Tsinghua University, #IBM Thomas J. Watson Research Center

Ferroelectric field-effect-transistor (FeFET) 1T NOR Array is promising for multiple applications yet not well studied on its write mechanism and schemes. In this work, we demonstrate 4 write schemes and a study of parasitic parameters for prospective FeFET 1T NOR array implementations as embedded NVM and beyond.

Session 14: EDT – Focus Session - Quantum Information and Sensing
Tuesday, December 6, 9:00 a.m.
Continental Ballroom 6
Co-Chairs: Bogdan Govoreanu, IMEC
Cezar Zota, IBM Zurich

9:05 a.m.
14.1 Spin Qubits in Silicon FinFET Devices (Invited), A. Fuhrer, M. Aldeghi, T. Berger*, L. Camenzind*, R. Eggli*, S. Geyer*, P. Harvey-Collard, N. Hendrickx, E. Kelly, L. Massai, M. Mergenthaler, P. Mueller, A. Kuhlmann, T. Patlatiuk*, S. Paredes, F. Schupp, G. Salis, L. Sommer, K. Tsoukalas, N. Vico Trivino, R. Warburton, D. Zumbühl, IBM Research Europe - Zurich, *University of Basel

We discuss a custom bulk FinFET platform for implementing fast and dense hole spin qubits. Using a double quantum dot with two confined holes, single- and two-qubit control is demonstrated by applying electrical microwave signals to one of the gate electrodes. From these experiments we estimate that both types of gate operations can be realized with gate times in the few nanoseconds regime. In an outlook we discuss how to further scale this technology towards 2D arrays.

9:30 a.m.
14.2 Rare earth based solid-state qubit platforms (Invited), M. Singh, J. Ahn*, S. Sullivan*, A. Kumar**, T. Zhou*, C. Ji, G. Grant, K. Sautter*, M. Holt*, A. Dibos*, F. Heremans, J. LeBeau**, D. Awschalom, S. Guha, University of Chicago, *Argonne National Laboratory, **Massachusetts Institute of Technology

Rare earth ions (REIs) are a promising platform for quantum technology given their long optical and spin coherence times. With a brief review of the field, we show how we can engineer REIs doped thin films on silicon and leverage CMOS nanofabrication methods for the development of integrated quantum devices.

9:55 a.m.
14.3 Josephson parametric amplifiers for rapid, high-fidelity measurement of solid-state qubits (Invited), S. Shankar, Z. Hao, W. Strickland*, M. Hatefipour*, J. Yuan*, J. Shabani*, University of Texas at Austin, *New York University

Josephson parametric amplifiers (JPAs) are crucial devices for readout of solid-state qubits. We review how to optimize the compression power and bandwidth of JPAs, necessary for realizing large-scale quantum information processors. We also discuss recent work to realize JPAs with a Josephson Junction Field Effect Transistor made from InAs-Al heterostructures.

10:45 a.m.
14.4 Towards Topological Superconducting Qubits (Invited), J. Shabani, W. Schiela, B. Heiba Elfeky, New York University

We review the basic model of topological quantum computation and present progress in the realization of topological qubits in hybrid superconductor-semiconductor heterostructures, including advances towards the demonstration of their exchange statistics.

11:10 a.m.
14.5 Potential of diamond solid-state quantum sensors (Invited), M. Hatano, Tokyo Institute of Technology

NV centers in diamond have superior physical properties, and their quantum coherence is preserved even at room temperature. To achieve scalable applications, the technical challenges in the sensor materials and the quantum control techniques are developed. Moreover, sensor systems for the biological/medical systems and battery/ power electronics are introduced.

11:35 a.m.
14.6 Hybrid-Magnon Quantum Devices: Strategies and Approaches (Invited), Y. Li, J. Qian*, Z. Jiang*, T-H Lo*, D. Ding*, T. Draher, T. Polakovic*, W. Pfaff, A. Schleife*, J-M Zuo*, W-K Kwok, V. Novosad, A. Hoffmann*, Argonne National Laboratory, *University of Illinois at Urbana-Champaign

Hybrid magnonics offers novel paths towards quantum information by utilizing the unique advantages of magnon excitations. We review two strategies of hybrid magnonics for advancing quantum computing, *i.e.*, multi-magnon entanglement and nonreciprocal magnon trans-duction. We also present our efforts on low-damping magnetic materials, short-wavelength magnon transduction, and nanowire superconducting circuits.

Session 15: MS - Advanced TCAD Methodology
Tuesday, December 6, 9:00 a.m.
Continental Ballroom 7-9
Co-Chairs: Joddy Wang, Synopsys
Vita Pi-Ho Hu, National Taiwan University

9:05 a.m.
15.1 Performance and Variability-Aware SRAM Design for Gate-All-Around Nanosheets and Benchmark with FinFETs at 3nm Technology Node, G, Rzepa, K. K. Bhuwalka*, O. Baumgartner, D. Leonelli*, H-W Karner, F. Schanovsky, C. Kernstock, Z. Stanojevic, H. Wu*, F. Benistant**, C. Liu*, M. Karner, Global TCAD Solutions GmbH, *Huawei Technologies R&D Belgium, **Hisilicon Technologies

Gate-all-around nanosheets offer a non-disruptive process transition from fin technologies with the advantage of full design flexibility, beneficial for n/pFET balancing in SRAM cells. Using a performance and variability-aware DTCO flow, we benchmark for 3nm. Despite lower parasitic capacitances of fins, nanosheet SRAMs achieve better Vmin, read delay, and footprint.

9:30 a.m.

15.2 Energy- and Area-Efficient 8T SRAM Cell with FEOL CFETs and BEOL-Compatible Transistors, M. Lee, S-F Fan, Z-Y Huang, Y-C Lu, V.P.-H Hu, National Taiwan University

Compared to the 6T NS SRAM, the optimized 8T $CFET_{BEOL}$ SRAM shows 40% cell area reduction, 2.2 times higher RSNM, 1.68 times larger WSNM, 53% reduction in read time, 27.8% decrease in dynamic energy, and 65.7% improvements in EDP. The 8T $CFET_{BEOL}$ SRAM could be promising candidates for data-centric applications.

9:55 a.m.
15.3 Thermal Modelling of GaN & InP RF Devices with Intrinsic Account for Nanoscale Transport Effects (Invited), B. Vermeersch, R. Rodriguez, A. Sibaja-Hernandez, A. Vais, S. Yadav, B. Parvais, N. Collaert, imec

We present a Monte Carlo thermal modelling framework with partial experimental validation suited for simulating complex 3D device geometries. Steady state and transient case studies on GaN HEMTs and InP nanoridge HBTs reveal peak temperature rises that are up to threefold larger than conventional predictions based on bulk diffusion.

10:45 a.m.
15.4 Simulation Methods of Multi-physics Effects in Nano-scale CMOS (Invited), X. Liu, M. Fan, Y. Hu, R. Chen, F. Liu, J. Kang, Peking University

Complex multi-physics effects in advanced CMOS pose great challenges to the modeling and simulation of devices and circuits. Multi-scale and multi-physics simulation methods are proposed aiming to investigate and evaluate various reliability problems (self-heating effect, trap-induced degradation and electro-migration of interconnects) with maximum accuracy and efficiency.

11:10 a.m.
15.5 Multi-Scale Thermal Modeling of RRAM-based 3D Monolithic-Integrated Computing-in-Memory Chips, A. Ma, B. Gao, Y. Liu, P. Yao, Z. Liu, Y. Du, X. Li, F. Xu, Z. Hao, J. Tang, H. Qian, H. Wu, Tsinghua University

We demonstrated the first multi-scale thermal simulation for RRAM-based computing-in-memory chips. To achieve this, we developed a thermal modeling framework, from RRAM device to two level of circuits, 3D integration architecture, and chip package. We assess the temperature distributions under different technology nodes, different cooling methods, and different operation conditions.

11:35 a.m.
15.6 Towards accurate and efficient process simulations based on atomistic and neural network approaches, L. Li, M. Agrawal, S-Y Yeh*, K-T Lam, J. Wu*, B. Magyari-Köpe, TSMC Technology, *TSMC

Leveraging powerful new methodologies coupling machine learning and atomistic simulations, novel reaction mechanism responsible for Si growth plateau appearance in Si_{2H6} precursor depositions with H_2 carrier gas, is identified. The general workflow is transferable to any deposition and etching process optimization to enhance film quality and provide yield improvement pathways.

Session 16: SMB - RF MEMS for Communication and Sensing
Tuesday, December 6, 9:00 a.m.
Imperial Ballroom A
Co-Chairs: Philip Feng, University of Florida

Rama Ventury, Akoustic Technologies, Inc.

9:05 a.m.
16.1 XBAW, An Enabling Technology for Next Generation Resonators and Filter Solutions for 5G and Wi-Fi 6/6E/7 applications (Invited), R. Vetury, A. Kochhar, J. Shealy, Akoustis

We report XBAW, a bulk acoustic wave (BAW) manufacturing technology for Wi-Fi 6/6E/7. Performance metrics of resonators and filters on AlScN piezoelectric films on 150mm silicon substrates are reported. Trade space between Q and k_t^2 is presented. AlscN based Filters enable 160 MHz channels in UNII bands 1-8.

9:30 a.m.
16.2 3D Monolithic Integration of ScAlN-based GHz MEMS Acoustic Filters on 200mm RFSOI Wafer, Y. Zhang, X. Wang, C. Liu, Y. Woo, W. Yang, Q. Zhang, H. Lin, D. Yan, R. Kumarasamy, B. Chen, N. Wang, T. Zhu, A*star

A wafer-level 3D monolithic integration of the scandium aluminum nitride (ScAlN) based radio frequency (RF) bulk acoustic wave (BAW) filters with RF silicon-on-insulator (RFSOI) switches were demonstrated for the first time, aiming for significant reduction of footprint and parasitics for the next generation RF frontend modules in wireless communication systems.

9:55 a.m.
16.3 Multiple Stable Oscillators Referenced to the Same Multimode AlN/Si MEMS Resonator with Mode-Dependent Phase Noise and Frequency Stability, T. Kaisar, S M Enamul Hoque Yousuf, J. Lee, A. Qamar*, M. Rais-Zadeh*, S. Mandal***, P. Feng, University of Florida, *University of Michigan, **NASA JPL, ***Brookhaven National Laboratory

We report on the first experimental demonstration of multiple self-sustaining feedback oscillators referenced to a single multimode resonator, using piezoelectric aluminum nitride on silicon (AlN/Si) microelectromechanical systems (MEMS) technology. The three oscillators' overall excellent performance suggests suitability for multimode resonant sensing and tracking.

10:45 a.m.
16.4 57 GHz Acoustic Resonator with k^2 of 7.3% and Q of 56 and in Thin-Film Lithium Niobate, J. Kramer, S. Cho, M. Liao*, K. Huynh*, O. Barrera, L. Matto*, M. Goorsky*, R. Lu, The University of Texas at Austin, *University of California, Los Angeles

We report an acoustic resonator at 57 GHz with high electromechanical coupling of 7.3% and quality factor of 56, enabling a record-breaking figure of merit of 4.1. The device uses A3 mode in 110-nm 128° Y-cut lithium niobate thin film, transferred on top of sapphire substrate with intermediate amorphous silicon.

11:10 a.m.
16.5 Bit Rate-Adapting Resoswitch, Q. Jin, K. Zheng, C. Nguyen, University of California, Berkeley

A micromechanical resoswitch design and operation mode harnesses stored mechanical resonance energy to reduce its required switching energy, i.e., improve its sensitivity, while simultaneously reducing its switching time to support a bit rate of 8 kbps, which is at least 12 times faster than without pre-energization.

Session 17: RSD/MS – Focus Session - DNA Digital Data Storage, Transistor Based DNA Sequencing, and Bio-Computing
Tuesday, December 6, 9:00 a.m.

Imperial Ballroom B
Co-Chairs: Chan Lim, SK Hynix
Giuseppe Iannaccone, University of Pisa

9:05 a.m.
17.1 Advances in Electronic Nano-biosensors and New Frontiers in Bioengineering (Invited), S. Chen, M. Hwang, T. Wang*, J. Wang, A. Ganguli, I. Park**, Y. Kim, E. Valera, S W Nam***, N. Aluru#, A. van der Zande, R. Bashir, University of Illinois at Urbana-Champaign, *Gachon University, **Korea University, ***University of California, Irvine, #The University of Texas at Austin

Nano-biosensors offer unprecedented sensitivities over conventional biosensors. In this paper, we review our past work on electrical detection of bio-molecules such as DNA, proteins, and viruses using silicon field-effect transistor (FET) biosensors, crumpled graphene FETs, and solid-state nanopores. We also highlight our work on muscle-based miniature bio-robots, and neuron-based bio-computers.

9:30 a.m.
17.2 Single-molecule field-effect transistors: carbon nanotube devices for temporally encoded biosensing (Invited), D. Lynall, K. Shepard, Columbia University

Point-functionalized carbon nanotubes, known as single-molecule field-effect transistors, are capable of sensing binding events and conformational changes at the single-molecule level. Here, we demonstrate the capabilities of single-molecule field-effect transistors to measure DNA hybridization kinetics and to selectively detect small molecules through the use of a single-stranded DNA aptamer.

9:55 a.m
17.3 Wafer-scale biologically sensitive carbon nanotube FETs: from fabrication to clinical applications (Invited), Z, Zhang, M. Xiao, Peking University and Xiangtan University

Semiconducting carbon nanotubes (CNTs) have been of particular interest in applications for biosensors with high sensitiviy, selectivity, density and compatibility to micro-fabrication process. We reviews our progress in fabrication of CNT FET based bio-chemical sensors and their application in various biomarkers ultra-sensitive detection and then discuss remaining challenges.

10:20 a.m.
17.4 The Nanopore-FET as a High-Throughput Barcode Molecule Reader for Single-Molecule Omics and Read-out of DNA Digital Data Storage (Invited), K. Martens*, D. Barge, L. Liu*, S. Santermans, C. Stoquart*, J. Delport*, K. Willems*, D. Ruic*, S. Marion, J. Gevers*, B. Du Bois, A. Andrei, L. Lagae*, M. Veugelers**, A. Verhulst, S. Severi, P. Van Dorpe*, imec, *imec/KU Leuven, **KU Leuven

Nanopore technology has revolutionized DNA sequencing, and nanopore-based technology is expected to lead to revolutions in omics and DNA digital data storage. Current nanopore technology is slow due to the low ionic currents. The Nanopore Field Effect Transistor (NPFET) relies on much larger currents, enabling larger bandwidths and translocation speeds.

11:10 a.m.
17.5 DNA storage: synthesis and sequencing semiconductor technologies (Invited), D. Lavenier, CNRS - IRISA

Storing data on DNA molecules is an alternative to traditional storage media by promoting density and longevity. This paper gives an overview of how data is stored on DNA and how the reading and writing processes (sequencing and synthesis) can be implemented on semiconductor devices.

11:35 a.m.
17.6 Bacterial nanopores open the future of data storage (Invited), C. Cao, L. Krapp, A. Agerova, A. Al Ouahabi*, A. Radenovic, J-F Lutz*, M. Dal Peraro, École polytechnique fédérale de Lausanne, *Institute Charles Sadron

In the era of "big data" finding solutions for data storage is an urgent need for our society. Biological pores hold the promise to accurately decode the digital information encoded in tailored polymers opening up promising possibilities to develop writing-reading technologies to process digital data using a biological-inspired platform.

12:00 p.m.
17.7 System Design Considerations for Automated Digital Data Storage in DNA (Invited), C. Takahashi, University of Washington

Synthetic DNA is an attractive medium for long term data storage because of its density, ease of copying, and longevity. However, bringing the "wetlab" into the data center presents many challenges. Here we present an overview and highlight systems considerations when automating digital data storage in DNA.

Session 18: MT - In-Memory Computing (IMC) and Storage Class Memory (SCM)
Tuesday, December 6, 2:15 p.m.
Grand Ballroom A
Co-Chairs: Suock Chung, SK Hynix
Shosuke Fujii, Kioxia

2:20 p.m.
18.1 A Hybrid Computing-In-Memory Architecture by Monolithic 3D Integration of BEOL CNT/IGZO-based CFET Logic and Analog RRAM, R. An, Y. Li, J. Tang, B. Gao, Y. Du, J. Yao*, Y. Li, S. Wen, H. Zhao, J. Li, Q. Qin, Q. Zhang, S. Qiu*, Q. Li*, Z. Li, H. Qian, H. Wu, Tsinghua University, *Chinese Academy of Sciences, Chinese Academy of Sciences

We present a hybrid computing-in-memory (CIM) architecture, named M3D-CCP, by monolithically 3D integration of Si CMOS logic layer, RRAM-based CIM layer and processing-near-memory (PNM) layer with CNT/IGZO-based complementary field-effect transistor (CFET). An image super-resolution task was implemented using the fabricated M3D-CCP chip, achieving GPU-equivalent performance with 149× lower energy consumption.

2:45 p.m.
18.2 A > 64 Multiple States and > 210 TOPS/W High Efficient Computing by Monolithic Si/CAAC-IGZO + Super-Lattice $ZrO_2/Al_2O_3/ZrO_2$ for Ultra-Low Power Edge AI Application, M-C Chen, S. Ohshita*, S. Amano*, Y. Kurokawa*, S. Watanabe*, Y. Imoto*, Y. Ando*, W-H Hsieh, C-H Chang, C-C Wu, S-S Chuang, H Yoshida, M-C Lu, M-H Liao**, S-Z Chang, S. Yamazaki*, Powerchip Semiconductor Manufacturing Corporation, *Semiconductor Energy Laboratory Co., Ltd., **National Taiwan University

We present a novel Si/CAAC-IGZO + Super-Lattice $ZrO_2/Al_2O_3/ZrO_2$ analog in-memory computing (AiMC) chip by monolithic 3D technique with the high stability of Si/OS process. This monolithic AiMC chip achieves >64 multiple weighting states, >210TOPS/W operation energy efficiency, and an inference accuracy can keep >90% even at 125°C high temperature operation.

3:10 p.m.

18.3 Highly Reliable Physical Unclonable Functions using Memristor Crossbar with Tunneling Conduction, J. Park, T.-H. Kim*, S. Kim*, M. S. Song, S. Youn, K. Hong*, B-G Park*, H. Kim, Inha University, *Seoul National University

We present highly reliable PUF operations using Al_2O_3/TiO_x memristor crossbar arrays. The device stack was optimized in terms of stoichiometry and thickness to obtain temperature-independent *I-V* properties. Strong PUF operations were presented using crossbar, and bit-error rate was experimentally verified 0.896% at 80°C without correction methods thanks to tunneling conduction.

4:00 p.m.
18.4 Demonstration of a Multi-Level µA-Range Bulk Switching ReRAM and its Application for Keyword Spotting, Y. Wu, F. Cai, L. Thomas, T. Liu, A. Nourbakhsh, J. Hebding, E. Smith, R. Quon, R. Smith, A. Kumar, A. Pang, J. Holt, R. Someshwar, F. Nardi, J. Anthis, S-H Yen, C. Chevallier, A. Uppala, X. Chen, N. Breil, T. Sherwood, K. K. Wong, W. Cho, F. Thompson, J. J Hsu, B. Ayyagari-Sangamalli, S. Krishnan, W.D. Lu*, M. Chudzik, Applied Materials, *University of Michigan

We report a bulk ReRAM that can be programmed up to 128 levels in µA range. The device exhibits forming-free, analog switching with low noise and operating currents. A ReRAM-based SoC is built with 65nm CMOS technology, and keyword spotting is demonstrated with software equivalent accuracy and high energy efficiency.

4:25 p.m.
18.5 New Phase-Change Materials by Atomic-Level Engineering the Dopants for Extremely Low Vth Drift at 85 oC and High Endurance 3D Crosspoint Memory, H-Y Cheng, A. Grun, W-C Chien, C-W Yeh, A. Ray*, C-W Cheng*, E-K Lai, C. Lavoie*, L. Gignac*, M. Hopstaken*, I-T Kuo, C-S Hsu, L. Buzi*, R. Bruce*, D-Y Lee, N. Gong*, D. Bishop*, M. Brightsky*, H-L Lung, Macronix, *IBM

New phase-change materials from single composite target are systematically studied. It integrated with high Indium doped AsSeGe selector, demonstrates a wide V_{tS}/V_{tR} memory window, stable 1E7 chips level write cycles (using 400ns box SET) and non-detectable V_{tS} and V_{tR} drift characteristic at 85ºC/1 day in 256kbits ADM memory arrays.

4:50 p.m.
18.6 Extremely high performance, high density 20nm self-selcting cross-point memory for Compute Express Link, S. Hong, H. Choi, J. Park, Y. Bae, K. Kim, W. Lee, S. Lee, H. Lee, S. Cho, J. Ahn, S. Kim, T. Kim, M-H Na, S. Cha, SK Hynix

We demonstrate an array operation of 20 nm self-selecting memory (SSM) for the first time. SSM shows extremely high cell performance, great reliability, and promising scalability below 1z nm technodes. The innovation of material engineering enables memory-selector duality, which can reduce the aspect ratio and consequently lead to better scalability.

5:15 p.m.
18.7 Engineering defects in pristine amorphous chalcogenides for forming-free low voltage selectors, E. Ambrosi, C-H Wu, H. Lee, C-F Hsu, C-M Lee, S. Vaziri, I. Datye, Y-Y Chen, D-H Hou, P-C Chang, D. Heh, P-J Liao, T.Y. Lee, M.M.F. Chang, H.-S. P. Wong, X. Bao, TSMC

This work presents a novel approach to realize forming-free low-voltage selectors by including additional defects to pristine amorphous chalcogenides. We study the conduction and forming-free mechanisms for different defect amount. Optimized forming-free selectors based on arsenic-free SiNGeCTe are demonstrated with low initial leakage and excellent endurance over 10^{10} cycles.

Session 19: ODI - Photonic Technologies and Non-Visible Imaging
Tuesday, December 6, 2:15 p.m.
Continental Ballroom 1-3
Co-Chairs: Lucio Pancheri, University of Trento
Qing Chao, META

2:20 p.m.
19.1 Record-low Loss Non-volatile Mid-infrared PCM Optical Phase Shifter based on $Ge_2Sb_2Te_3S_2$, Y. Miyatake, K. Makino*, J. Tominaga*, N. Miyata*, T. Nakano*, M. Okano*, K. Toprasertpong, S. Takagi, M. Takenaka, The University of Tokyo, *National Institute of Advanced Industrial Science and Technology (AIST)

We propose a low-loss non-volatile PCM phase shifter operating at mid-infrared wavelengths using $Ge_2Sb_2Te_3S_2$ (GSTS), a new selenium-free widegap PCM. The GSTS phase shifter exhibit the record-low optical loss for π phase shift of 0.29 dB/π, more than 20 times better than reported so far in terms of figure-of-merit.

2:45 p.m.
19.2 Monolithic Integration of Top Si3N4-Waveguided Germanium Quantum-Dots Microdisk Light Emitters and PIN Photodetectors for On-chip Ultrafine Sensing, C-H Lin, P-Y Hong, B-J Lee, H. C. Lin, T. George, P-W Li, National Yang Ming Chiao Tung University

An ingenious combination of lithography and self-assembled growth has allowed accurate control over the geometric conditions of our "designer" Ge QDs with high-temperature thermal stability. This significant fabrication advantage has opened up the 3D integration feasibility of top-SiN waveguided Ge photonics for on-chip ultrafine sensing and optical interconnect applications.

3:10 p.m.
19.3 Colloidal quantum dot image sensors: a new vision for infrared (Invited), P. Malinowski, V. Pejovic*, E. Georgitzikis, JH Kim, I. Lieberman, N. Papadopoulos, M.J. Lim, L. Moreno Hagelsieb, N. Chandrasekaran, R. Puybaret, Y. Li, T. Verschooten, S. Thijs, D. Cheyns, P. Heremans*, J. Lee, imec, *KULeuven

Short-wave infrared (SWIR) range carries information vital for augmented vision. Colloidal quantum dots (CQD) enable monolithic integration with small pixel pitch, large resolution and tunable cut-off wavelength, accompanied by radical cost reduction. In this paper, we describe the challenges to realize manufacturable CQD image sensors enabling new use cases.

4:00 p.m.
19.4 Grating-resonance InGaAs narrowband photodetector for multispectral detection in NIR-SWIR region, J. Jang, J. Shim, J. Lim, G. C. Park*, J. Kim**, D-M Geum, S. Kim, Korea Advanced Institute of Science and Technology (KAIST), *Electronics and Telecommunications Research Institute (ETRI), **Korea Advanced Nano Fab Center (KANC)

We proposed grating-resonance narrowband photodetector for the wavelength selection functionality at the range of 1300~1700 nm. Based on parameters designed from the simulation, we fabricated an array of pixels to selectively detect different wavelengths. Our device showed great wavelength selectivity and tunability depending on grating design with a narrow FWHM.

4:25 p.m.

19.5 Alleviating the Responsivity-Speed Dilemma of Photodetectors via Opposite Photogating Engineering with an Auxiliary Light Source beyond the Chip, Y. Zou, Y. Zeng, P. Tan, X. Zhao, X. Zhou, X. Hou, Z. Zhang, M. Ding, S. Yu, H. Huang, Q. He, X. Ma, G. Xu, Q. Hu, S. Long, University of Science and Technology of China

The dilemma between responsivity and speed limits the performance of photodetectors. Here, opposite photogating engineering was proposed to alleviate this dilemma via an auxiliary light source beyond the chip. Based on a WSe_2/Ga_2O_3 JFET, a $>10^3$ times faster speed towards deep ultra-violet has been achieved with negligible sacrifice of responsivity.

4:50 p.m.
19.6 Experimental Demonstration of the Small Pixel Effect in an Amorphous Photoconductor using a Monolithic Spectral Single Photon Counting Capable CMOS-Integrated Amorphous-Selenium Sensor, R. Mohammadi, P. M. Levine, K. S. Karim, University of Waterloo

We directly demonstrate, for the first time, the small pixel effect in an amorphous material, a-Se. The results are also the first demonstration of the transient response of a-Se monolithically combined with a CMOS, with and without SPE, and the first aSe/CMOS PHS results, offering a-Se/CMOS for photon counting applications.

¶Session 20: ALT - 3D Stacked Transistor Architectures
Tuesday, December 6, 2:15 p.m.
Continental 4
and

2:20 p.m.
20.1 Heterogeneous 3D Sequential CFET with Ge (110) Nanosheet p-FET on Si (100) bulk n-FET by Direct Wafer Bonding, Seong Kwang Kim, Hyeong-Rak Lim, Jaejoong Jeong, Seung Woo Lee, Joon Pyo Kim, Jaeyoung Jeong, Bong Ho Kim, Seung-Yeop Ahn, Youngkeun Park, Dae-Myoung Geum, Younghyun Kim*, Yongku Baek, Byung Jin Cho, and Sang Hyeon Kim, Korea Advanced Institute of Science and Technology (KAIST), *Hanyang University

We demonstrated 3D sequential complementary field-effect-transistor (CFET) by direct wafer bonding (DWB) technique and a low-temperature process for monolithic 3D (M3D) integration using a high-performance top Ge (110)/<110> channel on bottom Si CMOS. In addition, we obtained record high mobility of approximately 400 $cm^2/V{\cdot}s$ among the reported Ge pFET

2:45 p.m.
20.2 First Demonstration of Heterogeneous L-shaped Field Effect Transistor (LFET) for Angstrom Technology Nodes, C.-Y. Yang, P.-J. Sung*, M.-H. Chuang, C.-W. Chang, Y.-J. Shih, T.-Y. Huang, D. D. Lu, T.-C. Hong**, X.-R. Yu, W.-H. Lu, S.-W. Chang, J.-J. Tsai, M.-K. Huang, T.-C. Cho*, Y.-J. Lee*, K.-L. Luo*, C.-T. Wu*, C.-J. Su**, K.-H. Kao, T.-S. Chao**, W.-F. Wu*, Y.-H. Wang, Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan; *Taiwan Semiconductor Research Institute, Hsinchu, Taiwan; **National Yang Ming Chiao Tung University

This study proposes and demonstrates a novel heterogeneous L-shaped FET (LFET) structure consisting of a vertical Ge pFET above a lateral Si nFET. The fabrication challenges of the heterogeneous CFET structure, consisting of a lateral Ge pFET and a lateral Si nFET, are greatly alleviated with the new LFET design.

3:10 p.m.

20.3 First Demonstration of Monolithic 3D Self-aligned GeSi Channel and Common Gate, Complementary FETs by CVD Epitaxy Using Multiple P/N Junction Isolation, Chien-Te Tu, Yi-Chun Liu, Bo-Wei Huang, Yu-Rui Chen, Wan-Hsuan Hsieh, Chung-En Tsai, Shee-Jier Chueh, Chun-Yi Cheng, Yichen Ma, and C. W. Liu, National Taiwan University

Monolithic 3D self-aligned $Ge_{0.75}Si_{0.25}$ nanosheet CFETs with P/N junction isolation by CVD epitaxy are experimentally demonstrated. The triple P/N junctions suppress leakage current without extra dielectrics. The stacked GeSi nanosheet pFETs on GeSi nanosheet nFETs without wafer bonding, dielectric isolation, and epi regrowth can simplify the process for transistor stacking.

4:00 p.m.
20.4 Monolithic 3D Integration of Vertically Stacked CMOS Devices and Circuits with High-Mobility Atomic-Layer-Deposited In_2O3 n-FET and Polycrystalline Si p-FET: Achieving Large Noise Margin and High Voltage Gain of 134 V/V, W. Tang, Z. Lin, Z. Wang, Z. Lin*, L. Feng**, Z. Liu**, X. Li***, P. D. Ye*, X. Guo, M. Si, Shanghai Jiao Tong University, *Purdue University, **Hangzhou LinkZill Technology Co., Ltd., ***Huazhong University of Science and Technology

In this work, we demonstrate the monolithic 3D integration of vertically stacked p-type LTPS top-gate transistor and n-type back-gate oxide semiconductor transistor. High-performance logic devices and circuits are demonstrated with a high voltage gain of 134.3 V/V and a large noise margin of 0.84 V at V_{DD} of 2 V.

4:25 p.m.
20.5 Integration Design and Process of 3-D Heterogeneous 6T SRAM with Double Layer Transferred Ge/2Si CFET and IGZO Pass Gates for 42% Reduced Cell Size, X.-R. Yu, M.-H. Chuang*, S.-W. Chang, W.-H. Chang***, T.-C. Hong**, C.-H. Chiang*, W.-H. Lu , C.-Y. Yang, W.-J. Chen, J.-H. Lin^^, P.-H. Wu^, T.-C. Sun, S. Kola*, Y.-S. Yang*, Yun Da*, P.-J. Sung**, C.-T. Wu**, T.-C. Cho**, G.-L. Luo**, K.-H. Kao, M.-H. Chiang, W. C.-Y. Ma^^, C.-J. Su**, T.-S. Chao^, T. Maeda***, S. Samukawa*, Y. Li*, Y.-J. Lee**, W.-F. Wu**, J.-H. Tarng*, Y.-H. Wang, National Cheng Kung University, *College of Electrical and Computer Engineering, National Yang Ming Chiao Tung University, **Taiwan Semiconductor Research Institute (TSRI), ***National Institute of Advanced Industrial Science and Technology (AIST), ^National Yang Ming Chiao Tung University, ^^Sun Yat-Sen University

A new integration design and process for SRAM with a highly 3-D vertically stacked structure of the CFET inverter and IGZO pass gate is proposed. We fabricated single crystalline Ge/2Si heterogeneous CFET. Furthermore, an IGZO nFET is fabricated as an additional pass gate (PG) after the CFET structure is fabricated.

4:50 p.m.
20.6 Top-Gate CVD WSe_2 pFETs with Record-High I_d~594 µA/µm, Gm~244 µS/µm and WSe_2/MoS_2 CFET based Half-adder Circuit Using Monolithic 3D Integration, Xiong Xiong, Shiyuan Liu, Honggang Liu**, Yang Chen**, Xinhang Shi**, Xin Wang**, Xuefei Li**, Ru Huang, and Yanqing Wu, Peking University, *Beijing Advanced Innovation Center for Integrated Circuits, **Huazhong University of Science and Technology

We demonstrate monolithic 3D CFET based on CVD 2D materials channels for low-power ICs. The top-gate bilayer WSe_2 pFET exhibits a record-high I_{on} of ~594 µA/µm and G_m of ~244 µS/µm. Furthermore, the CFET inverters with rail-to-rail operations are achieved to establish the SRAM and half-adder circuits with footprint reduction.

¶Session 21: FS-MT-EDT: Special Topics in Non-Von Neumann Computing

Tuesday, December 6, 9:00 a.m.
Continental Ballroom 5
Jianshi Tang, Tsinghua University and Sapan Agarwal, Sandia National Labs

2:20 p.m.
21.1 Training-to-Learn with Memristive Devices (Invited), Zhenming Yu, Nathan Leroux, Emre Neftci, Forschungszentrum Juelich

This work combines a phenomenological model of the device and bi-level optimization to pre-train the neural network to be insensitive to memristor device non-idealities on learning tasks.

2:45 p.m.
21.2 Energy-efficient activity-driven computing architectures for edge intelligence (Invited), Shih-Chii Liu, Chang Gao, Kwantae Kim, Tobi Delbruck, University of Zurich & ETH Zurich

We present an overview of brain-inspired features incorporated into high energy-efficient tiny deep network accelerators. We show that by using network architectures with states, the number of computes can be further reduced. When interfaced to an activity-driven sensor, these devices can further reduce the computes for solving a task.

3:10 p.m.
21.3 Multistable neuromorphic computing: controlling attractor switches using waveforms (Invited), Joshua Chang, David Paydarfar, John Milton, The University of Texas at Austin

An important question in designing multistable neuromorphic computing devices is how best to switch between attractors. We demonstrate that waveform-based stimuli are more energy-efficient than single pulses and can target all attractors, allowing for the possibility of developing non-von Neumann neuromorphic circuit architectures that incorporate both digital and analog components.

4:00 p.m.
21.4 Life is probabilistic - Why should all our computers be deterministic? Computing with p-bits: Ising Solvers and Beyond (Invited), Jan Kaiser, Supriyo Datta, Behtash Behin-Aein*, Purdue University, *Ludwig Computing

Many problems in life are probabilistic; even deterministic problems are often solved using probabilistic algorithms. Anytime conventional computers are used to process uncertain data or to implement algorithms that leverage randomness, there is a mismatch between software and hardware that can be avoided using a probabilistic processor built from p-bits.

4:25 p.m.
21.5 Ferroelectric FET Configurable Memory Arrays and Their Applications (Invited), Dayane Reis, Ann Franchesca Laguna*, Mengyuan Li**, Michael Niemier**, X. Sharon Hu**, University of South Florida, *De La Salle University, **University of Notre Dame

Configurable memory arrays (CMAs) execute various operations (e.g., searches, lookups, Boolean logic) in one in-memory-computing (MC) structure benefiting many applications. Emerging non-volatile devices, e.g., Ferroelectric FET (FeFETs) can lead to denser, lower-energy CMAs. This paper presents FeFET-based CMAs, and demonstrates the utility of CMA-based IMC architectures through application case studies.

4:50 p.m.

21.6 Scalable In-Memory Computing Architectures for Sparse Matrix Multiplication (Invited), Jack Kendall, Alexander Conklin, Ross Pantone, Juan Nino, Suhas Kumar, Rain Neuromorphics

We present two novel memory-dense and fully parallel architectures for analog sparse matrix multiplication: one based on memristive nanowires, and the other based on 3D lithographic memristors, both realized on a CMOS-integrated chip, Cumulus. We experimentally demonstrate accurate generation of deterministic chaotic signals via an echo state network on Cumulus.

5:15 p.m.
21.7 Subthreshold operation of SONOS analog memory to enable accurate low-power neural network inference (Invited), V. Agrawal, T. P. Xiao*, C. H. Bennett*, B. Feinberg*, S. Shetty, K. Ramkumar, H. Medu, K. Thekkekara, R. Chettuvetty, S. Leshner, Z. Luzada, L. Hinh, T. Phan, M. J. Marinella**, and S. Agarwal*, Infineon Technologies, *Sandia National Laboratories, **Arizona State University

Hardware accelerators that exploit analog in-memory computing offer an energy-efficient edge deployment solution for machine learning algorithms. We give an overview of the device requirements and hardware-software co-design principles for these systems to achieve efficient and accurate deep neural network (DNN) inference.

5:40 p.m.
21.8 Analog Compute-in-Memory For AI Edge Inference (Invited), Dave Fick, Mythic

The information age has ushered in a wave of data at both the cloud and on the edge. Engineers have created new algorithms to identify higher-level information within this data, which often involves scanning with increasingly complex pattern recognition systems. Compute-in-Memory (CiM) is an architectural strategy that seeks to optimize these important applications by computing at the memory instead of inefficiently shuffling data to/from a CPU. This paper surveys a few of these techniques, then dives into analog CiM (ACiM) for edge AI, specifically looking at the Mythic M1076.

¶Session 22: EDT - Quantum-Inspired and Emerging Technologies
Tuesday, December 6, 2:15 p.m.
Continental
Bogdan Govoreanu, IMEC and Kerem Camsari, UCSB

2:20 p.m.
22.1 Methodology for an efficient characterization flow of industrial grade Si-based qubit devices, L.C. Contamin, B. Cardoso Paz*, B. Martinez Diaz**, B. Bertrand, H. Niebojewski, V. Labracherie, A. Sadik, E. Catapano, M. Casse, E. Nowak, Y.-M. Niquet**, F. Gaillard, T. Meunier*, P.-A. Mortemousque, M. Vinet, CEA-Leti, **CNRS Neel Institute, **CEA-Irig, and Univ. Grenoble Alpes

We present here our fast characterization methodology for qubit devices, and wafer-level measurements on different qubit-array structures at both 300K and 1K. They are crucial for process evaluation as well as device screening before continuing to mK characterization. We measure and extract, for the first time, wafer-level quantum dot metrics.

2:45 p.m.
22.2 An efficient synchronous updating memristor-based Ising solver for combinatorial optimization, Mingrui Jiang, Keyi Shan, Xia Sheng*, Cat Graves*, John Paul Strachan**, Can Li, The University of Hong Kong, *Hewlett Packard Labs, **Forschungszentrum Juelich

Existing memristor-based solvers update node states asynchronously by performing matrix multiplication column-by-column. This work experimentally demonstrates solving the optimization problems with a synchronous-updating memristor-based Ising solver with physics-inspired annealing, saving more than 5× time and 35× energy consumption for a 60-node Max-cut problem when compared to the state-of-the-art mem-HNN solver.

3:10 p.m.
22.3 Enhancement in Capacitance and Transconductance in 90 nm nFETs with HfO_2-ZrO_2 Superlattice Gate Stack for Energy-efficient Cryo-CMOS, W. Li, L. C. Wang, S. S. Cheema, N. Shanker, C. Hu, S. Salahuddin, University of California, Berkeley

The negative-capacitance mixed-ferroic HfO_2-ZrO_2 superlattice (HZH) gate stack on SOI nFETs shows dispersion-free capacitance enhancement (<8 Å EOT) over regular HfO_2 high-κ gate stack up to 40 GHz down to 77 K. The resulted charge boost and unaffected injection velocity at low temperatures are highly beneficial for energy-efficient Cryo-CMOS.

4:00 p.m.
22.4 Experimental evaluation of simulated quantum annealing with MTJ-augmented p-bits, Andrea Grimaldi, Kemal Selcuk, Navid Anjum Aadit, Keito Kobayashi*, Qixuan Cao, Shuvro Chowdhury, Giovanni Finocchio, Shun Kanai*, Hideo Ohno*, Shunsuke Fukami*, Kerem Y. Camsari, University of California Santa Barbara, *Tohoku University

We present the first experimental demonstration of a probabilistic computer where a stochastic magnetic tunnel junction drives a powerful CMOS-based field programmable gate array (FPGA) in a heterogeneous compute fabric. We then show a systematic evaluation of the simulated quantum annealing algorithm for hard combinatorial optimization problems using an emulator.

4:25 p.m.
22.5 Scalable In-Memory Clustered Annealer with Temporal Noise of FinFET for the Travelling Salesman Problem, Anni Lu, Jae Hur, Yuan-Chun Luo, Hai Li*, Dmitri Nikonov*, Ian Young*, Yang-Kyu Choi**, Shimeng Yu, Georgia Institute of Technology, *Intel Corporation, **Korea Advanced Institute of Science and Technology

We propose a scalable in-memory annealer for solving the large-scale travelling salesman problem (TSP) using a hierarchical clustered approach, based on a Hopfield neural network (HNN) implemented with a crossbar array of FinFET, using its intrinsic temporal noise of the drain current caused by trapping/detrapping to realize the annealing process.

4:50 p.m.
22.6 Steep-Slope Negative Quantum Capacitance Field-Effect Transistor, Yafen Yang, Kai Zhang, Yi Gu, Parameswari Raju*, Qiliang Li*, Li Ji, Lin Chen, Dimitrios Ioannou**, Qingqing Sun, David Wei Zhang, Hao Zhu, Fudan University, *NIST, **George Mason University

For the first time, we report the design and fabrication of a steep-slope negative quantum capacitance field-effect transistor (NQCFET) with a single-layer (SL)-graphene encapsulated in the gate stack of a MoS_2 FET. Sub-thermionic steep switching is achieved with a minimum subthreshold slope (SS) of 31 mV/dec with negligible hysteresis.

5:15 p.m.

22.7 ITO Schottky Diode wth *f*T Beyond 400 GHz: Exploring Thickness Depdendant Film Property and Novel Heterogeneous Design, Kaizhen Han, Chengkuan Wang, Yuye Kang, Long Liu, Gong Zhang, Yue Chen, Xiao Gong, University of Singapore

A strong thickness dependent characteristic was unleashed for indium-tin-oxide (ITO) thin film entering sub-10 nm regime: a property transition from metal-like to SEMI-like. A novel heterogeneous design was further proposed for ITO Schottky diode, achieving a rectifying ratio of 5 orders and a record high cut-off frequency of 422 GHz.

¶Session 23: ALT - Design-Technology CoOptimization and System Technology CoOptimization
Tuesday, December 6, 2:15 p.m.
Continental Ballroom 7-9
Lars Liebmann, Intel and You-seok Suh, Qualcomm

2:20 p.m.
23.1 Forksheet FETs with Bottom Dielectric Isolation, Self-Aligned Gate Cut, and Isolation between Adjacent Source-Drain Structures, H. Mertens, R. Ritzenthaler, Y. Oniki, P. Puttarame Gowda, G. Mannaert, F. Sebaai, A. Hikavyy, E. Rosseel, E. Dupuy, A. Peter, K. Vandersmissen, D. Radisic, B. Briggs, D. Batuk, J. Geypen, G. Martinez-Alanis, F. Seidel, O. Richard, B.T. Chan, J. Mitard, E. Dentoni Litta, N. Horiguchi, imec

We report on forksheet field-effect transistors that are isolated from the substrate by bottom dielectric isolation formed by replacing a SiGe epitaxial layer with a dielectric film while the devices are anchored to the substrate by forksheet walls. Functional forksheet devices with BDI are demonstrated for 10nm wall width.

2:45 p.m.
23.2 Semi-damascene Integration of a 2-layer MOL VHV Scaling Booster to Enable 4-track Standard Cells, V. Vega-Gonzalez, D. Radisic, S. Choudhury, D. Tierno, A. Thiam, D. Batuk, G.T. Martinez, F. Seidel, S. Decoster, S. Kundu, D. Tsvetanova, A. Peter, H. de Coster, A. Sepulveda-Marquez, E. Altamirano-Sanchez, BT Chan, Y. Drissi, Y. Sherazi, J. Uk-Lee, I. Ciofi, G. Murdoch, N. Nagesh, G. Hellings, J. Ryckaert, S. Biesemans, E. Dentoni Litta, N. Horiguchi, S. Park, Zs. Tőkei, imec

An innovative semi-damascene integration scheme enabling the new 4-track standard-cell routing architecture called VHV relevant for the beyond-2nm node is demonstrated. The required boundary between cells is built with two vias with zero-line extension facing each other and an aggressive T2T=8.9nm in between, all self-aligned to the top 18nm-pitch layer.

3:10 p.m.
23.3 Insights into Scaled Logic Devices Connected from Both Wafer Sides, A. Veloso, G. Eneman, P. Matagne, B. Vermeersch, A. Jourdain, H. Arimura, B. O'Sullivan, R. Chen, A. De Keersgieter, E. Simoen, D. Radisic, Y. Oniki, A. Laffitte*, S. Brus, E. Beyne, E. Dentoni Litta, N. Horiguchiimec, *Grenoble INP – Phelma

A thorough evaluation of finFETs connected from both wafer sides via BPR, on ≠ thinned Si substrates and various layouts, including zero BPR trench-fin lateral distance. Post-BS anneal optimization with HPA → lower temperature FGA. Further IR drop improvements, self-heating of BPR NSFET configurations, BS source contact considerations also explored.

4:00 p.m.

23.4 Power, Performance, Area and Thermal Analysis of 2D and 3D ICs at A14 Node Designed with Back-side Power Delivery Network, R. Chen, M. Lofrano, G. Mirabelli, G. Sisto, S. Yang, A. Jourdain, F. Schleicher, A. Veloso, O. Zografos, P. Weckx, G. Hiblot, G. Van der Plas, G. Hellings, J. Ryckaert, E. Beyne, imec

Impact of using BSPDN for CPUs of 2D and 3D designs in the aspects of power, performance, area and thermal (PPAT) is evaluated. 46% and 9% improvement in IR drop and performance respectively and 8% core area scaling is found for BSPDN while thermal performance is ~45% worse than FSPDN.

4:25 p.m.
23.5 Cryo-Computing for Infrastructure Applications: A Technology-to-Microarchitecture Co-optimization Study, Divya Prasad, Manoj Vangala, Mudit Bhargava, Arnout Beckers*, Alexander Grill*, Davide Tierno*, Krishnendra Nathella, Thanusree Achuthan**, David Pietromonaco, James Myers**, Matthew Walker**, Bertrand Parvais*, Brian Cline, Arm Inc., *imec, **Arm Ltd.

A system-technology co-optimization of cryogenic (100-150K) HPC designs is proposed. Device and circuit-level optimizations are considered for logic and memory (SRAM and eDRAM) circuits. Up to 16X performance/watt benefit is demonstrated at system level, at a projected cooling cost of 4X.

4:50 p.m.
23.6 AI Computing in Light of 2.5D Interconnect Roadmap: Big-Little Chiplets for In-memory Acceleration, Zhenyu Wang, Gopikrishnan Raveendran Nair, Gokul Krishnan, Sumit K. Mandal*, Ninoo Cherian, Jae-sun Seo, Chaitali Chakrabarti, Umit Y. Ogras*, Yu Cao, Arizona State University, *University of Wisconsin-Madison

This pathfinding work explores heterogeneous chiplets with 2.5D interconnect for AI computing. Our benchmark tool, SIAM, integrates the roadmap of 2.5D interconnect and in-memory computing to illustrate the required bandwidth for various AI models. We further propose the big-little chiplets to map the non-uniformity in algorithms for high energy efficiency.

¶Session 24: SMB - Novel Sensors and Architectures for Biology
Tuesday, December 6, 2:15 p.m.
Imperial A
Arvind Balijepalli, NIST and Xiaoting Jia, Virginia Tech

2:20 p.m.
24.1 Biochemical spectroscopy based on germanium-on-insulator platform for mid-infrared optical sensor, Jinha Lim, Joonsup Shim, Inki Kim, Seong Kwang Kim, Hyeongrak Lim, Seung-Yeop Ahn, Juhyuk Park, Dae-Myeong Geum, Sanghyeon Kim, Korea Advanced Institute of Science and Technology (KAIST)

We demonstrated Ge-OI gas sensor for MIR biochemical sensing. Ge-OI we fabricated by wafer bonding and electron-beam lithography. Ge-OI sensor had low loss (1.88 dB/cm) and high confinement factor (44.3%). For compact footprint, spiral structure with a 20-mm-length of 3.5-mm^2-area was fabricated. Sensitivity and LoD were 0.0885%/ppm and 8.5 ppm.

2:45 p.m.
24.2 High-Resolution DNA Binding Kinetics Measurements with Double Gate FD-SOI Transistors, Seulki Cho, Alexander Zaslavsky, Curt Richter, Jacob Majikes, J. Alexander Liddle, Francois Andrieu*, Sylvain Barraud*, Arvind Balijepalli, NIST, *CEA Leti, University of Grenoble Alpes

Double gate fully-depleted SOI transistors operating in a remote gate configuration and under closed-loop feedback allow noise performance that exceeds their single gate counterparts by more than an order of magnitude. This high performance enabled measurements of DNA binding in real-time with a limit of detection of ~ 100 fM.

3:10 p.m.
24.3 Flexible, Transparent, Active-Matrix Tactile Sensor Interface Enabled by Solution-Processed Oxide TFTs, Yingjie Tang, Dingwei Li, Yan Wang, Fanfan Li, Yitong Chen, Kun Liang, Huihui Ren, Chunyan Song, Hong Wang*, and Bowen Zhu, Westlake University, *Xidian University

In this work, we demonstrate a flexible, transparent, active-matrix (AM) tactile sensor array (TSA) by monolithically integrating solution-processed indium oxide (In_2O_3) thin-film transistor (TFT) array with a highly pressure-sensitive micro-pyramidal film. The In_2O_3 TFTs exhibit excellent uniformity by process optimization, enabling a prototypical 10×10 AM-TSA for user-interactive sensor interfaces.

4:00 p.m.
24.4 Spike-based Beamforming using pMUT Arrays for Ultra-Low Power Gesture Recognition, E. Hardy, B. Fain, T. Mesquida*, F. Blard, F. Gardien, F. Rummens*, J.C. Bastien, J.R. Chatroux, S. Martin, V. Rat, and E. Vianello, CEA-Leti, University of Grenoble Alpes, *CEA-List, University of Grenoble Alpes

We propose the first end-to-end Ultra-low Power Gesture Recognition system comprising an array of emitting and receiving piezoelectric micromachined ultrasonic transducers, driving/sensing electronics, a novel spike-based beamforming strategy without conventional analog-to-digital converters and a spiking recurrent neural network. We experimentally demonstrate an accuracy of 86.0% on a five gestures dataset.

4:25 p.m.
24.5 Novel Energy-efficient Hafnia-based Ferroelectric Processing-in-Sensor with *in-situ* Motion Detection and Four-quarter Mutipilcation, Zhiyuan Fu, Kaifeng Wang, Boyi Fu, Shaodi Xu, Hao Zheng, Jin Luo, Chang Su, Weikai Xu, Xiao Lv, Qianqian Huang, Ru Huang, Peking University

This work reports first experimental demonstration of CMOS-compatible FE-HZO based non-volatile PIS array and IR response by utilizing its pyroelectric effect, enabling zero-power sense and inference with in-situ-motion detection and four-quarter-multilevel multiplication by one FE-capacitor. Moreover, high-accuracy motion pattern recognition are demonstrated, showing great potential for compact and efficient edge-AI.

Session 26: MT - Charge-Based Memories
Wednesday, December 7, 9:00 a.m.
Grand Ballroom A
Shyam Raghunathan, Micron and Subhali Subhechha, imec

9:05 a.m.
26.1 3D NAND scaling in the next decade (Invited), Russ Meyer, Yoshiaki Fukuzumi, Yingda Dong, Micron Technology Inc.

As 3D NAND enters its second decade of scaling we must continue to develop solutions to maintain the cost and performance improvement trajectories. Looking forward, the scaling vectors that reduce the stack height demands are crucial for the economic viability of the roadmap.

9:55 a.m.

26.2 FinFETs with Thermally Stable RMG Gate Stack for Future DRAM Peripheral Circuits, E. Capogreco, H. Arimura, R. Ritzenthaler, S. Brus, Y. Oniki, E. Dupuy, F. Sebaai, D. Radisic, B. T. Chan, D. Zhou, V. Machkaoutsan*, S. Yoon**, H. Itokawa***, M. Yamaguchi***, Z. Gao^, P. Fazan*, Y. Chen^, S. Subramanian, L.-Å. Ragnarsson, A. Spessot, E. Dentoni Litta, and N. Horiguchi, imec, *assignee at imec from Micron, **SK-Hynix, ***Kioxia, ^Western Digital

In this work, a 14-nm-node RMG high-k Last FinFET flow, compatible with the high thermal budget required during a DRAM fabrication process is demonstrated for the first time. A thermally stable nMOS gate stack featuring La-dipole and TiN/TiAl/TiN WFMs is proposed to achieve sub 0.2 V nMOS V_t.

10:45 a.m.
26.3 A 3D Stackable DRAM: Capacitor-less Three-Wordline Gate-Controlled Thyristor (GCT) RAM with >40μA Current Sensing Window, >10^{10} Endurance, and 3-second Retention at Room Temperature, Wei-Chen Chen, Hang-Ting Lue, Meng-Yan Wu, Teng-Hao Yeh, Pei-Ying Du, Tzu-Hsuan Hsu, Chih-Chang Hsieh, Keh-Chung Wang, Chih-Yuan Lu, Macronix International Co.

A novel capacitor-less three-wordline gate-controlled thyristor RAM is reported featuring >2V hysteresis, > 40μA current sensing window, good retention (~3sec at RT), and no degradation within 10^{10} cycling test. We propose a 3D architecture leveraging the technology of stacked nanosheet and 3D NAND to realize a highly layer-stackable 3D DRAM.

11:10 a.m.
26.4 First Demonstration of Dual-Gate IGZO 2T0C DRAM with Novel Read Operation, One Bit Line in Single Cell, I_{ON}=1500 μA/μm@VDS=1V and Retention Time>300s, Wendong Lu, Zhengyong Zhu*, Kaifei Chen, Menggan Liu, Bok-Moon Kang*, Xinlv Duan, Jiebin Niu, Fuxi Liao, Wang Dan*, Xie-Shuai Wu*, Joohwan Son*, De-Yuan Xiao**, Gui-Lei Wang*, Abraham Yoo**, Kan-Yu Cao**, Di Geng, Nianduan Lu, Guanhua Yang, Chao Zhao*, Ling Li, and Ming Liu, Institute of Microelectronics, Chinese Academy of Sciences, *Beijing Superstring Academy of Memory Technology, **ChangXin Memory Technologies, Inc.

We propose and experimentally demonstrate one novel dual-gate (DG) IGZO 2T0C cell design for high-density and high-performance DRAM application.

11:35 a.m.
26.5 Inter-Layer Dielectric Engineering for Monolithic Stacking 4F^2-2T0C DRAM with Channel-All-Around (CAA) IGZO FET to Achieve Good Reliability (>10^4s Bias Stress, >10^{12} Cycles Endurance), Chuanke Chen, Kailiang Huang*, Xinlv Duan, Guanhua Yang, Junxiao Feng*, Ying Sun*, Congyan Lu, Guangfan Jiao*, Shihui Yin*, Jiazhen Sheng*, Weiliang Jing**, Zhengbo Wang*, Jeffrey Xu*, Di Geng*, Ling Li* and Ming Liu, Institute of Microelectronics of the Chinese Academy of Sciences, *Huawei Technologies Co., Ltd.

To address the stacking requirement of 4F^2 2T0C DRAM, the effect of ILD on CAA-IGZO FETs has been studied. By using optimized ILD and IGZO deposition cycle ratio, FET with high reliability is obtained. Device exhibits a ΔV_{th} of <25mV after 10^4s bias stress and no significant degradation after 10^{12}cycles-endurance.

12:00 p.m.
26.6 Optimized IGZO FETs for Capacitorless DRAM with Retention of 10 ks at RT and 7 ks at 85 °C at Zero V_{hold} with Sub-10 ns Speed and 3-bit Operation, Qianlan Hu, Qijun Li*, Shenwu Zhu*,

Chengru Gu*, Shiyuan Liu, Ru Huang, Yanqing Wu, Peking University, *Huazhong University of Science and Technology

IGZO transistor with ultra-low off-state current and excellent on-state current is adopted as write transistor of capacitorless DRAM cells to experimentally demonstrate the remarkable retention time over 10 ks with record high-speed of 10 ns, as well as the 3-bit operation at room-temperature and 85 ℃ for the first time.

Session 27: ALT - CMOs Scaling and Platforms
Wednesday, December 7, 9:00 a.m.
Grand Ballroom B
Namoi Yoshida, Applied Materials and Robert Clark, Tokyo Electron

9:05 a.m.
27.1 Critical Process Features Enabling Aggressive Contacted Gate Pitch Scaling for 3nm CMOS Technology and Beyond, Chih-Hao Chang, V.S. Chang, K.H. Pan, K.T. Lai, J. H. Lu, J.A. Ng, C.Y. Chen, B.F. Wu, C.J. Lin, C.S. Liang, C.P. Tsao, Y.S. Mor, C.T. Li, T.C. Lin, C.H. Hsieh, P.N. Chen, H.H. Hsu, J.H. Chen, H.F. Chen, J.Y. Yeh, M.C. Chiang, C.Y. Lin, J.J. Liaw, C.H. Wang, S.B. Lee, C.C. Chen, H.J. Lin, R. Chen, K.W. Chen, C.O. Chui, Y.C. Yeo, K.B. Huang, T.L. Lee, M.H. Tsai, K.S. Chen, Y.C. Lu, S.M. Jang, and S.-Y. Wu, TSMC

We report a leading-edge CMOS technology at 45nm contacted gate pitch that incorporates optimized fin profile, low-k spacer and self-aligned contact. The process is validated by logic test chip with >3.5 billion transistors and fully functioning 256Mb HC/HD SRAM macros. The 0.0199μm^2 HD SRAM is the smallest reported to date.

9:30 a.m.
27.2 18nm FDSOI Enhanced Device Platform for ULP/ULL MCUs, Olivier Weber, Doohong Min*, Alexandre Villaret, Jinha Park*, Ilmin Lee*, Eric Vandenbossche, Dohun Kim*, Jiyoung Yun*, Jinwoo Park*, Minuk Lee*, Jinseok Kang*, Hyunjong Lee*, Youngju Choi*, Inhwan Kim*, Joochan Kim*, Dhori Kedar, Janardan, Sebastien Haendler, Salim Elghouli, Sophie Puget, Christophe Bernicot, Emilie Bernard, François Wacquant, Fabien Nimsgern, Joonhyuk Choi*, Shigenobu Maeda*, Jongho Lee* and Franck Arnaud, STMicroelectronics, *Samsung Electronics Co.

We report for the first time multiple FDSOI device innovations which have been implemented in the 18nm technology platform. 4 mixable Vts, high performance at low voltage (+80% wrt 28nm FDSOI at Vdd=0.6V) and low retention leakage (0.6pA at Vdd=0.55V) in high density SRAM bitcells have been demonstrated.

9:55 a.m.
27.3 Enabling Next Generation 3D Heterogeneous Integration Architectures on Intel Process, A. Elsherbini, K. Jun, S. Liff, T. Talukdar, J. Bielefeld, W. Li, R. Vreeland, H. Niazi, B. Rawlings, T. Ajayi, N. Tsunoda, T. Hoff, C. Woods, G. Pasdast, S. Tiagaraj, E. Kabir, Y. Shi, W. Brezinski, R. Jordan, J. Ng, X. Brun, B. Krisnatreya, P. Liu, B. Zhang, Z. Qian, M. Goel, J. Swan, G. Yin, C. Pelto, J. Torres, P. Fischer, Intel Corporation

This paper discusses a new generation of heterogeneous integration architectures which we refer to as quasi-monolithic chips (QMC). We show the main structural elements of the architecture and its performance including 9x+ interconnect power reduction and density improvements. We also cover the main new process modules needed to enable QMC.

10:45 a.m.

27.4 High Performance 5G mobile SoC Design-Technology Co-Optimization for PPA and Manufacturability with 5nm EUV FinFET technology, Youseok Suh, Jerry Bao, Vicki Lin, Wade Kuo*, Leo Kim**, Ying Chen, Hao Wang, Yandong Gao, Jason Cheng, Xiao-Yong Wang, Hyuk Park***, Hochul Lim***, Sungwon Kim***, Hun Shin***, Byungmoo Song***, Yuri Y. Masuoka***,Taegyun Kim***, Ja-Hum Ku***, Giri Nallapati, Sam Yang, PR. Chidambaram, Qualcomm Technologies Inc., *Qualcomm Semiconductor Limited, **Qualcomm Korea YH, ***Samsung Electronics

We report on Snapdragon® 888, the first integrated 5G modem SoC Flagship Platform for premium tier smartphones using 5nm EUV FinFET technology. It exhibits >20% CPU performance gain over its predecessor Snapdragon 865 thanks to new design architecture and multiple process improvements. Low voltage operation/consumption are achieved with further Design-Technology-Co-Optimization.

11:10 a.m.
27.5 A 3nm CMOS FinFlex™ Platform Technology with Enhanced Power Efficiency and Performance for Mobile SoC and High Performance Computing Applications (Late News), Shien-Yang Wu, C.H. Chang, M.C. Chiang, C.Y. Lin, J.J. Liaw, J.Y. Cheng, J.Y. Yeh, H.F. Chen, S.Y. Chang, K.T. Lai, M.S. Liang, K.H. Pan, J.H. Chen, V.S. Chang, T.C. Luo, X. Wang, Y.S. Mor, C.I. Lin, S.H. Wang, M.Y. Hsieh, C.Y. Chen, B.F. Wu, C.J. Lin, C.S. Liang, C.P. Tsao, C.T. Li, C.H. Chen, C.H. Hsieh, H.H. Liu,
P.N. Chen, C.C. Chen, R. Chen, Y.C. Yeo, C.O. Chui, W. Chang, T.L. Lee, K.B. Huang, H.J. Lin, K.W. Chen, M.H. Tsai, K.S. Chen, X.M. Chen, Y.K. Cheng, C.H. Wang, W. Shue, Y. Ku, S. M. Jang, M. Cao, L.C. Lu, T.S. Chang, Taiwan Semiconductor Manufacturing Company

The 3nm CMOS platform technology with FinFlex™ standard cells innovation is presented to offer the critical design flexibility for better power efficiency and performance optimization. About 1.6X logic density increase, 18% speed improvement and 34% power reduction are achieved over our previous 5nm CMOS process to unleash product innovations.

Session 28: MS - 2D Materials: Devices and Contacts
Wednesday, December 7, 9:00 a.m.
Continental Ballroom 1-3
Zlatan Stanojevic, Global TCAD Solutions and Mincheol Shin, KAIST

9:05 a.m.
28.1 Computational Screening and Multiscale Simulation of Barrier-Free Contacts for 2D Semiconductor pFETs, Ning Yang, Yuxuan Cosmi Lin, Chih-Piao Chuu, Saifur Rahman*, Tong Wu**, Ang-Sheng Chou, San-Lin Liew, Kohei Fujiwara***, Hung-Yu Chen, Junya Ikeda***, Atsushi Tsukazaki***, Duen-Huei Hou, Wei-Yen Woon, Szuya Liao, Shengxi Huang*, Xiaofeng Qian^, Jing Guo**, Iuliana Radu, H.-S. Philip Wong, Han Wang, TSMC, *Pennsylvania State University, **University of Florida, ***Tohoku University, ^Texas A&M University

We computationally screen and identify designs for ultralow-resistance p-type contacts to 2D semiconductors such as WSe_2. Two new contact strategies, van der Waals metallic contact (such as 1H-NbS_2), and bulk semimetallic contact (such as $Co_3Sn_2S_2$), are identified as realistic pathways to achieving Schottky-barrier-free and low-contact-resistance p-type contacts for 2D pFETs.

9:30 a.m.
28.2 *Ab-initio* transport simulations unveil the Schottky versus Tunneling barrier trade-off in metal-TMD contacts, Daniel Lizzit, Pedram Khakbaz, Francesco Driussi, Marco Pala, David Esseni, University of Udine, Universit´e Paris-Saclay

We investigate metal-2D semiconductor contacts with an in-house developed, *ab-initio* quantum transport methodology. We found that a trade-off exists between Schottky and Tunneling barriers and this sets the minimum contact resistance. We show calculations for the bismuth-MoS_2 system for *n*-type contacts and investigate Au-WSe_2 for a low resistance *p*-type contact.

9:55 a.m.
28.3 *Ab initio* quantum transport simulations of defective devices based on 2-D materials *via* a projected-GW approach, G. Gandus, J. Cao, T. Agarwal*, M. Luisier, Y. Lee, ETH Zurich, *Indian Institute of Technology Gandhinagar

We propose an ab initio defect modeling framework for defective devices based on two-dimensional (2-D) materials. The so-called projected-GW method is combined with density functional theory and incorporated into the quantum transport equations. It can efficiently and accurately investigate the characteristics of defective 2-D FETs through quasi-particle correlated defect-level modeling.

10:45 a.m.
28.4 Comprehensive Physics Based TCAD Model for 2D MX_2 Channel Transistors, D. Mahaveer Sathaiya, Terry Y.T. Hung, Edward Chen, Wen-Chia Wu*, Aslan Wei, Chih-Piao Chuu, Sheng-Kai Su, Ang Sheng Chou, Cheng-Ting Chung, Chao-Hsin Chien*, Han Wang, Jin Cai, Chung -Cheng Wu, Iuliana P. Radu, and Jeff Wu, Taiwan Semiconductor Manufacturing Company, *National Yang Ming Chiao Tung University

For the first time, a comprehensive TCAD model is developed to unambiguously extract key device parameters: R_c, μ_{CH}, SBH, & D_{it} from experimental data on back-gate transistors with MX_2 channel. Analyzed the accuracy of R_c and μ_{CH} extracted by TLM method and provide guidance on the limits of its applicability.

11:10 a.m.
28.5 Characterization and Closed-Form Modeling of Edge/Top/Hybrid Metal-2D Semiconductor Contacts, Arnab Pal, Varun Mishra*, Justin Weber*, Karthik Krishnaswamy*, Krishnendu Ghosh*, Ashish Verma Penumatcha*, Salim Berrada*, Kevin O'Brien*, David Kencke**, and Kaustav Banerjee, University of California, Santa Barbara, *Intel Corporation

Employing ab-initio techniques, the first comprehensive analyses of electrical contact topologies to two-dimensional atomically-thin layered-semiconductors are evaluated and closed-form models for contact resistance are presented for the first time. The closed-form models allow rapid metal-2D contact design evaluations to identify optimal contact topologies and process conditions that satisfy IRDS requirements.

Session 29: FS-SMB - Emerging Implantable-Device Technology
Wednesday, December 7, 9:00 a.m.
Continental Ballroom 4
Xiaoting Jia, Virginia Tech and Francesca Santoro, FZ Juelich

9:05 a.m.
29.1 Optogenetic Neural Probes: Fiberless, High-Density, Artifact-Free Neuromodulation (Invited), Eunah Ko, Kanghwan Kim, Mihály Vöröslakos, Sungjin Oh, György Buzsáki*, Kensall D. Wise, and Euisk Yoon, University of Michigan, *New York University

Evolution of "Michigan Probes" has enabled unraveling the connectivity of neurons at cellular resolution and their dynamic interaction that underlie behavioral and cognitive functions. Recent development of high-

density micro-LED optoelectrodes will be presented along with discussion of technical challenges in scaling of optogenetic probes and future directions.

9:30 a.m.
29.2 Soft Wireless Optogenetic and Hybrid Implants for Advanced Neural Interfacing (Invited), J.-W. Jeong, Korea Advanced Institute of Science and Technology (KAIST)

Unveiling the functions of the brain can open new opportunities for neuroscience research and therapeutic applications. Here, we present soft wireless optogenetic and hybrid implants that overcome limitations of conventional neural tools to enable highly precise, target-specific neuromodulation and neural activity monitoring for advanced neural interfacing.

9:55 a.m.
29.3 Bilayer-Nanomesh Transparent Neuroelectrodes on 10μm-Thick PDMS (Invited), Jaehyeon Ryu, Yi Qiang*, Dongyeol Jang*, Junyeub Suh**, Hui Fang*, Northeastern University, *Dartmouth College, **Samsung Electronics

Here, we report an ultra-soft and thin-film microelectrode array in the Polydimethylsiloxane (PDMS) film with Au/PEDOT: PSS electrode that retains excellent electrochemical properties with single neuron scale dimensions.

10:45 a.m.
29.4 Biodegradable Implantable Microsystems (Invited), J. Park, J. Brugger, Ecole Polytechnique Fédérale de Lausanne (EPFL)

Biodegradable implanted devices and microsystems are candidates to fulfill the utmost required in-vivo assistance for a variety of envisioned bio-medical health care applications. They range from monitoring biomarkers, recording, and stimulation, to local drug administration. Ideally, the implants bring minimal invasive damage but have maximum interaction with the surrounding tissue.

11:10 a.m.
29.5 The Future of Holistic Neural Interfaces: 2D Materials, Neuromorphic Computing, and Computational Co-Design (Invited), M. Wilson, M. Ramezani, J. Kim, D. Kuzum, University of California, San Diego

The next leap in neural interfaces requires advances in materials, devices, and computing paradigms. Integration of optical and electrical sensing using 2D materials and neuromorphic computing can overcome spati o temporal resolution limits. We present recent advances in multimodal recordings, on-chip neural signal processing and computational co-design for minimally invasive neural interfaces.

11:35 a.m.
29.6 Channels, Layout and Size Scalability of Implantable CMOS-Based Multielectrode Array Probes (Invited), J. F. Ribeiro, G. Angotzi, A. Perna, M. Vincenzi, G. Orban, F. Boi, L. Berdondini, Fondazione Istituto Italiano di Tecnologia

Micro-structured monolithic CMOS devices enable the integration of dense microelectrode arrays and on-chip circuits for low-power implantable brain interfaces with single neuron spatiotemporal resolution. Here, we demonstrate the scalability of SiNAPS CMOS-probe technology with respect to different probe layouts, array sizes and shank dimensions down to microwire size ranges.

12:00 p.m.

29.7 Increasing the Lifetime of the Implantable Neural Devices (Invited), C. K. Nguyen, B. Srikanthan*, R. Bhandari*, S F. Cogan, and S. Negi*, University of Texas at Dallas, *Blackrock Neurotech

Brain implants with complex 3D geometries provide a challenge for current encapsulation techniques. Parylene has been the gold standard for encapsulation , however, recording capabilities show signs of degradation within 6 months. Silicon Carbide is studied as an encapsulation material designed to extend the long-term stability and implantable lifetime.

12:25 p.m.
29.8 A Transient, Closed-Loop Network of Wireless, Body-Integrated Devices for Autonomous Electrotherapy (Invited), J.A. Rogers, Northwestern University

Traditional systems for the care of cardiac patients involve expensive, complex collections of wired hardware for continuous monitoring and autonomous treatment. The work described here demonstrates an approach that exploits a collection of small wireless wearables for monitoring cardiac activity and delivering cardiac stimulation through an implanted, bioresorbable, battery-free pacemaker.

Session 30: RSD - Reliability of Transistor Technology
Wednesday, December 7, 9:00 a.m.
Continental 5
William Vandendaele, CEA-Leti and Byoung Min, GlobalFoundries

9:05 a.m.
30.1 Characterizing and Modelling of the BTI Reliability in IGZO-TFT using Light-assisted I-V Spectroscopy, Z. Wu, A. Chasin, J. Franco, S. Subhechha, H. Dekkers, Y.V. Bhuvaneshwari, A. Belmonte, N. Rassoul, M.J. van Setten, V. Afanas'ev*, R. Delhougne, B. Kaczer, G.S. Kar
imec, *KU Leuven

The sub-gap Density-of-State in IGZO-TFT is investigated using Light-assisted-I-V-Spectroscopy(LaIVs), which quantifies the sub-gap DoS of pristine and electrically stressed IGZO-TFTs. By combining LaIVs with I-V modelling, charge trapping and DoS changes during PBTI are decoupled. Their time/voltage evolutions are revealed, allowing to project the I-V degradations to any stress time/voltages.

9:30 a.m.
30.2 New Insights into the Impact of Hydrogen Evolution on the Reliability of IGZO FETs: Experiment and Modeling, Qiwen Kong, Gan Liu*, Chen Sun, Zijie Zheng, Dong Zhang, Jishen Zhang, Haiwen Xu, Long Liu, Zuopu Zhou, Leming Jiao, Xiaolin Wang, Kaizhen Han, Yuye Kang, Bich-Yen Nguyen*, Kai Ni**, and Xiao Gong, National University of Singapore; *Soitec, **Rochester Institute of Technology

In this work, we report a comprehensive and deep understanding of the impact of hydrogen evolution on the reliability of the Indium-Gallium-Zinc-oxide (IGZO) FETs with HfO_2 gate dielectric. We innovate in combining negative bias stress (NBS) and positive bias temperature instability (PBTI) with a unique physics-based model proposed.

9:55 a.m.
30.3 Reliability of Atomic-Layer-Deposited Gate-All-Around In_2O_3 Nano-Ribbon Transistors with Ultra-High Drain Currents, Z. Zhang, Z. Lin, A. Charnas, H. Dou, Z. Shang, J. Zhang1, M. Si, H. Wang, M. A. Alam and P. D. Ye, Purdue University

In this work, we systematically investigate the reliability of atomic-layer-deposited (ALD) gate-all-around (GAA) single-channel In_2O_3 nano-ribbon field-effect transistors (FETs) with a maximum on-state current approaching 20 mA/μm. A counter-intuitive positive/negative threshold voltage shift under negative/positive gate bias stress is observed universally in all GAA In_2O_3 FETs.

10:45 a.m.
30.4 Low thermal budget PBTI and NBTI reliability solutions for multi-V_{th} CMOS RMG stacks based on atomic oxygen and hydrogen treatments, J. Franco, H. Arimura, J.-F. de Marneffe, D. Claes, S. Brus, A. Vandooren, E. Dentoni Litta, N. Horiguchi, K. Croes, B. Kaczer, imec

We demonstrate an atomic oxygen PBTI treatment, which combined with our atomic hydrogen NBTI treatment provides a complete low thermal budget BTI solution for Sequential 3D integration and tightly spaced nanosheets. We deploy these low-temperature treatments with different WFM stacks and explain the fundamental correlation between effective WF and reliability.

11:10 a.m.
30.5 New insights on the excess 1/f noise at cryogenic temperatures in 28 nm CMOS and Ge MOSFETs for quantum computing applications, R. Asanovski, A. Grill*, J. Franco*, P. Palestri**, A. Beckers*, B. Kaczer* and L. Selmi, Universit`a degli Studi di Modena e Reggio Emilia, *imec, **Universit`a degli Studi di Udine

We extensively characterize noise on a commercial 28 nm CMOS technology as well as on Ge channel devices at temperatures ranging from 370 K down to 4 K. Our investigations give fundamental insights into the origin of the excess 1/f noise (deviating from linear temperature scaling) at cryogenic temperatures.

11:35 a.m.
30.6 Back Barrier Trapping Induced Resistance Dispersion in GaN HEMT: Mechanism, Modeling, and Solutions, Hao Yu, B. Parvais, U. Peralagu, R. Y. ElKashlan, R. Rodriguez, A. Khaled, S. Yadav, A. Alian, M. Zhao, N. de Almeida Braga*, J. Cobb*, J. Fang*, P. Cardinael, A. Sibaja-Hernandez, and N. Collaert, imec, *Synopsys

Trapping in back barrier (BB) of GaN HEMTs causes on-resistance (R_{on}) dispersion. We demonstrate that BB trapping is alleviated by increasing 2DEG density N_{sh} (~50% increased N_{sh} with ~30% less ΔR_{on}) and inserting AlGaN BB (100 nm AlGaN with ~50% less ΔR_{on}). We propose a novel AlGaN/C-GaN BB designing criterion.

12:00 p.m.
30.7 Comprehensive Investigations of HBM ESD Robustness for GaN-on-Si RF HEMTs, S. Abhinay, W.-M. Wu, C.-A. Shih, S.-H. Chen, A. Sibaja-Hernandez, B. Parvais, U. Peralagu, A. Alian, T.-L. Wu*, M.-D. Ker*, G. Groeseneken, N. Collaert, imec, *National Yang Ming Chiao Tung University

Experimental studies and simulations elaborate on the impact of different stress scenarios on ESD robustness of GaN-on-Si RF HEMTs. The different discharge paths for each HBM stress scenario determine its robustness. Transient HBM *I-V* characteristics have been verified with TCAD and indicate 3 different failure mechanisms in GaN RF HEMTs.

12:25 p.m.
30.8 Novel all-around diamond integration with GaN HEMTs demonstrating highly efficient device cooling, R. Soman, M. Malakoutian, B. Shankar, D. Field*, E. Akso**, N. Hatui**, N. J. Hines***, S. Graham^, U. K. Mishra**, M. Kuball*, and S. Chowdhury, Stanford University, *University of Bristol, **UCSB, Santa Barbara, ***Georgia Institute of Technology, ^University of Maryland

A novel all-around heat spreader for GaN HEMTs is implemented by integrating it with polycrystalline diamond to facilitate hot-spot removal at the device level. Devices with only 500nm-thick all-around diamond, exhibited 98±19°C lower gate temperature at 9.5W/mm DC power compared to devices without diamond, without any degradation in electrical performances.

Session 31: SMB - Advanced Photonics and Electronics Sensing
Wednesday, December 7, 9:00 a.m.
Continental Ballroom 6
Wen Li, Michigan State University and

9:05 a.m.
31.1 Towards Functional Metamaterials and Metadevices, Xin Zhang, Zhiwei Yang, Yuwei Huang, Boston University

Metamaterials are a unique set of artificial materials which exhibit non-naturally occurring properties, whereby the precise tailoring of these materials enables versatile control over the propagation of electromagnetic waves. Recent trends in metamaterials research have advanced towards the realization of functional and modular metamaterials that enable real-time control over their optical properties, which has led to innovations in the field of active and tunable metamaterials via external stimuli such as electrical regulation, magnetic fields, thermal gradients, and optical pulses. The application of microsystems-based technologies has become a featured method to enrich the functionality and tunability of metamaterials and the corresponding metadevices. Here, we report our recent progress on dynamic, functional metamaterials with the help of microsystem technologies and discuss the outlook and challenges for the future of functional metamaterials and metadevices.

9:30 a.m.
31.2 Innovative Gas Sensing Method Using Transient Behavior of FET-type Sensors with Gate Pulse Input, Gyuweon Jung, Jaehyeon Kim, Wonjun Shin, Seongbin Hong, Yujeong Jeong, Chayoung Lee, Woo Young Choi, Jong-Ho Lee, Seoul National University

We propose a new gas sensing method using the transient behaviors of FET-type gas sensors with gate pulse input. This method enables the sensor to detect the target gas in 1 s while consuming only 2.8 mJ and identify 25 distinct gas mixtures using a single gas sensor.

9:55 a.m.
31.3 Reconfigurable and In-sensor Computing Pb-free Perovskite Array towards Intelligent X-ray Imaging, Guan-Hua Dun, Ken Qin, Ze-Shu Wang, Xiang-Shun Geng, Yuan-Yuan Li, Peng Wan, Yi-Chu He, Ren-Rong Liang, Dan Xie, He Tian, Yi Yang, Tian-Ling Ren, Tsinghua University

We demonstrate the first X-ray band in-sensor computing Pb-free perovskite array. X-ray detection sensitivity is 2 order larger than commercial a-Se sensors, and detection limit is 2 order lower than medical requirement. The array enables a 98.2% accuracy for chest recognition. Our results contribute to high-performance and intelligent X-ray imaging.

10:45 a.m.
31.4 A 2T2R1C vision cell with 140 dB dynamic range and event-driven characteristic for in-sensor spiking neural network, Yue Zhou,*, Jiawei Fu, Tianqing Wan*, Lin Xu*, Sijie Ma*, Jiewei Chen*, Xiangshui Miao, Yuhui He, and Yang Chai*, Huazhong University of Science and Technology, *The Hong Kong Polytechnic University

We demonstrate a 2T2R1C vision cell as sensor and synapse for spike neural network with event-driven characteristics. Our 2T2R1C cell is based on MoS_2 phototransistors that inherently have ultra-large dynamic range (140dB). The phototransistors have modulated photoresponvity by configuring different gate voltage, making the cell function as synaptic weights.

11:10 a.m.
31.5 A New Self-Powered Wireless Sensing Circuitry for On-Wafer In-Situ EUV Detection, Wei-Hwa Lin, Li Ci Chen, Ming-Han Ho, Hong-Shen Chen, Yu-Lun Hu, Burn Jeng Lin, Pin-Jiun Wu*, Jenny Yi-Chun Liu, Yue-Der Chih**, Jonathen Chang**, Jiaw-Ren Shih, Chrong Jung Lin and Ya-Chin King, National Tsing Hua University (NTHU), *National Synchrotron Radiation Research Center (NSRRC), **Taiwan Semiconductor Manufacturing Company (TSMC)

A on-wafer self-powered wireless sensing module for EUV lithographic process is proposed. A surface sensing pad controlled oscillator oscillate at a frequency proportional to the EUV intensity, where its signal is transmitted through an on-chip antenna. Therefore, the sensor module can provide wireless EUV monitoring across wafer in lithographic chambers.

Session 32: RSD - Reliability of Ferroelectric Devices

9:05 a.m.
32.1 Highly Reliable, Scalable, and High-Yield $HfZrO_x$ FRAM by Barrier Layer Engineering and Post-Metal Annealing, Yu-De Lin, Po-Chun Yeh, Jheng-Yang Dai, Jian-Wei Su, Hsin-Hui Huang*, Chen-Yi Cho*, Ying-Tsan Tang**, Tuo-Hung Hou, Shyh-Shyuan Sheu, Wei-Chung Lo, and Shih-Chieh Chang, Industrial Technology Research Institute, *National Yang Ming Chiao Tung University, **National Central University

A reliable $HfZrO_x$ FRAM technology showing endurance up to 10^{12} cycles and 10^{10} cycles at 27°C and 120°C (unit area 0.36 μm^2) has been demonstrated. The improved endurance is accomplished through barrier layer engineering of TiON and 400°C-post-metal annealing. Wake-up-free 4 Kb 1T1C FRAM chips show a high initial yield(98%).

9:30 a.m.
32.2 Deep Understanding of Reliability in Hf-based FeFET during Bipolar Pulse Cycling: Trap Profiling for Read-After-Write Delay and Memory Window Degradation, Puyang Cai, Tianxiang Zhu, Jiahui Duan*,3, Zixuan Sun, Hao Li, Yongkang Xue**, Zhiwei Liu**, Hao Xu*, Liangliang Zhang, Xiaolei Wang*, Zhigang Ji**, Runsheng Wang, Ru Huang, Peking University, *Chinese Academy of Sciences, **Shanghai Jiao Tong University

This work is focused on the read-after-write delay and MW degradation of FeFET. Two types of traps are identified to be responsible for these two reliability issues by trap dynamics investigation. Further, through the trap energy profile, the behaviors of two types of traps during cycling are clarified in detail.

9:55 a.m.
32.3 Temperature-dependent Defect Behaviors in Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Thin Film: Re-wakeup Phenomenon and Underlying Mechanisms, Xiaopeng Li, Jixuan Wu, *, Lu Tai, Wei Wei,*, Pengpeng Sang, Yang Feng, Bo Chen, Guoqing Zhao, Xuepeng Zhan, Xiaolei Wang*, Masaharu Kobayashi**, Jiezhi Chen, Shandong University, Qingdao, *Institute of Microelectronics of Chinese Academy of Sciences, **The University of Tokyo

Aiming at deep insights into the defect behaviors in ferroelectric HZO film, a systematical study in 7nm HZO at a high-temperature range is done. The re-wakeup phenomenon is observed with cycling operation

at high temperatures.The underlying mechanisms are discussed and the electron injection at grain boundary could be the reason.

10:45 a.m.
32.4 Direct Quantitative Extraction of Internal Variables from Measured PUND Characteristics Providing New Key Insights into Physics and Performance of Silicon and Oxide Channel Ferroelectric FETs, Matthias Passlack, Nujhat Tasneem*, Zheng Wang*, Khandker A. Aabrar**, Jae Hur*, Hang Chen*, Vincent D.-H. Hou, Chih-Sheng Chang, Meng-Fan Chang, Shimeng Yu*, Winston Chern*, Suman Datta**, Asif Khan*, Taiwan Semiconductor Manufacturing Company, *Georgia Tech, **University of Notre Dame

We propose a new approach where *internal* distributed variables of ferroelectric FETs (FEFET) are directly extracted from measured positive-up negative-down (PUND) FEFET and ferroelectric capacitor P-V data. Quantitative energy band diagrams (EBDs) reveal the detailed device physics by providing *interna*l device quantities including potential, polarization, carrier density, and defect density.

11:10 a.m.
32.5 Novel Opposite Polarity Cycling Recovery (OPCR) of $HfZrO_2$ Antiferroelectric-RAM with an Access Scheme Toward Unlimited Endurance, K.-Y. Hsiang, Y.-C. Chen*, F.-S. Chang, C.-Y. Lin, C.-Y. Liao, Z.-F. Lou, J.-Y. Lee, **, W.-C. Ray, Z.-X. Li, C.-C. Wang, H.-C. Tseng, P.-H. Chen, J.-H. Tsai, M. H. Liao**, T.-H. Hou*, C. W. Liu**, P.-T. Huang*, P. Su*, and M. H. Lee, National Taiwan Normal University, *National Yang Ming Chiao Tung University, **National Taiwan University

Opposite polarity cycling recovery (OPCR) and comprehensive model are proposed to completely restore a fatigued AFE capacitor back to initial-state and aspiring to unlimited-endurance. Experimental validation is demonstrated for $>5\times10^{11}$ cycles with nondegradation and restoration of Pr, and its access scheme is revealed for 1T1C AFE-RAM with alternate polarity operation.

11:35 a.m.
32.6 Investigation of Defect Engineering Toward Prolonged Endurance for HfZrO Based Ferroelectric Device (Invited), J.H. Lee, C.H. Chou, P.J. Liao, Y.K. Chang, H.H. Huang*, T.Y. Lin*, Y.S. Liu, C.H. Nien, D.H. Hou, T.H. Hou*, and Jun He, Taiwan Semiconductor Manufacturing Company, *National Yang Ming Chiao Tung University

This paper reports defect analyses of IL and HfZrO stacks from high-endurance FE devices. We validated the critical roles to enhance device endurance by inserting optimized IL with fast de-trapping behavior and doped-HZO with highly conductive grain boundary. In this work, FE device with promising defect engineering can achieve endurance~$5x10^{11}$.

12:00 p.m.
32.7 Total Ionizing Dose Effect in Tri-gate Silicon Ferroelectric Transistor Memory, Khandker Akif Aabrar, James Read*, Sharadindu Gopal Kirtania, Sergei Stepanoff**, Douglas E. Wolfe**, Shimeng Yu* and S. Datta, University of Notre Dame, *Georgia Institute of Technology, **Pennsylvania State University

For the first time, we demonstrate the survivability of programmed states in a FeFET memory under gamma-ray irradiation. The un-irradiated FeFET shows a large memory window, a high current window, a long retention & high endurance. Under radiation, retain current window $>10^2$ up to a high radiation dose of 10Mrad.

12:25 p.m.

32.8 The Role of Interface Dynamics on the Reliability performance of BEOL Integrated Ferroelectric HfO2 Capacitors, R. Alcala, P.D. Lomenzo, T. Mittmann, B. Xu, R. Guido, S. Lancaster, P. Vishnumurthy, L. Grenouillet*, S. Martin*, J. Coignus*, T. Mikolajick, U. Schroeder, NaMLab/TU Dresden gGmbH, *CEA, LETI, Univ. Grenoble Alpes

A complete picture of the dynamics of the ferroelectric oxide/metal interface is presented, which unifies the main reliability issues, cycling endurance and retention for HfO_2¬based films in ferroelectric random-access memory. Together with a novel retention interpretation, the interface is established as the key component for HfO_2-based ferroelectrics for commercial memories.

Session 33: MT - In-Memory Computing (IMC)
Wednesday, December 5, 1:30 p.m.
Grand Ballroom A
Hsiang-Lan Lung, Macronix and Martin Frank, IBM

1:35 p.m.
33.1 Gradient descent-based programming of analog in-memory computing cores, J. Büchel, A. Vasilopoulos, B. Kersting, F. Odermatt, K. Brew*, I. Ok*, S. Choi*, I. Saraf*, V. Chan*, T. Philip*, N. Saulnier**, V. Narayanan**, M. Le Gallo, A. Sebastian, IBM Research Europe, Rüschlikon, *IBM Research – Albany, **IBM Research – Yorktown Heights

Precise programming of crossbar arrays is crucial for high matrix-vector-multiplication (MVM) accuracy in analog in-memory computing cores. By minimizing the MVM error using gradient descent, our method significantly reduces the MVM error compared with conventional iterative programming, eliminates the need for high-resolution ADCs, and improves the experimental accuracy of ResNet-9.

2:00 p.m.
33.2 Hybrid Precoding with a Fully-Parallel Large-Scale Analog RRAM Array for 5G/6G MIMO Communication System, Qi Qin, Bin Gao, Qi Liu, Zhengwu Liu, Yudeng Lin, Peng Yao, Ying Zhou, Ruihua Yu, Zhenqi Hao, Jianshi Tang, Qingtian Zhang, Linglong Dai, Zhiqiang Su*, Qingqing Xu*, Shujuan You*, Huaqiang Wu, and He Qian, Tsinghua University, *China Mobile Research Institute

For the first time, an energy-efficient hybrid precoding with computing-in-memory technology for 5G/6G MIMO communication system is demonstrated. We realize the first fully-parallel large-scale (128K) analog RRAM array. To address the IR-drop issue in the fully-parallel large-scale arrays, a compact model and compensation scheme are proposed.

2:25 p.m.
33.3 Analog Computing in Memory (CIM) Technique for General Matrix Multiplication (GEMM) to Support Deep Neural Network (DNN) and Cosine Similarity Search Computing using 3D AND-type NOR Flash Devices, Ming-Liang Wei, Hang-Ting Lue, Shu-Yin Ho, Yen-Po Lin,2, Tzu-Hsuan Hsu, Chih-Chang Hsieh, Yung-Chun Li, Teng-Hao Yeh, Shih-Hung Chen, Yi-Hao Jhu, Hsiang-Pang Li, Han-Wen Hu, Chun-Hsiung Hung, Keh-Chung Wang, and Chih-Yuan Lu, Macronix International Co., Ltd

We propose an analog in-memory computing technique using 3D NOR Flash devices to support general-purpose matrix multiplication for AI inference and data search. It supports ResNet-50 inference throughput >300 frame/sec with Top-5 accuracy ~90% on ImageNet. It offers feature-searching bandwidth of ~5Tb/s/chip with ~0.2% accuracy loss on VGGFace2 dataset.

3:15 p.m.

33.4 MRAM In-memory computing macro for AI computing (Invited), Seungchul Jung, Sang Joon Kim, Samsung Electronics

In-memory computing is one of the most progressive attempts in AI acceleration. The key embodiment is the crossbar array of conductive memories which stores neural net weights and performs MAC operations in an analog manner. Here we innovate device and circuit solutions to develop the first MRAM crossbar array.

3:40 p.m.
33.5 First Demonstration of Homomorphic Encryption using Multi-Functional RRAM Arrays with a Novel Noise-Modulation Scheme, Xueqi Li, Bin Gao, Bohan Lin, Ruihua Yu, Han Zhao, Ze Wang, Qi Qin, Jianshi Tang, Qingtian Zhang, Xinyi Li, Zhenqi Hao, Xiaotao Li*, Dequn Kong*, Liqiu Ma*, Ning Deng, He Qian, and Huaqiang Wu, Tsinghua University, *China Mobile Research Institute

Homomorphic encryption is firstly implemented on RRAM arrays, which are utilized as both MVM units and TRNG. Both high stability and good randomness are achieved by using different forming schemes. Furthermore, the encryption-decryption process for privacy-preserving cloud computing is experimentally implemented on a hardware system with eight 144Kb RRAM arrays.

4:05 p.m.
33.6 An Analog In-Memory-Search Solution based on 3D-NAND Flash Memory for Brain-Inspired Computing, Po-Hao Tseng, Yu-Hsuan Lin, Tian-Cih Bo, Feng-Ming Lee, Yu-Yu Lin, Ming-Hsiu Lee, Kuang-Yeu Hsieh, Keh-Chung Wang, Chih-Yuan Lu, Macronix International Co., Ltd.

We present a high performance 3D-NAND-flash-based analog in-memory-searching (AIMS) chip, which enables novel searching/matching functionality in analog domain. It can perform ultra-high parallel in-memory similarity searching with digital or analog output. The AIMS chip can mimic the operations as human brain, and enables many applications with AI and memory-centric computing.

4:30 p.m.
33.7 Deep learning acceleration in 14nm CMOS compatible ReRAM array: device, material and algorithm co-optimization, N. Gong, M.J. Rasch, S.-C. Seo*, A. Gasasira*, P. Solomon, V. Bragaglia**, S. Consiglio***, H. Higuchi***, C. Park*, K. Brew*, P. Jamison*, C. Catano***, I. Saraf*, F.F. Athena, C. Silvestre*, X. Liu*, B. Khan, N. Jain*, S. Mcdermott*, R. Johnson*, I. Estrada-raygoza*, J. Li*, T. Gokmen, N. Li, R. Pujari*, F. Carta, H. Miyazoe, M.M. Frank, D. Koty***, Q. Yang***, R. Clark***, K. Tapily***, C. Wajda***, A. Mosden***, J. Shearer***, A. Metz***, S. Teehan*, N. Saulnier*, B. J. Offrein**, T. Tsunomura^, G. Leusink***, V. Narayanan, T. Ando, IBM Thomas J. Watson Research Center, * IBM Research, **IBM Research–Zurich, ***TEL Technology Center, America, LLC ^Tokyo Electron Limited

We co-optimize ReRAM material and training algorithm using 14nm CMOS based ReRAM arrays and achieve a FP comparable accuracy on reduced MNIST classification using open-loop and parallel training. Our simulation based on array-level statistical data shows that the improvement from the co-optimized material and algorithm extends to larger DNN workloads.

Session 34: ALT - Advanced CMOS: Technology and Devices
Wednesday, December 7, 1:30 p.m.
Grand Ballroom B
Francois Andrieu, CEA-Leti and Anne Vandooren, IMEC

1:35 p.m.

34.1 Low temperature source / drain epitaxy and functional silicides: essentials for ultimate contact scaling, C. Porret, J.-L. Everaert, M. Schaekers, L.-A. Ragnarsson, A. Hikavyy, E. Rosseel, G. Rengo, R. Loo, R. Khazaka*, M. Givens*, X. Piao, S. Mertens, N. Heylen, H. Mertens, C. Toledo de Carvalho Cavalcante, G. Sterckx, S. Brus, A. Nalin Mehta, M. Korytov, D. Batuk, P. Favia, R. Langer, G. Pourtois, J. Swerts, E. Dentoni Litta and N. Horiguchi, Imec, *ASM

Low temperature source-drain processes are associated with exploratory contacts to alleviate access resistance issues. TiN/W stacks demonstrate sub $1x10^{-9}$ $\Omega.cm^2$ contact resistivity extraction capability. Sc/Si:P contacts yield ~ $1.3x10^{-9}$ $\Omega.cm^2$ (35% reduction versus Ti/Si:P reference), confirming sufficient doping in Si:P. Analyses reveal reaction mechanisms responsible for this improvement.

2:00 p.m.
34.2 Record 7(N)+7(P) Multiple V_Ts Demonstration on GAA Si Nanosheet n/pFETs using WFM-Less Direct Interfacial La/Al-Dipole Technique, Jiaxin Yao, Yanzhao Wei, Shuai Yang, Hong Yang, Gaobo Xu, Yadong Zhang, Lei Cao, Xuexiang Zhang, Qianqian Liu, Zhenhua Wu, Huaxiang Yin, Qingzhu Zhang, Junfeng Li, Jun Luo, Chinese Academy of Sciences

In this paper, for the first time, we have realized record 7(N)+7(P) multiple threshold voltages ($V_{<TS}$) on horizontal gate-all-around (GAA) Si nanosheet (SiNS) n/pFETs using work-function-metal-less (WFM-less) direct interfacial La/Al-dipole technique. The maximum V_T tuning ranges reach 1105mV/873mV and the minimum discriminated ΔV_T over 83mV/76mV for n/pFETs.

2:25 p.m.
34.3 CMOS Demonstration of Negative Capacitance HfO_2-ZrO_2 Superlattice Gate Stack in a Self-Aligned, Replacement Gate Process, N. Shanker, M. Cook*, S.S. Cheema*, W. Li, R. Rastogi*, D. Pipitone*, C. Chen*, M. Smith*, S. Meninger*, F. Bauer*, G. Pinelli*, J. Hunt* S. Salahuddin, M. Mohamed*, University of California, Berkeley, *Massachusetts Institute of Technology

We report on the successful integration of a low EOT negative capacitance (NC) gate stack – a 1.8 nm HfO_2-ZrO_2 superlattice (HZH) – into a 90 nm CMOS R&D technology. The integrated gate oxides show an effective oxide thickness (EOT) of 7.5 Å on both p- and n-SOI MOSFETs.

3:15 p.m.
34.4 Hardware Based Performance Assessment of Vertical-Transport Nanosheet Technology (Invited), G. Tsutsui, S. Song*, J. Strane, R. Xie, L. Qin, C. Zhang, D. Schmidt, S. Fan, B. Hong*, Y. Jung*, C-W. Sohn*, I. Hwang*, J. Yim*, G. H. Son*, G. Jo*, K-I. Kim*, M. Sankarapandian, S. Mochizuki, I. Seshadri, E. Miller, J. Li, J. Demarest, C. Waskiewicz, R. G. Southwick, H. Zhou, R. N. Pujari, P. Nieves, M. Wang, H. Jagannathan, B. Anderson, D. Guo, R. Divakaruni, T. Wu, K-I. Seo*, and H. Bu, IBM, *Samsung Electronics

Vertical-transport FET (VTFET) has its advantage on area scaling, which enables to scale logic area beyond sub-45nm contacted gate pitch (CGP). This paper focuses on VTFET performance assessment. 1.2x effective capacitance contrasting to technology target is demonstrated based on 40CGP VTFET ring oscillator. 90% DC performance is demonstrated as well.

3:40 p.m.
34.5 First Demonstration of GAA Monolayer-MoS_2 Nanosheet nFET with 410 µA/µm I_D at 1V V_D at 40nm gate length, Yun-Yan Chung, Bo-Jhih Chou*, Chen-Feng Hsu, Wei-Sheng Yun, Ming-Yang Li, Sheng-Kai Su, Yu-Tsung Liao*, Meng-Chien Lee*, Guo-Wei Huang, San-Lin Liew, Yun-Yang Shen*, Wen-Hao Chang*, Chien-Wei Chen**, Chi-Chung Kei**, Han Wang, H.-S. Philip Wong, T. Y. Lee, Chao-Hsin Chien*, Chao-Ching Cheng, Iuliana P. Radu, Taiwan Semiconductor Manufacturing

Company, *National Yang Ming Chiao Tung University, **Taiwan Instrument Research Institute, National Applied Research Laboratories

Demonstrates first monolayer MoS_2 nanosheet FET in a gate-all-around configuration. At a L_G of 40nm, transistor exhibits a remarkable I_{ON} ~410 μA/μm at V_{DS} = 1V, achieved large I_{ON}/I_{OFF}>1E8, V_{TH} ~1.4 V with nearly zero DIBL. We propose a fully integrated flow and detail the feasibility of critical modules.

4:05 p.m.
34.6 FDSOI for cryoCMOS electronics: device characterization towards compact model (Invited), M. Casse, B. Cardoso Paz*, F. Bergamaschi**, G. Ghibaudo***, F. Serra***, G. Billiot, A. G. M. Jansen^, Q. Berlingard***, S. Martinie, T. Bedecarrats, L. Contamin, A. Juge^^, E. Vincent6, P. Galy^^, M.A Pavanello**, M. Vinet, T. Meunier* and F. Gaillard, CEA-Leti, *CNRS Institut Neel, **Centro Universitario FEI, ***CNRS IMEP-LAHC, ^CEA-IRIG, ^^STMicroelectronics

We present a status of FDSOI transistors electrical characterization for very low temperature operation. We highlight in particular singular transport and thermal effects occurring at low T. We also present the physical and analytical models associated with various characteristic electrical parameters, paving the way towards cryogenic compact models.

Session 35: PDS - Latest Records and Achievements in GaN Power Devices
Wednesday, December 7, 1:30 p.m.
Continental Ballroom 4
Olga Spahn, ARPA-E and Adrei Vescan, RWTH Aachen University

1:35 p.m.
35.1 Scaled Submicron Field-Plated Enhancement Mode High-K Gallium Nitride Transistors on 300mm Si(111) Wafer with Power FoM ($R_{ON}xQ_{GG}$) of 3.1 mohm-nC at 40V and f_T/f_{MAX} of 130/680GHz, H. W. Then, M.Radosavljevic, P.Koirala, M.Beumer, S.Bader, A.Zubair, T.Hoff,R.Jordan, T.Michaelos, J.Peck, I.Ban,N.Nair, H.Vora, K.Joshi, I.Meric, A.Oni, N.Desai, H.Krishnamurthy, K.Ravichandran, J.Yu, S.Beach, D.Frolov, A.Hubert, A.Latorre-rey, S.Rami, J.Rangaswamy,Q.Yu, P.Fischer, Intel Corporation

We demonstrate high-voltage enhancement-mode high-k GaN-on-300mm-Si(111) NMOS transistor employing scaled submicron-length field-plate. We achieve power FoM($R_{ON}xQ_{GG}$)=3.1mohm-nC at 40V, ~20-30X better than p-GaN HEMT and Si-LDMOS; low drain-leakage=0.3pA/μm at 40V (V_G=0V). A power switch is fabricated with total width=1300mm, and R_{DSON}=1.9 mohm-mm^2. A 30nm-L_G, 100nm-source-field-plated GaN NMOS transistor demonstrates record f_{MAX}=680GHz.

2:00 p.m.
35.2 1200V GaN Switches on Sapphire: A low-cost, high-performance platform for EV and industrial applications (Invited), G. Gupta, M. Kanamura*, B. Swenson, C. Neufeld, T. Hosoda*, P. Parikh, R. Lal, U. Mishra, Transphorm, Inc., *Transphorm Japan

We demonstrate 1200V GaN HEMT switches on sapphire substrate with fast-switching and low-loss. Insulating sapphire substrate is used to extend rated voltage of GaN HEMTs to 1200V with much thinner buffer vs GaN-on-Si. The 1200V/70mΩ GaN-on-sapphire switches show excellent efficiency of >99% in hard-switched 900:450V buck converter at 50kHz.

2:25 p.m.
35.3 Highly-Scaled Self-Aligned GaN Complementary Technology on GaN-on-Si Platform, Qingyun Xie, Mengyang Yuan, John Niroula, James Greer, Nitul Rajput*, Nadim Chowdhury**, Tomas Palacios,

Massachusetts Institute of Technology, *Technology Innovation Institute, **Bangladesh University of Engineering and Technology

This paper reports on the scaling of self-aligned(SA) GaN complementary technology on a GaN-on-Si platform. The highly scaled SA p-FinFET achieved I_{ON}=−300 mA/mm, R_{ON}=27 Ω·mm, a record for MOCVD III-N p-FETs. The newly proposed SA scaled p-GaN-gate process yields Enhancement-mode n-FETs (I_{ON}=525 mA/mm, R_{ON}=2.9 Ω·mm) on the same platform.

3:15 p.m.
35.4 Hybrid Gate p-GaN Power HEMTs Technology for Enhanced V_{th} Stability, Chi Zhang, Sheng Li, Siyang Liu, Weihao Lu, Yanfeng Ma, Jiaxing Wei, Long Zhang, Weifeng Sun, Denggui Wang*, Jianjun Zhou*, Song Bai*, Southeast University, *Nanjing Electronic Devices Institute

A novel Hybrid gate p-GaN power HEMT technology is proposed to enhance V_{th} stability without I_{gss} degradation. Charge storage effect can be alleviated through a free-carrier "discharge path" induced by ohmic-type region. It is experimentally demonstrated that Hyb-HEMT can achieve higher gate reliability than commercial products.

3:40 p.m.
35.5 Superior Breakdown, Retention, and TDDB Lifetime for Ferroelectric Engineered Charge Trap Gate E-mode GaN MIS-HEMT, J.-S. Wu, P.-H. Liao, S.-J. Chang, T.-Y. Yang, C.-Y. Teng, Y.-K. Liang, D. Panda, Q. H. Luc, and E. Y. Chang, National Yang Ming Chiao Tung University

A high-performance La-doped ferroelectric engineered charge trap gate E-mode MIS-HEMT (FEG-HEMT) proved excellent V_{th} stability of 2.9 V after 10 years of retention, high gate breakdown of V_{GS} = 26.6 V, and long time-dependent gate dielectric breakdown (TDDB) (13.38 V at a failure rate of 0.01%).

4:05 p.m.
35.6 First Demonstration of Vertical Superjunction Diode in GaN, Ming Xiao, Yunwei Ma, Zhonghao Du*, Yuan Qin, Kai Liu**, Kai Cheng**, Florin Udrea***, Andy Xie^, Edward Beam^, Boyan Wang, Joseph Spencer^^, Marko Tadjer^^, Travis Anderson^^, Han Wang*, Yuhao Zhang, Virginia Polytechnic Institute and State University, *University of Southern California, **Enkris Semiconductor, Inc., ***University of Cambridge, ^Qorvo, Inc., ^^U.S. Naval Research Laboratory

We report the first experimental demonstration of a functional vertical superjunction device in GaN. Vertical GaN superjunction p-n diodes are demonstrated on both GaN and sapphire substrates with a drift region resistance of 0.15 mΩ·cm^2 and breakdown voltage over 1100 V, the trade-off of which exceeds the 1-D GaN limit.

4:30 p.m.
35.7 Current Status and Future Prospects of GaN-on-GaN Vertical Power Devices (Invited), J. Suda, Nagoya University

Current status and future prospects of GaN vertical power devices fabricated on GaN substrates are presented. Fundamental material properties of GaN related to vertical power devices, progress of GaN bulk substrate developments and device fabrication processes as epitaxial growth, ion implantation and MOS interface are reviewed.

Session 36: EDT - Magnetic and Ferroelectric Technologies
Wednesday, December 7, 1:30 p.m.
Continental 5

Jean Anne Incorvia, University of Texas at Austin and Uwe Schroeder, NAMLAB

1:35 p.m.
36.1 Scalable Ising Computer Based on Ultra-Fast Field-Free Spin Orbit Torque Stochastic Device with Extreme 1-Bit Quantization, Jialiang Yin, Yu Liu, Bolin Zhang, Ao Du, Tianqi Gao, Xiangyue Ma, Yi Dong, Yue Bai, Shiyang Lu, Yudong Zhuo, Yan Huang, Wenlong Cai, Daoqian Zhu, Kewen Shi, Kaihua Cao, Deming Zhang, Lang Zeng, Weisheng Zhao, Beihang University

In this work, an ultra-fast field-free P-Bit tunable by Spin Orbit Torque (SOT) Effect is proposed and carefully verified by throughout experimental measurement. Further, for the first time, an extreme 1-Bit quantization method against device variation is proposed for the hardware implementation of Ising computer with large P-Bit array.

2:00 p.m.
36.2 First demonstration of field-free perpendicular SOT-MRAM for ultrafast and high-density embedded memories, K. Cai, G. Talmelli, K. Fan, S. Van Beek, V. Kateel, M. Gupta, M.G. Monteiro, M. Ben Chroud, G. Jayakumar, A. Trovato, S. Rao, G.S. Kar, S. Couet, imec

For the first time, we experimentally demonstrate the field-free switching in multi-pillar (MP) spin-orbit torque magnetic random-access memory (SOT-MRAM) devices, which are CMOS-compatible 300mm integrated perpendicular MTJs (p-MTJs). This FFS scheme is fully compatible with the standard integration process and the voltage-gated SOT (VG-SOT) switching in MP devices.

2:25 p.m.
36.3 Magnetic skyrmions for unconventional embedded computing applications (Invited), F. Büttner, Helmholtz-Zentrum Berlin

Magnetic skyrmions are nanometer-scale textures which can encode, carry, process, and store information with little or no energy. Possible applications include low-energy, embedded applications. This paper reviews technologically relevant properties of skyrmions and presents our recent advances in harnessing these properties in a deterministic, fast (sub-nanosecond), and device-compatible fashion.

3:15 p.m.
36.4 Low-voltage and high-speed switching of a magnetoelectric element for energy efficient compute, Punyashloka Debashis, John Plombon, Chia-Ching Lin, Yu-Ching Liao, Hai Li, Dmitri Nikonov, Dominique Adams, Carly Rogan, Mahendra DC, Marko Radosavljevic, Scott Clendenning, Ian Young, Intel Corporation

150 mV voltage-driven switching of a ferromagnet exchange-coupled to 6-nm-thick lanthanum-doped $BiFeO_3$ and less than 2 ns switching of this material's polarization was experimentally demonstrated at room temperature. Circuit simulations utilizing experimentally calibrated compact models show the energy-delay benefits of the magnetoelectric random access memory using this material.

3:40 p.m.
36.5 Novel Ferroelectric Tunnel FinFET based Encryption-embedded Computing-in-Memory for Secure AI with High Area- and Energy-Efficiency, Jin Luo, Hanyong Shao, Boyi Fu, Zhiyuan Fu, Weikai Xu, Kaifeng Wang, Mengxuan Yang, Yiqing Li, Xiao Lv, Qianqian Huang, Ru Huang, Peking University

This work reports the first experimental demonstration of FeTFET-based area- and energy-efficient encryption-embedded nvCIM, in which the encrypted-MAC with multilevel weight is implemented by

XNOR-operation in weight-cell based on FeTFET with one transistor. Based on the proposed design, security-enhanced inference and learning are demonstrated, showing great potentional for secure AI.

4:05 p.m.
36.6 Superlattice HfO_2-ZrO_2 based Ferro-Stack $HfZrO_2$ FeFETs: Homogeneous-Domain Merits Ultra-Low Error, Low Programming Voltage 4 V and Robust Endurance 10^9 cycles for Multibit NVM, C.-Y. Liao, Z.-F. Lou, C.-Y. Lin, A. Senapati*, R. Karmakar*, K.-Y. Hsiang,**, Z.-X. Li, W.-C. Ray, J.-Y. Lee,***, P.-H. Chen, F.-S. Chang, H.-H. Tseng, C.-C. Wang, J.-H. Tsai, Y.-T. Tang^, S. T. Chang^^, C. W. Liu***, S. Maikap*,*, and M. H. Lee, NTNU, *CGU, **NYCU, ***NTU, ^NCU, ^^NCHU

Superlattice (SL) HfO_2-ZrO_2 with 5nm reveals high orthorhombic-phase ~80% and low monoclinic-phase 7.9% by GPA. The homogeneous and coherent of SL-HZO with sufficient ferroelectric-domain demonstrates improvement on D2D variation for nanoscale 3D-FET, and ferro-stack FeFETs for low $|V_{PG/ER}|$=4V, ultra-low ER=7.5×10^{-16}, record high 2-bit endurance 10^9 cycles, and stable data retention>10^4s.

4:30 p.m.
36.7 Compact Ferroelectric Programmable Majority Gate for Compute-in-Memory Applications, Shan Deng, Mahdi Benkhelifa*, Simon Thomann*, Zubair Faris, Zijian Zhao, Tzu-Jung Huang, Yixin Xu**, Vijaykrishnan Narayanan**, Kai Ni, Hussam Amrouch*, Rochester Institute of Technology, *University of Stuttgart, **Pennsylvania State University

Compact and novel ferroelectric programmable majority gate is proposed and its novel application in Binary Neural Network is investigated. By integrating N metal-ferroelectric-metal (MFM) capacitors on the gate of a transistor, a nonvolatile and programmable majority gate that performs MAJ of AND between the gate input and polarization is realized.

Session 37: ODI - Silicon Image Sensors and Photonics
Wednesday, December 7, 1:30 p.m.
Continental Ballroom 6
Keiji Mabuchi, Omnivision Technologies and In-Sung Joe, Samsung Electronics

1:35 p.m.
37.1 Coherent Silicon Photonics for Imaging and Ranging (Invited), Ali Hajimiri, Aroutin Khachturian, Parham Khial, Reza Fatemi, California Institute of Technology

Silicon photonics platform and their potential for integration with CMOS electronics present novel opportunities in applications such as imaging, ranging, sensing, and displays. Here, we present ranging and imaging results for a coherent silicon-imaging system that uses a two-path quadrature (IQ) approach to overcome optical path length mismatches.

2:00 p.m.
37.2 Near-Infrared Sensitivity Enhancement of Image Sensor by 2^{ND}-Order Plasmonic Diffraction and the Concept of Resonant-Chamber-Like Pixel, Nobukazu Teranishi, Takahito Yoshinaga, Kazuma Hashimoto, Atsushi Ono, Shizuoka University

We propose 2^{nd}-order plasmonic diffraction and the concept of a resonant-chamber-like pixel to enhance the near-infrared (NIR) sensitivity of Si image sensors. Optical requirements for deep trench isolation are explained. In the simulation, Si absorptance as high as 49% at 940 nm wavelength for 3.25-µm-thick Si is obtained.

2:25 p.m.
37.3 A SPAD Depth Sensor Robust Against Ambient Light: The Importance of Pixel Scaling and Demonstration of a 2.5µm Pixel with 21.8% PDE at 940nm, S. Shimada, Y. Otake, S. Yoshida, Y. Jibiki, M. Fujii, S. Endo, R. Nakamura, H. Tsugawa, Y. Fujisaki, K. Yokochi, J. Iwase, K. Takabayashi*, H. Maeda*, K. Sugihara*, K. Yamamoto*, M. Ono*, K. Ishibashi*, S. Matsumoto, H. Hiyama, and T. Wakano, Sony Semiconductor Solutions, *Sony Semiconductor Manufacturing

This paper presents scaled-down SPAD pixels to prevent PDE degradation under high ambient light. This study is carried out on Back-Illuminated structures with 3.3, 3.0, and 2.5µm pixel pitches. Our new SPAD pixels can achieve PDE at λ=940nm of over 20% and a peak of over 75%, even 2.5µm pixel.

3:15 p.m.
37.4 3-Tier BSI CIS with 3D Sequential & Hybrid Bonding Enabling a 1.4um pitch,106dB HDR Flicker Free Pixel, F. Guyader, P. Batude*, P. Malinge, E.Vire, J. Lacord*, J. Jourdon, J. Poulet, L. Gay, F. Ponthenier*, S. Joblot, A. Farcy, L. Brunet*, A. Albouy*, C. Theodorou**, M. Ribotta*, D. Bosch*, E. Ollier*, D.Muller, M.Neyens, D. Jeanjean, T.Ferrotti, E.Mortini, J.G. Mattei, A. Inard, R. Fillon, F. Lalanne, F. Roy, E. Josse, STMicroelectronics, *CEA-Leti, Univ. Grenoble Alpes, **Univ. Grenoble Alpes, Univ. Savoie Mont Blanc, CNRS, Grenoble INP, IMEP-LAHC

A 3-tier CIS combining 3D Sequential Integration for the 2-tier pixel realization & Hybrid Bonding for the logic circuitry connection is demonstrated. Thin film pixel transistors are built above photo-gate without congestion. Dual carrier collection 3DSI pixel offers an attractive dynamic range (106dB, Single Exposure) versus pixel pitch (1,4µm) trade-off

3:40 p.m.
37.5 3-Layer Stacked Voltage-Domain Global Shutter CMOS Image Sensor with 1.8µm-Pixel-Pitch, Seung-Sik Kim, Gwi-Deok Ryan Lee, Sang-Su Park, Heesung Shim, Dae-Hoon Kim, Minjun Choi, Sangyoon Kim, Gyunha Park, Seung-Jae Oh, Joosung Moon, Sungbong Park, Sol Yoon, Jihye Jeong, Sejin Park, Sanggwon Lee, HaeJung Lee, Wonoh Ryu, Taehyoung Kim, Doowon Kwon, Hyuk Soon Choi, Hongki Kim, Jonghyun Go, JinGyun Kim, Seunghyun Lim, HoonJoo Na, Jae-kyu Lee, Chang-Rok Moon, Jaihyuk Song, Samsung Electronics

We developed a 1.8µm-pixel GS sensor which is suitable for mobile applications. Pixel shrink was possible by the 3-layer stacking structure with pixel-level Cu-to-Cu bonding and high-capacity DRAM capacitors . As a result, excellent performances were achieved i.e. -130dB, 1.8e-rms and 14ke- of PLS, TN and FWC, respectively.

4:05 p.m.
37.6 Advanced Color Filter Isolation Technolgy for Sub-Micron Pixel of CMOS Image Sensor, Hojin Bak, Horyeong Lee, Won-Jin Kim, Inho Choi, Hanjun Kim, Dongha Kim, Hanseung Lee, Sukman Han, Kyoung-In Lee, Youngwoong Do, Minsu Cho, Moung-Seok Baek, Kyungdo Kim, Wonje Park, Seong-Hun Kang, Sung-Joo Hong, Hoon-Sang Oh, and Changrock Song SK hynix Inc.

The novel color filter isolation technology, which adopts the air, the lowest refractive index material on the earth, as a major component of an optical grid for sub-micron pixels of CMOS image sensors, is presented. The image quality improvement was verified through the enhanced optical performance of the air-grid-assisted pixels.

4:30 p.m.
37.7 A 140 dB Single-Exposure Dynamic-Range CMOS Image Sensor with In-Pixel DRAM Capacitor, Youngsun Oh, Jungwook Lim, Soeun Park, Dongsuk Yoo, Moosup Lim, Joonseok Park, Seojoo

Kim, Minwook Jung, Sungkwan Kim, Junetaeg Lee, In-Gyu Baek, Kwangyul Ryu, Kyungmin Kim, Youngtae Jang, Min-SunKeel, Gyujin Bae, Seunghun Yoo, Youngkyun Jeong, Bumsuk Kim, Jungchak Ahn, Haechang Lee, Joonseo Yim, Samsung Electronics Co., Ltd.

A CMOS image sensor with a 2.1 μm pixel for automotive applications was developed. With a sub-pixel structure and a high-capacity DRAM capacitor, a single exposure dynamic range achieves 140 dB at 85°C, supporting LED flicker mitigation and blooming free. SNR stay above 23 dB at 105°C.

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