Tutorial 3: Reliability Challenges of Emerging FET Devices

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Abstract:

The unabated performance enhancement of semiconductor technology has been sustained in recent years by disruptive device and material innovations. For the successful deployment of any novel device concept, the promised enhanced performance must be guaranteed for the entire expected lifetime of the final product. Traditionally, device reliability optimization was an aspect considered only at a late stage in the development of a new device technology. We argue that in contemporary devices, fabricated with complex integrations and a plethora of materials, potential reliability issues should be considered from the very early stage of the technology development, as they can potentially disqualify otherwise promising device concepts. In particular, charge trapping in gate dielectrics is an aspect that can “make or break” any MOS-based device, and thus gate stack stability should be considered as a primary metric in the evaluation of novel device concepts.

In this Tutorial we will review the fundamentals of charge trapping in gate dielectrics in terms of phenomenology, characterization techniques and physical models. Next, we will briefly discuss as case studies some recent examples of MOS innovations which made it into mainstream technology (e.g., SiGe channels), as well as other examples which to date remain confined to academic research (e.g., III-V and Ge channels for Logic). We will then focus on specific gate stack challenges for upcoming CMOS technology innovations, including Nanosheet and Forksheet device architectures, and novel device concepts such as the stacked Complementary FET (CFET) and 2D channel transistors. To further highlight the general relevance of charge trapping in dielectrics, we will briefly discuss its role also in wide-bandgap semiconductors (GaN, SiC) MOS-based devices for Power and Analog/RF applications. Finally, we will discuss novel transistors based on oxide semiconductor channels (e.g., IGZO), which due to their extremely low off-state leakage and their flexible fabrication flow are considered as potential gamechangers for memory periphery and, in general, for the heterogeneous integration of transistors in the Back End of Line (BEOL). For these devices, we will discuss how the interplay between their gate dielectric and channel instabilities makes the reliability assessment and optimization particularly complex and requiring the combination of electrical and optical characterization techniques.

Bio:

Dr. Jacopo Franco is a Principal Member of Technical Staff in the Reliability group of the Advanced Reliability, Robustness and Test department of imec, Belgium. He received the B.Sc. (2005) and M.Sc. (2008) from the University of Calabria - Italy, and the Ph.D. degree from KU Leuven - Belgium (2013) in Electrical Engineering. His research focuses on CMOS FEOL reliability characterization, optimization, and modelling, and in particular: i) on gate stack development for novel device technologies (SiGe, Ge, III-V, IGZO), architectures (finFETs, FD-SOI, Nanowires, Nanosheets), and integration schemes (Sequential 3D tier stacking, CFETs); ii) on characterization and physics-based modeling of FEOL degradation mechanisms (BTI, Hot Carrier, Off-state degradation, TDDB, RTN, time-dependent variability); iii) on reliability compact models to accurately propagate individual device aging to circuit level. He has (co)authored 250+ contributed or invited papers and 3 patents, and he is a recipient of several IEEE awards: Best Student Paper at SISC (2009), EDS Ph.D. Student Fellowship (2012), Paul Rappaport Award (2011), Best (2012, 2022), Outstanding (2014), and Best Student (2016) paper awards at IRPS. He has been serving in various functions on the Technical Program Committees of IRPS, SISC, IIRW, ESREF, WoDiM and INFOS conferences, and as an Associate Editor of IEEE Transactions on Device and Materials Reliability (2017-2020) and of IEEE Transactions on Electron Devices (2020-2022).