Advanced Technology Requirement for Edge Computing

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Jie Deng received his B.S. degree in Electronics from Beijing University and Ph.D. degree in Electrical Engineering from Stanford University, specializing in advanced devices, such as Carbon Nanotube Transistor (CNFET), research, modeling and circuit design optimization. In 2007, he joined IBM Semiconductor Research and Development Center (SRDC) at Wappingers Falls, NY as an advisory engineer where he worked on device research and development for low-power and high-performance logic technology from 65nm node to 14nm node. Since 2013, he has been with Qualcomm Process Technology & Foundry Engineering Team, working on advanced nodes High-Volume-Manufacturing (HVM) products bring-up and foundry engagement, spanning from 14nm node to 3nm node. His current role also includes the evaluation of tech nodes power-performance-area-cost (PPAC) and roadmap planning for tech node selection and technology features to meet different product KPI requirements. Jie Deng has authored and coauthored over 40 papers in accredited journals and international conferences in semiconductor technology.

Abstract: The next-generation computing market is poised to experience an astounding six-fold surge from 2023 to 2033, driven by a remarkable compound annual growth rate (CAGR) exceeding 19% in the next decade. The escalating computing demand intensifies the necessity for optimal low-power and high-performance solutions. Achieving continuous power-performance scaling demands seamless synergy between transistors, interconnects, and packaging technologies. With FinFET scaling approaching its limits, innovative device architectures emerge as promising candidates for next-generation transistor technology, including gate-all-around (GAA/NS), Forksheet FET (FS), complementary FET (CFET), 2D-material FET. To address large wire delay and the high IR drop issue resulting from continuous area scaling, novel interconnect material and innovative integration schemes like Backside Power Delivery (BSP) are required. Furthermore, the semiconductor industry is moving towards advanced heterogeneous packaging platforms for both 2.5D and 3D integration. In this short course, we will explore the current state of transistor, interconnect, and packaging technologies, review challenges in continuous power-performance scaling, and delve into emerging technologies for next-generation low-power, high-performance computing. Additionally, we will discuss economic impact and production interception timeline outlook of various emerging technologies for different applications.