Process Technology toward 1nm and Beyond

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Abstract: This short course will cover the processes technologies that enable the continuous evolution of logic transistors and interconnects towards the 1nm node and beyond. The critical metric for logic density is the product of the "logic cell width x logic cell height". Gate pitch scaling is a crucial factor for scaling logic cell width. To enable this, scaling of gate length, gate spacer width, and contact feature size is necessary. Gate-All-Around (GAA) technology improves electrostatics compared to FinFETs and enables continuous gate length scaling. Material advancements are necessary to mitigate parasitic capacitance and resistance increase while securing yield and reliability of the transistors. In terms of the logic cell height, advancements in layout and transistor structure innovations, as well as interconnect metal pitch scaling, contribute to its scaling. Continuous RC reduction techniques have been implemented for copper interconnect extension with metal pitch scaling. Eventually, alternative metals that outperform copper in CD sizes of 10nm and below need to be considered. Regarding layout and transistor structure innovations, a backside Power Delivery Network (PDN) is an attractive option for better area utilization and performance enhancement. Additionally, Complementary FET (CFET), which consists of stacked transistors, is a promising architecture for enabling continuous logic cell height scaling. To enable these advancements, continuous process and tool advancements are necessary not only in film, etch, lithography, and wet processing but also in wafer bonding and