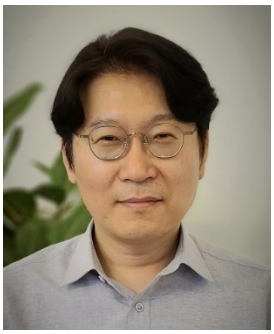
thinning technologies. The talk will also review recent progress in EUV-related solutions, including self-aligned patterning.

Empowering Platform Technology with Future Semiconductor Device Innovation

Jaehun Jeong, Samsung Electronics



Jaehun Jeong is a Project Leader and Technology Manager on the logic device solutions in Technology Development Group of Samsung Foundry. His role is in the management on the performance of not only leading-edge transistor like Samsung's Multi-Bridge-Channel FET (MBCFETTM) and FinFET itself, also chip-level process optimization for mass-production. His team has responsibility about maintaining electrical characteristics including transistor performance, variation, PDK model target generation and chip performance improvement in several fields of Foundry products such as SoC, GPU, ASIC and HPC. Since he joined Samsung Foundry in 2009, he led advanced technology development in many nodes, including 28nm/20nm planar technologies, FinFET technologies from 10nm to 4nm, and 3nm MBCFETTM. He has many experiences in SRAM cell development in foundry products. And he also researched 3-dimensional memory structure like stacked SRAM/Flash-memory and VNAND in the Memory division of Samsung electronics before he entered the Foundry business. Jaehun Jeong received his B.S/M.S degrees in electrical engineering from Seoul National University in South Korea.

Abstract: FinFET, the platform technology in foundry business for more than a decade, has faced fundamental limitations for the further scaling with PPA improvement and it is the time to move on another "New dimension" of transistor. Gate-All-Around (GAA) FETs / MBCFETTM have been already introduced as the logic device for next generation and started mass production. MBCFETTM has been enabling different type of PPA enhancement with the design flexibility allowing additional room for DTCO to optimize standard cell speed/power with various nano-sheet size beyond its intrinsic device gain like short channel effect improvement and high drivability. In near future, 3D stacked structure connecting multiple layers of transistors vertically and Backside-PDN technology relocating the power delivery network to the backside of the chip will be ready for innovative integration schemes. Also, 2D transistor has been studied to use their high carrier mobility and excellent electrostatic control enabling another scaling of gate length and pitch. These innovations in the semiconductor industry can bring another breakthrough to enhance the capabilities of foundry platform technologies, and the key to sustainable success lies in how to harness the power of those technological advancement to the platform technology including emerging applications such as mobile SoC, AI, autonomous vehicle and HPC with enhancement of overall chip performance.