Future Power Delivery Process Architectures and Their Capability and Impact on Interconnect Scaling

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Abstract: As continued semiconductor technology scaling becomes increasingly more challenging and expensive it is crucial to invent ways to enable increasing the ability to interconnect the transistors and slow the degradation of the interconnect properties. Traditionally, degree of connectivity is maintained thru scaling interconnect pitches and feed thru pitches and adding ever more interconnect layers. The cost of this approach is becoming increasingly more impactful we must find new ways to add design value and scaling capability outside of the conventional approach. Novel technologies such as buried power rails can reduce the impact of these effects to a limited extent. One step beyond this lies in the introduction of backside power. Moving power to the backside of the wafer greatly reduces the interconnect tax on the conventional front side interconnects by removing the need spend interconnect resources on power. Beyond backside power advantage lies in leveraging the ability to contact the transistor from top and bottom and introducing dense metal on both frontside and backside. In this short course we will look at the scaling pressures on interconnects driving the need for these new technologies as well as the technologies themselves along with the engineering opportunities and challenges for high volume manufacturing.