

DTCO/STCO in the Era of Vertical Integration

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YK Chong is a Fellow and Lead Memory Architect at Arm. At Arm's Solution Engineering Physical IP Group, YK leads the Memory Roadmap in collaboration with Arm's Central Engineering teams to define the next-generation memory requirements and features for CPU, GPU, and System that improve the SoC level PPA and IPC. His team designs the best-in-class memories that are optimized for Infrastructure, Client, Automotive, and IoT applications. YK is also responsible for the Design Technology Co-Optimization (DTCO) with multiple foundries to

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Abstract: As we venture into the era of AI, the demand for energy-efficient computation continues to accelerate. However, the relentless push towards smaller semiconductor geometries has brought about significant challenges to technology scaling. To sustain progress, the semiconductor industry must explore alternative approaches. Coordinated innovations across system, circuit, and technology abstraction levels are needed to continue the trajectory of power, performance, area, and cost (PPAC) metrics within compressed product development timelines. In this short course, we offer an industry perspective on the technological and product development challenges of advanced process nodes. We will delve into Design-Technology Co-Optimization (DTCO) and System-Technology Co-Optimization (STCO) strategies that have been explored at Arm, encompassing various techniques applied to logic, SRAM, interconnects, power delivery, system partitioning, and packaging. We hope that our practical insights will help device engineers, circuit designers, and system architects to continue to improve high-performance computing in the sub-3 nm era.