Low Power SOC Design trends/3D Integration/Packaging for Mobile Applications

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Milind Shah is Head of IC Packaging @ Google working on consumer devices IC packaging. He is currently working on mobile SOC, SiP integration for Google consumer products. His group is responsible for early development through HVM deployment for products. Prior to joining Google, Milind spend 14yrs at Qualcomm working on System in Package (SiP) technologies to enable 5G, IoT, Automotive sub-systems modules and technologies such as fine pitch flip chip as well as new package structures such as PoP. Prior to Qualcomm, Milind spent nine years at RFMD developing packages for RF front end modules, conformal shielding, and embedded actives. Milind has an MSME degree from Florida International University and is an inventor on 30 plus issued patents.

Abstract: Moore's Law has been the driving force behind the scaling of process nodes for decades, enabling higher transistor density in monolithic system-on-chip (SoC) architecture designs. However, cost pressure and longer cycle times for manufacturing monolithic SoC designs in recent process generations have slowed down node scaling, forcing chip designers to explore new architectures to meet higher performance requirements more economically. Chiplet-based architectures with high-density interconnect packaging integration for homogeneous and/or heterogeneous nodes offer a new way to design chips that allow for more flexibility and scalability, as well as the creation of chiplets tailored to specific applications and easier upgrades. This short course will review the current industry landscape of 3D packaging integration solutions, which enable higher off-chip interconnect density, resulting in higher data bandwidth, power efficiency, lower data communication latency and future trends. The broader industry trend of 3D interconnect packaging strategy and optimization will also be highlighted in this study.