High-Density and High-Performance Technologies for Future Memory

Koji Sakui, Unisantis Electronics Singapore, Tokyo Institute of Technology

Koji Sakui is the Executive Technical Manager of Unisantis Electronics Singapore. He received his B.Eng. and M.E. degrees, both in Instrumentation Engineering, from Keio University in 1979 and 1981, respectively, and his Ph.D. degree from Tohoku University in 1995. In 1981, he joined Toshiba Research and Development Center, where he was engaged in the circuit design of DRAM's. Since 1990 he has been working on the development of high-density NAND Flash memories. He managed the Flash Memory Design Department of SoC R & D Center to develop 90 nm, 70nm, and 55 nm NAND Flash memory design. He moved to Sony Corporation in 2004, and served as the General Manager of Memory System Department. In 2007, he moved to NAND Products Group, Intel Corporation, as a Research Scientist. In 2009, he became a Visiting Professor of Tohoku University for the research on the SGT circuit application. In 2010, he joined Micron as Sr. Architect and Technologist–Memory Innovations. In 2017, he joined Honda Research Institute as Senior Scientist. Thereafter, since 2018, he has been a Researcher at Tokyo Institute of Technology for the research on the BBCube as part of the WoW Alliance. In 2020, he joined Unisantis Electronics Singapore as Executive Technical Manager for the research on the DFM, KFBM, and SGT.

Dr. Sakui is a member of the IEEE Electron Device Society, and served on the Technical Program Committee for NVSMW (currently IMW) from 1998 to 2012. He is an inventor on over 180 granted US patents, and published over 40 technical papers (h-index=43). In 2012, he became an IEEE Fellow, with the accompanying citation: "for the contribution to NAND flash memories."

Abstract: The agenda is composed of four key technologies; **1) DFM**, **2) KFBM**, **3) SGT**, and **4) BBCube**. 1**) DFM**: A new high-density memory technology called Dynamic Flash Memory (DFM) which can be built using a conventional silicon process. DFM is scalable and has no special material requirements, making it a cost-effective alternative to emerging memory technologies. The proposed stackable DFM eliminates the need for capacitors, resulting in smaller cell sizes than $6F^2$ with 3~4 tiers. **2) KFBM**: A fully CMOS compatible Key shape Floating Body Memory (KFBM) cell consists of MOSFET with virtually floating body formed by bulk silicon and trench with on/off margins of more than three orders of magnitude. The vertical device in KFBM helps to improve retention and disturbance and reduce the scaling pressure. **3) SGT**: A Surrounding Gate Transistor (SGT) has advantages of improved density and reduced power leakage, which means that the SGT is a promising candidate for a switching transistor of a variety of memory devices, such as DRAM. **4) BBCube**: The Bumpless Build Cube (BBCube) 3D has been proposed for AI and HPC applications, which need high bandwidth and power efficiency. The BBCube 3D is constructed by heterogeneous 3D integration in which xPU (CPU, GPU etc.) chips and DRAM wafers are stacked using a combination of bumpless Wafer-on-Wafer and Chip-on-Wafer. The BBCube 3D has the potential to achieve a bandwidth 30 times higher than DDR5 and four times higher than HBM2E with the access energy per bit 1/20th that of DDR5 and 1/5th that of HBM2E.