The Next Generation of AI Architectures: The Role of Advanced Packaging Technologies in Enabling Heterogeneous Chiplets

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Bio

Dr. Raja Swaminathan is CVP, Packaging instrumental in the development of AMD's industry leading advanced packaging roadmap. Raja has been a leader in silicon-package-system architecture definition and a co-design expert with extensive experience introducing new technologies and innovation across the silicon-packaging spectrum at Intel, Apple and AMD. He's helped enable PPAC (power, performance, area, and cost) improvements as well as introduction of novel heterogeneous architectures throughout his career: EMIB, Apple's Mx package architectures, 3D V-Cache, Elevated Fan-Out Bridge, High Performance Fanout to name a few. Raja received his PhD from Carnegie Mellon University and has over 40 US patents in the field. He is an IEEE Senior Member and is on the technical advisory board for multiple semiconductor startups.

Abstract

As we further race to bring together heterogenous compute and acceleration from the motherboard to the package, our industry will need to solve several new challenges. Chiplet architectures are fundamental to the continued economic viable growth of power efficiency of AI, 5G and edge computing. The slowing of Moore's law has also placed advanced packaging at the critical juncture of technology-architecture intersection driving unique product capabilities. UCIe is a great step forward to address the interconnect aspect, but how do we bring UCIe together with advanced packaging. What standard form factors should we define? How do we enable debug/test beyond KGD? What kind of power delivery and thermal controls will we need? Can we also enable DVFS and binning? How do these challenges differ between advanced and organic packaging solutions? In this course, we will take a look at these questions and discuss some possible ways forward to address these challenges. New heterogeneous architectures like 2.5D Fanout and 3D Hybrid bonded architectures driving AMD's industry leading advanced technology roadmap to enable power, performance, area, and cost (PPAC) as well as challenges and solutions for large chiplet modules etc. will also be discussed.