Charge-Trapping Memories: From the Fundamental Device Physics to 3D Memory Architectures (3D NAND, 3D NOR, 3D DRAM) and Computing in Memory (CIM)

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Bio: Hang-Ting (Oliver) Lue currently serves as the Director of the Emerging Memory Technology R&D Division at Macronix. His research primarily focuses on a wide array of topics related to charge-trapping memories, such as Bandgap engineered-SONOS and its variants, as well as their applications in memory products. With a track record spanning over twenty years, he has authored more than 150 IEEE papers and holds over 150 granted patents in the United States. Notably, he has contributed to over 50 papers presented at IEDM and VLSI conferences. His research pursuits extend to encompass 3D NAND, 3D NOR, and 3D DRAM architectures, alongside the exploration of computing in memory (CIM) through the utilization of 3D memory devices. In recognition of his achievements, he was elected as an IEEE Fellow in the Electron Devices Society (EDS) in 2021. Throughout the years, he has actively participated in various IEEE semiconductor device conferences, including IEDM, VLSI, IMW, SSDM, and VLSI-TSA. He has been a member of the VLSI Symposia technical committee since 2011.

Abstract: Charge-trapping Flash memory devices, including SONOS and its variations, have surpassed floating gate (FG) devices in the commercial market share recently, primarily due to the remarkable success of 3D NAND technology. This concise course will commence with a review of the fundamental physical principles behind bandgap engineered (BE) SONOS, encompassing AB initio modeling of commercially adopted SiON tunnel dielectrics and SiN traps. Detailed scrutiny will extend to 3D NAND architectures, encompassing both standard commercial cells and emerging double-density structures such as hemi-cylindrical or flat cells. Additionally, the potential of 3D NOR structures to offer a superior product performances with low-latency and byte-addressable 3D memory will be explored. Introducing a notable innovation, a micro heater capable of localized heating above 400°C will be presented. This innovation has potential to enhance the P/E cycling endurance of 3D charge-trapping Flash memory to over 100 million cycles, with remarkable high-temperature data retention. Finally, addressing the escalating demands of big-data AI computing, the course will delve into 3D DRAM architectures and the concept of computing in memory (CIM) utilizing 3D memory technology.