You are INVITED!

- In-person discussions on the hottest reliability topics
- Cultivate networking and collaboration

All of these (except Workshops and Posters) will be available via real-time streaming in the US Central time zone with virtual attendees having Q&A access opportunities. For those virtual attendees who cannot watch the live presentations, the material will be available on demand to all attendees after the symposium with the ability to communicate with the authors.
Join us at IRPS 2024 from April 14-18, 2024, in Dallas, TX!

On behalf of the management committee and board of directors, it gives me great pleasure to extend a warm welcome to all attendees, with sincere gratitude to our patrons and exhibitors. You can attend the symposium both IN-PERSON and VIRTUALLY. IRPS 2024 will offer a two-day tutorial, and a three-day technical program containing a poster and workshop session. Be sure to visit the IRPS homepage and complete your registration. We certainly look forward to your participation!

IRPS 2024 General Chair, Koji Eriguchi (Kyoto Univ.)
Overview

For 62 years, IRPS has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and all other parts of the world, IRPS seeks to understand the reliability of semiconductor devices, integrated circuits, and microelectronic systems through an improved understanding of both the physics of failure as well as the application environment. IRPS provides numerous opportunities for attendees to increase their knowledge and understanding of all aspects of microelectronics reliability. It is also an outstanding chance to meet and network with reliability colleagues from around the world. The IRPS2024 and the International ESD Workshop (IEW) will be co-hosted with IEW registrants participating in both IRPS and IEW programs.

For 2024, we are face to face but have adopted a hybrid format allowing virtual access to live oral presentations. The Technical Program consists of 4 keynote speakers, 17 invited speakers, 85 oral presentations organized in 29 technical sessions on 18 reliability topics, 10 Workshops, 74 Posters, 21 tutorials and 3 Year in Reviews, which serves as a summary of research in the past year. All of these (except Workshops and Posters) will be available via real-time streaming in the US Central time zone with virtual attendees having Q&A access opportunities. For those virtual attendees who cannot watch the live presentations, the material will be available on demand to all attendees after the symposium with the ability to communicate with the authors.
14th - 18th Apr. 2024, Dallas, TX
Registration now!:
https://www.irps.org/registration

**Keynote Speakers**

**“Hafnium-Oxide-Based Ferroelectric Devices for Low-Power Memory and AI Applications: Promises and Reliability Challenges”**

![Su Jin Ahn](image1.jpg)

Su Jin Ahn, EVP, Advanced Technology Development Office at Samsung Semiconductor R&D Center, Samsung

**“Innovative Technologies for Sustainable Future of Semiconductor Industry”**

![Shinichi Takagi](image2.jpg)

Shinichi Takagi, Professor, The University of Tokyo, Japan

**“Utility-scale Quantum Computing - Advances and Future Challenges”**

![Rajeev Malik](image3.jpg)

Rajeev Malik, Program Director, Systems Development & Deployment at IBM Quantum

**“Analog Technology Scaling and Reliability Implications”**

![Sameer Pendharkar](image4.jpg)

Sameer Pendharkar, VP of Advanced Technology Development, Texas Instruments

**Detail of keynote talk:**
https://www.irps.org/keynote-speakers

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The IRPS Reliability Year-in-Review (YiR) session consists of three presentations reviewing the past year's reliability work by experts in the field for areas of high interest. It is an excellent augmentation to the tutorial sessions immediately preceding, and attendees may obtain keen reliability insights in a short amount of time.

"From the Mathematical Foundations to the Physical Models: A Year in Review of Neuromorphic Reliability"

Brian Hoskins, Physicist in NIST

"Dielectric Breakdown: Advances in Characterization Techniques and Extrapolation to Use Conditions for Low and High-Voltage FETs"

Bonnie Weir, Master Engineer at Broadcom Inc.

"The exciting era of compact electronics with Gallium Nitride technology"

Stanford University

Srabanti Chowdhury, Associate Professor of Electrical Engineering, Senior Fellow at the Precourt Institute for Energy

Detail of Year-in-Review: https://www.irps.org/year-in-review

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Don’t miss the Exhibition of IRPS 2024.

- **Date and time:** Apr. 16th–18th
- **Location:** the front of the conference room (International I-IV)
- **Why Visit Exhibition:**
  - **Discovering:** Cutting-edge products and solutions.
  - **Expert Guidance:** Engage with our expert team
  - **Networking:** Connect with global professionals

**Detail of Exhibition:** https://www.irps.org/exhibitors

**Become a patron!**
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Workshop

Don’t miss the Workshop

- **Date:** Apr. 16th (Tue)
- **Time:**
  - 6:00 PM-7:30 PM: Reception
  - 7:30 PM-8:30 PM: 1st Session
  - 8:45 PM-9:45 PM: 2nd Session
- **Why Visit Exhibition:**
  - Discovering: In-person discussion on the hottest reliability topics.
  - Networking: Connect with global professionals

### Workshop Schedule

<table>
<thead>
<tr>
<th>Time</th>
<th>Session 1</th>
<th>Session 2</th>
<th>Session 3</th>
<th>Session 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:30-8:30</td>
<td>Circuit Aging Simulation Challenges &amp; Solution</td>
<td>Reliability Aware EDA (BEOL/Heating)</td>
<td>PID-Well Charging in product design</td>
<td>Increasing urgency of GaN reliability physics development</td>
</tr>
<tr>
<td>8:45-9:45</td>
<td>Technology scaling challenges: Power vs Reliability</td>
<td>HCI and self-heating advance devices Nanosheets</td>
<td>Challenges in RF/mmW/5G</td>
<td>ESD EDA: What Can be Done Now and in the Future?</td>
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</table>

**Detail of Workshop:** [https://www.irps.org/workshops](https://www.irps.org/workshops)

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### Session  
**Circuit Reliability and Aging**  
H. Amrouch (Technische Universität München)  
**Title**  
Machine Learning Unleashes Aging and Self-Heating Effects: From Transistors to Full Processor  
**Emerging Memory**  
U. Schroeder (Namlab)  
**Title**  
Ferroelectric HfO2-based Capacitors for FeRAM: Reliability from Single Devices to Memory Arrays  
**Failure Analysis**  
A. Griffin (TI)  
**Title**  
TBD  
**GaN Devices**  
S. Bahl (Texas Instrument)  
**Title**  
Status of JEDEC JC-70 Standards for GaN Power Devices Characterization and Reliability  
**Gate/MOL Dielectrics**  
M. Kobayashi (Univ. of Tokyo)  
**Title**  
Performance and reliability of nanosheet oxide semiconductor FETs with ALD-grown InGaO for 3D integration  
**Gate/MOL Dielectrics**  
H. Zhou (IBM)  
**Title**  
TDBD on gate-all-around nanosheets  
**Memory Reliability**  
R. Frickey (Solidigm)  
**Title**  
Comparing the Reliability of Solid State Drives based on TLC and QLC NAND Flash Memories  
**Metallization/BEOL Reliability**  
M. Herklotz (Globalfoundries)  
**Title**  
EDA method to address interconnect reliability and reduce overdesign in custom analog designs  
**Neuromorphic Computing Reliability**  
K. Toprasertpong (The Univ. of Tokyo & Stanford Univ.)  
**Title**  
Robustness to Device Degradation in Silicon FeFET-based Reservoir Computing  
**Packaging and 2.5/3D Assembly**  
K. Mysore (AMD)  
**Title**  
2.5/3D Package Reliability  
**Product Reliability**  
T. Zhang (Ansys)  
**Title**  
Design for Reliability (DFR) Aware EDA Solution for Product Reliability  
**Radiation Effect Reliability**  
E. Zhang (Univ. of Central Florida)  
**Title**  
Charge Trapping in Irradiated 3D Devices and ICs  
**Reliability Testing**  
R. Herrick (Robert Herrick Consulting)  
**Title**  
Reliability testing for silicon photonics and optoelectronics  
**RF/mmW/5G**  
J. Dunworth (Qualcomm)  
**Title**  
RF/mmW 5G/beyond 5G: advances & reliability  
**SiC Devices**  
P. Moens (onsemi)  
**Title**  
Evaluating SiC MOSFET Gate Reliability, Life Models and Safe Operating Area  
**System Electronics Reliability**  
Pradeep Lall (Auburn University)  
**Title**  
Assessment of Fracture Propensity of Flip-Chip Ball Grid Array Interfaces under Deformation and Fatigue Loads at Sustained High Temperatures  
**Transistors**  
Myunggil Kang (Samsung)  
**Title**  
Device design and reliability of GAA MBCFET

**Detail of Invited Speaker:** [https://www.irps.org/invited-speakers](https://www.irps.org/invited-speakers)
Gate/MOL Session

2A.1 “Challenges of gate stack TDDB in gate-all-around nanosheet towards further scaling” H. Zhou et al., IBM Research, presents GAA features and impact on TDDB reliability: Multi-VT integration, WSI and area scaling, spacer, Tsi.

Multi Vt and Integration

Inner Spacer and Bi-model

Wsi and Area Scaling

Tsi and TDDB

Gate/MOL Session

9A.2 “Joint Weibull-Fréchet model for dielectric breakdown in filament formation including reverse area scaling” E. Wu et al, IBM Research, presents a statistics-based model “Join Weibull-Fréchet” to characterize reverse area-scaling of RRAM TBD, and enabling reliability projection from test area to chip/product area.

Fig. 3. The joint PDF (Eq. 5) of the Weibull-Fréchet model for 100 and 10^4 μm^2 using the parameters in Fig. 5 (a)
**Transistor Session**

4A.1 “Fundamental understanding of NBTI degradation mechanism in IGZO channel devices”

Y. Zhao, et. al., KU Leuven, presents a comprehensive understanding of NBTI in IGZO TFTs with varying channel thickness and gate length.

**GaN Device Session**

6B.1 “PBTI in Scaled Oxide Submicron Enhancement Mode High-K Gallium Nitride Transistors,” S. Joy, et. al., Intel, presents E-mode HEMT with 2nm Hf-based dielectric (high-k) in Fabricated on 300 mm GaN-on-Si wafer

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**Figure 1.** (a) Schematic and TEM of gate-recessed, high-k E-mode GaN MOSHEMT in this work; (b) reported Power FoM ($R_{DSON}Q_{CG}$) of Intel GaN MOSHEMT [2]. (c) $I_D$ $V_G$ of $L_D=90$nm GaN MOSHEMT showing ON/OFF ratio>10^6, SS~80mV/dec, and $I_d<5pA/\mu m$ (d) no prominent increase in $I_d$ during PBTI measurements.
**Radiation Effect Reliability Session**

10C.1 “Soft-Error Sensitivity in SRAM of 3 nm Gate-All-Around (GAA) Technology” T. Uemura, et. al., Samsung Electronics, presents Alpha- and neutron-SERs in SRAMs manufactured with 3 nm bulk gate-all-around (bulk-GAA) process technology. The SER in SRAM of bulk-GAA is maximally 1.56X higher than in the same cell-size SRAM of bulk-FinFET. Moreover, shrinking cell size decreases the SER by a maximum of 0.38X in bulk-GAA. The SER of the minimum-size SRAM in bulk-GAA is lower than in bulk-FinFET.

![Diagram](image)

**ESD&Latch-up Session**

8C.1 “Insight into Latchup Risk in 28nm Planar Bulk Technology for Quantum Computing Applications” K. Servulova, et. al., imec. A Cryogenic environment is needed for quantum computing and a latch-up property will be changed. This paper presents well defined experiment and interpretation, and the current gain characteriztion of the parasitic bipolar transistors over wide temperature range is a valuable reference for future work.

![Graph](image)
RF/mmW/5G Session

4B.2 “A Methodology to address RF aging of 40nm CMOS PA cells under 5G mmW modulation profiles,” A. Divay, et. al, cea, presents a simplified methodology to link CW RF stresses to complex profiles, and improved lifetime for most complex 5G modulation due to output power/linearity constraints.

RF/mmW/5G Session

4B.1 “DC Reliability study of high-k GaN-on-Si MOSHEMTs for mm-Wave Power Amplifiers” B. O’Sullivan, et. al, imec, presents high-k GaN-on-Si MOSHEMTs for mm-Wave Power Amplifiers monolithically integrated on 200 mm Si substrates. Defects in HfO2 or Al2O3 result in significant $V_t$ instabilities, with dielectric-dependent charge emission kinetics: band alignment between high-k shallow defect levels and AlGaN conduction band enables full (Al2O3) or partial (HfO2) charge de-trapping.
Highlight Paper 5

Circuit Reliability Session

4C.1 “Demonstration of Chip Overclock Detection by Employing Tamper-aware Odometer Technology,” R. J. Diaz-Fortuny, et. al., imec, proposes a significant improvement of the tamper-aware odometer concept to obtain the degradation of a chip utilizing enhanced ring-oscillators-based degradation monitors. The authors present two new aging odometers designed in 28nm tech that, together with clear and concise data, allows avoiding the need of a pre-stress phase to obtain the age of a chip based on individual BTI and HCD RO readings. With the presented technology, the authors can unequivocally detect a previous overclock test to conducted intentionally to the chip’s digital circuitry.

System Electronics Session

5C.3 “Virtual FA methodology for DRAM: Real-time analysis and prediction method using Telemetry, Field data,” J. Lee, et. al, Samsung Electronics, presents Fast methodology of failure detection in deployed systems compared to conventional failure analysis flow. The paper describes a methodology that is widely conceptualized but in practice is hard to implement. The authors were successful in providing examples of failure modes that are classifiable on a database and are able to be resolved and confirmed through collaboration with customers. Both these elements are key to the success of this vFA methodology.
Failure Analysis Session


Reliability Testing Session

2B.1 “Modeling Dark Current Degradation of Monolithic InGaAs/GaAs-On-Si Nano-Ridge Photodetectors,” P. Hsieh, et. al., imec, thoroughly investigated dark current conduction mechanisms and degradation. The proposed semiempirical carrier emission/capture model successfully portrays the degradation and recovery, therefore enabling acceleration factor and device lifetime estimation, providing a more precise vision toward defect kinetics.
**Emerging Memory Session**

7A.4 "Comprehensive Reliability Assessment of 32Gb HfZrOx-Based Ferroelectric NVDRAM Memory," D. Ettisserry, et. al., Micron, presents array level HZO ferroelectric, and describes new reliability mechanisms.

**Memory Reliability Session**

3A.2 “Experimental Segmentation of Vertical Charge Loss Mechanisms in Charge Trap-Based 3D NAND Arrays,” L. Chiavarone, et. al., Micron, presents that vertical charge loss in charge trap 3D NAND arrays is characterized and modeled. The contributions of charge detrapping from bandgap-engineered tunnel stack and charge loss from silicon nitride storage node are experimentally separated for the first time.
Late news (Gate/MOL Dielectrics)

7B.4 "On-Chip Single-Shot Pulse Generator for TDDB Characterization on a Sub-nanosecond Timescale," M. Drallmeier, et. al., Univ. of Illinois, Presents an on-chip pulse generator fabricated in a 65-nm CMOS process capable of producing clean single-shot pulses with amplitude up to 6 V and pulse width as short as 200 ps. Experimentally investigates use of pulse generator on MOS gate oxide breakdown voltage on a sub-ns timescale and to assess the validity of the power-law model.

Late news (Transistor Session)

7B.5 "Modeling of Negative Bias Temperature Instability (NBTI) for Gate-all-around (GAA) Stacked Nanosheet Technology," J. Fang, et. al., Synopsys, Implements a physics-based NBTI framework involving trap generation and trapping, validates against measured data, investigated the impact of nanosheet thickness, channel stress and SiGe channel on GAA characteristics, demonstrates a TCAD to SPICE framework.
Late news (Gate/MOL Dielectrics)

8C.4 "On-Chip Single-Shot Pulse Generator for TDDB Characterization on a Sub-nanosecond Timescale," M. Drallmeier, et. al., Univ. of Illinois, performed a thermal analysis of a server SoC considering a realistic layer stack configuration mounted on a printed circuit board (PCB) with an active heat sink for the cooling solution and proposes a holistic co-optimization of the thermal interface material, cooling solution and SoC design.

Figure 1. 3D cross-sectional view of the SoC packaging to the cooling solution. Convective boundary conditions in terms of HTC are used on the top of the heat sink and the bottom of the PCB. The side surfaces of the heat spreader are assumed to be adiabatic conditions.

Figure 15. Variation of maximum temperature ($T_{max}$) with respect to time for multiple cases of 50% to 100% power workload variations.