IN100 Datasheet

IN100

Ultra-Low Power Bluetooth Beacon SoC

Key Features

- **Bluetooth Low Energy 5.3 Compliant**
  - Enhanced privacy mode support
- **Beacon Modes**
  - Proprietary
  - Bluetooth SIG compliant
  - iBeacon/Eddystone/Altbeacon compliant*
- **Ease of Use**
  - Config and use
  - No software programming required
- **Memory**
  - 4Kb eFuse memory
    - Advertising payload storage
    - Manufacturer ID
  - 4KB SRAM
    - Dynamic payload storage
- **Low Power Mode Advertising**
  - Continuous advertising
  - Event-triggered advertising
- **RF Radio**
  - 2.4GHz frequency band RF transmitter
  - MedRadio band support
  - Programmable TX output power, up to +5dBm
- **System Power Consumption**
  - Sub-uW power consumption for multi-year operation on a tiny battery
  - Sleep mode < 650nA with 32kHz RC ON
- **Peripheral**
  - 1 UART
  - 1 I2C
  - Pulse Count Interface for digital sensor input
  - Built-in ultra-low-leakage load switch x 2
  - Sensor ADC, 11bit
    - Chip temperature measurement
    - VCC voltage measurement
    - 4 channels for customer use
- **Clock Sources**
  - 26MHz XO crystal
  - 32.768kHz RTC crystal (optional)
- **Security and Privacy**
  - AES-128 based authentication
  - AES-128 based encryption
  - Privacy protection: resolvable private address
  - Anti-Cloning: time-varying payload in the beacon
- **Power Supply**
  - Integrated low leakage LDO
  - 1.1 – 3.6V input
  - Single cell 1.5V battery support
- **Operating temperature**
  - -40°C ~ +85°C (industrial, see ordering info)
  - -40°C ~ +125°C (full range industrial, see ordering info)
- **Packaging**
  - DFN8 2.5mm x 2.5mm
  - QFN18 3.0mm x 3.0mm
- **Typical Applications**
  - Standalone retail beacon
  - Wireless sensor
  - Asset tracking
  - Beacon tag for RTLS (Real Time Location System)
  - Active RFID
  - Low power alarm system
  - Wireless ID tag for healthcare
  - Wireless industrial application
  - Fitness and wellness

** iBeacon is a trademark of Apple Inc.*
** Eddystone is a trademark of Google Inc.*

About Documentation

Document name	Datasheet	
Part number	IN100	
Control number	IN1EDOC-DS-IN100-EN-V1.0	For external use
Revision	V1.0	

Product status	Document content	Data status
In Development	Objective Specification/MRD	Target Specification. Revised and supplementary data will be published later
Engineering Sample	Specification with measured data on E/S	Data based on early E/S sample testing
Customer Sample	Specification with measured data on the early production samples	Data based on early production samples. Revised and supplementary data may be published later.
Mass Production	Description of all functional features	Document contains final product specification

This document applies to the following products:

Document name	Applicable products	Product status
IN100 Datasheet	IN100-D1-R-RC1I	Mass production
	IN100-Q1-R-RC1I	Mass production
	IN100-D1-R-RC1F	Engineering sample
	IN100-Q1-R-RC1F	Engineering sample

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1. Product Overview

IN100 is a member of InPlay's NanoBeacon™ SoC product family, which supports Bluetooth low energy beacons in the ISM 2.4GHz frequency band and a proprietary beacon mode in either the 2.4GHz ISM frequency band or the MedRadio frequency bands. This SoC device features an efficient and configurable state machine, non-volatile memory for user pre-defined data payload, and data SRAM for dynamic data storage. The device includes an analog to digital converter, security engine and power management in a QFN form factor package as small as 2.5mm x 2.5mm. The device has very low power consumption and simple BOM requirements. It is ideal for coin cell battery or single cell 1.4V/1.5V battery-powered applications such as disposable beacon tags or wireless smart sensors.

Software programming free Bluetooth: The device is designed for maximum ease of use. There's no need to do any Bluetooth-related software programming in order to use this device. Once the device is properly configured, it automatically transmits Bluetooth Low Energy advertising packets, or proprietary-format advertising packets. The advertising data payload can be predefined user data stored on-chip, or dynamic data acquired from sensors or an external microcontroller. The NanoBeacon Config PC GUI tool provided by InPlay allows the user to easily configure the advertising mode and data payload.

Single cell (sub-1.5V) battery operation, Nanowatt power consumption: The device can operate at battery voltages as low as 1.1V, so a popular 1.5V single cell battery is sufficient to power the device. When the device is operating in sleep mode, it consumes less than 650nA from the battery.

Flexible features for pairing with an MCU & sensors: In addition to the standalone beacon mode, the device is designed to pair with a companion MCU and/or sensors. When the device is used with a microcontroller, the adverting data payload and control mode can be changed on-the-fly via the UART interface. Sensors with either analog or digital outputs can be used with the device. It supports multiple ADC input channels with 11-bit resolution. It has a linear scaling post-processing unit to condition readings before transmitting them wirelessly. In addition, there are two low-leakage load switches that turn power on or off to any external circuitry, including the sensor ICs.

Simple system BOM: The device does not require external RF matching components when interfacing to a 50Ω impedance. It does require a 26MHz crystal for accurate local oscillator generation. For applications that require an accurate real-time clock, a 32.768kHz crystal must be installed on-board. Both the 26MHz and 32.768kHz crystal interfaces provide programmable on-chip capacitors that eliminate the need for on-board load capacitors for most crystals.

Security engine: A built-in hardware security engine supports AES-128 and EAX encryption with/without authentication. A built-in True Random Number Generator (TRNG) facilitates secure applications.

Figure 1 shows the system block diagram of the NanoBeacon™ SoC IN100 product family. Features available will vary by part number. For more information on available features of different devices, please refer to Ordering information.

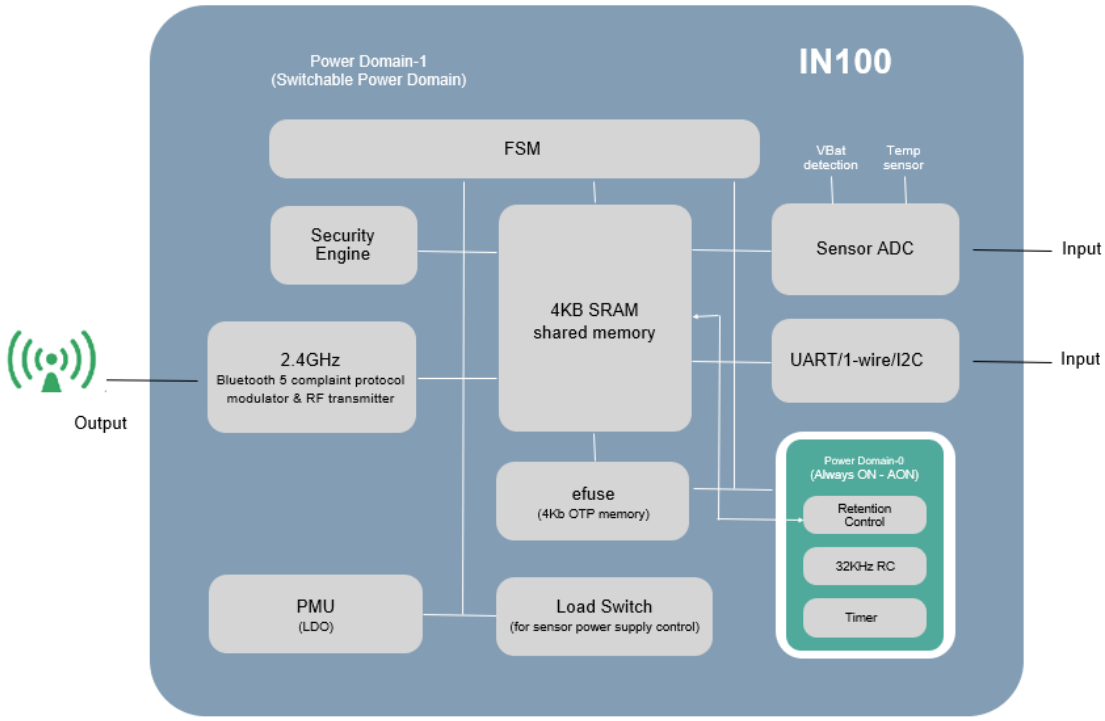


Figure 1 : System block diagram

Memory: The device has two types of memory built in.

- 4Kb OTP memory (eFuse): To store the user advertising data payload, security key and predefined register settings with one-time programming prior to usage.
- 4KB SRAM: For dynamic advertising data storage. Data in SRAM can be retained in memory during sleep mode when only the always-on (AON) domain is active.

Advertising data: The device can do non-connected advertising.

- Predefined data: Data is either stored in eFuse OTP memory or on-chip SRAM.

- Real time measurement data: Measurements come from internal on-chip sensors or external sensors with either analog or digital outputs to the device.

Types of advertising & data encryption: Continuous advertising and event-driven advertising are available; data can be encrypted or unencrypted, with or without authentication.

- Continuous advertising: Upon power-on, an advertising beacon is sent in every advertising interval, which is configurable.
- Event driven advertising: An advertising beacon is sent only when triggered by external events. An example event is when a sensor ADC measurement is larger or smaller than a predefined threshold.

The device supports privacy with a random or resolvable advertising address. It supports enhanced privacy of the user data payload through the built-in hardware security engine.

Load switch control: Two power supply switches are available to provide power to any external circuitry, including sensor ICs. These two switches can be event-driven or timer-driven.

- Switch 0 (SW0), ties the supply pin of the powered device to VCC when ON.
- Switch 1 (SW1), ties the supply pin of the powered device to GND when ON.

Power domain: There are two power domains, Always-ON (AON) domain and Dynamic ON/OFF Power Domain (DOOPD).

Figure 2 shows the workflow and features of the NanoBeacon™ SoC IN100 product family.

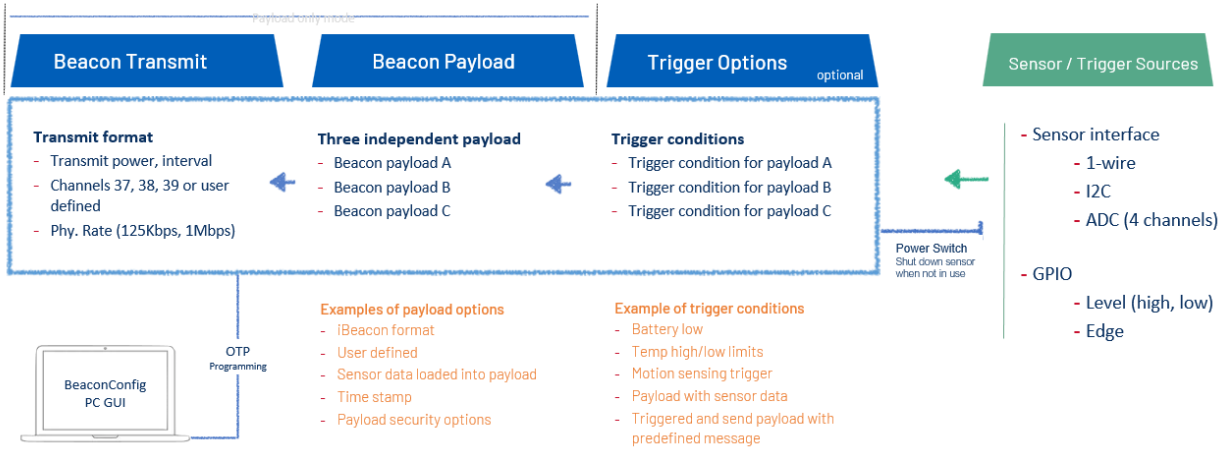
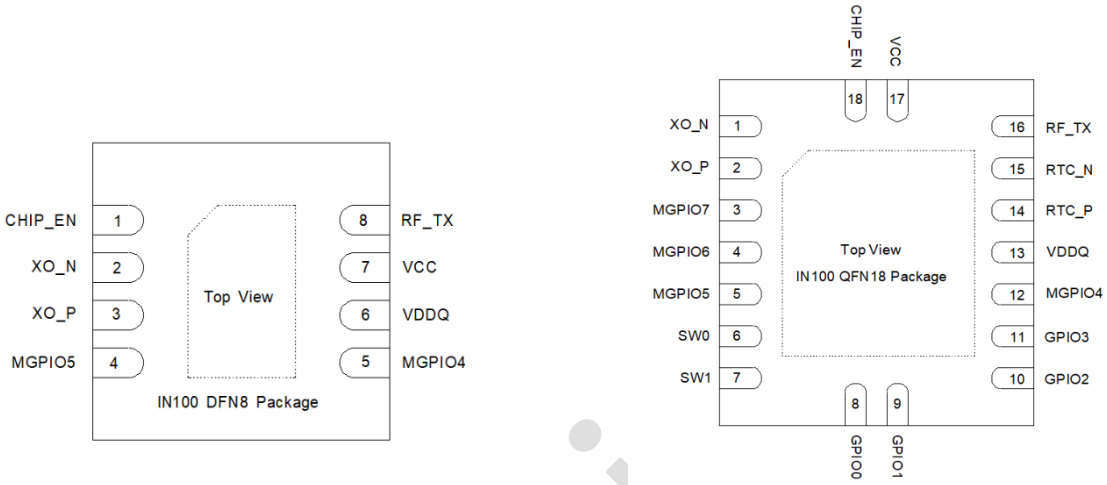


Figure 2 : NanoBeacon™ features overview

2. Package Pin Out Information

The device is offered in both DFN8 & QFN18 packages (denoted IN100-D1 and IN100-Q1, respectively). Both packages have an exposed paddle that must be connected to the system board ground.



(a) IN100-D1-R-RC1I(F) (b) IN100-Q1-R-RC1I(F)

Figure 3 : Pin assignments

2.1. Pin definition

Table 1 : IN100 QFN18 pin and pinmux info

QFN18 Pin #	Pin name	Pin type	Description	UART	I2C	Pulse counting	ADC
1	XO_N	Analog	26MHz XO N				
2	XO_P	Analog	26MHz XO P				
3	MGPIO7	MGPIO	Mixed signal GPIO		Any GPIO 2~5 & 7	Any GPIO	ADC CH3
4	MGPIO6	MGPIO	Mixed signal GPIO			Any GPIO	ADC CH2
5	MGPIO5	MGPIO	Mixed signal GPIO		Any GPIO 2~5 & 7	Any GPIO	ADC CH1
6	SW0	Switch	IO power switch				
7	SW1	Switch	IO ground switch				

QFN18 Pin #	Pin name	Pin type	Description	UART	I2C	Pulse counting	ADC
8	GPIO0	DGPIO	Digital signal GPIO	UART RXD	Any GPIO 2~5 & 7	Any GPIO	
9	GPIO1	DGPIO	Digital signal GPIO	UART TXD	Any GPIO 2~5 & 7	Any GPIO	
10	GPIO2	DGPIO	Digital signal GPIO		Any GPIO 2~5 & 7	Any GPIO	
11	GPIO3	DGPIO	Digital signal GPIO		Any GPIO 2~5 & 7	Any GPIO	
12	MGPIO4	MGPIO	Mixed signal GPIO		Any GPIO 2~5 & 7	Any GPIO	ADC CH0
13	VDDQ	I/O power	eFuse memory Programming power supply				
14	RTC_XO_P	Analog	32.768K RTC P				
15	RTC_XO_N	Analog	32.768K RTC N				
16	RF_TX	Analog RF	2.4G RF TX output				
17	VCC	Power	Power supply & IO reference voltage				
18	CHIP_EN	Analog	Chip enable				

Table 2：IN100 DFN8 pin and pinmux Info

DFN8 Pin #	Pin name	Pin type	Description
1	CHIP_EN	Analog	Chip enable
2	XO_N	Analog	26MHz XO N
3	XO_P	Analog	26MHz XO P
4	MGPIO5	GPIO	UART TXD
5	MGPIO4	GPIO	UART RXD
6	VDDQ	I/O Power	eFuse memory programming power supply
7	VCC	Power	Power supply & IO reference voltage
8	RF_TX	Analog RF	2.4G RF TX output

Note: The GPIOs and MGPIOs (when used as digital I/Os) are in the VCC power supply domain.

3. Function Block Description

3.1. Overview of beacon packets and beacon data set creation

The device is designed to be configure-and-use, so that the users do not need to do any software or application programing. *Figure 4* shows the advertising packet format, number of packets that are supported, and packet control settings. The user can employ the provided NanoBeacon Config PC GUI tools to generate the configuration file to be programmed into the eFuse memory of the device.

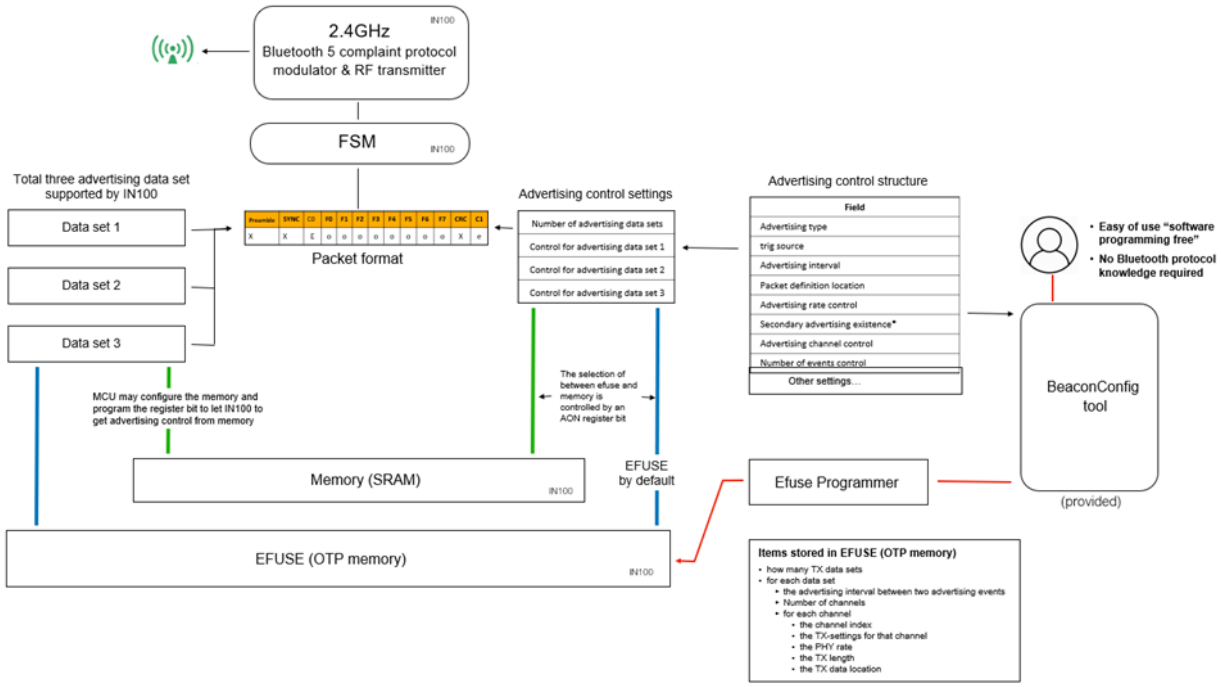


Figure 4 : Advertising packet and advertising packet creation process overview

3.2. Advertising control and packet definition

There are two advertising modes: continuous and event driven. In continuous advertising mode, advertising occurs every advertising interval upon power-on; In event-driven advertising mode, advertising only occurs when triggered by specified external events. For example, event-driven advertising can happen after some sensor ADC measurements are larger or smaller than a predefined threshold.

The device supports three different data sets for advertising. The control of the advertising is stored in eFuse memory or SRAM as shown in *Figure 4*.

3.3. eFuse memory (OTP)

The device provides a 4Kbit eFuse memory to store the configuration and advertising data packet information. The eFuse memory is organized as 256 16-bit words. The data in the eFuse memory is broken into 4 regions.

- Region 1 contains the commonly used configuration data, which is predefined and has fixed length.
- Region 2 contains more flexible configuration data, specified through register read/write based on different trigger conditions. This region has a user-defined length and is application-dependent.
- Region 3 contains the data that needs to be transmitted and how the data is transmitted. It also has a user-defined length and is application-dependent.
- Region 4 contains the instruction definition of the I2C protocols and is application dependent.

Region 2, 3 and 4 are optional and they may not be present. The presentation of the Region 2, 3 and 4 are specified in the region 1.

Table 3 : eFuse memory structure definition overview

Region	Description	Length
1	Commonly used configuration data.	Fixed
2	More flexible configuration data through register read/write.	Application dependent
3	Data to be transmitted and how the data is transmitted.	Application dependent
4	I2C instruction definition	Application dependent

The detailed content of the regions of the eFuse memory can be automatically generated by NanoBeacon Config PC GUI according to user's configuration and application.

NOTE that the eFuse memory can only be programmed once. Bits in the eFuse memory can only be written to 1 by the programmer and cannot be cleared to 0 afterwards.

3.4. SRAM

The device has an on-chip 4KB SRAM which can be used for advertising control and data storage. The content of the SRAM can be dynamically changed or updated by the external MCU.

3.5. Advertising control

The device supports two advertising modes, continuous or event triggered.

3.5.1. Continuous advertising mode

Advertising occurs every advertising interval. The advertising packet is transmitted periodically with the advertising interval specified in region 3 of the eFuse memory or the SRAM configuration.

3.5.2. Event-driven trigger mode

Advertising packet is only transmitted when a given conditions are met, which is also specified in region 3 of the eFuse memory or the SRAM configuration.

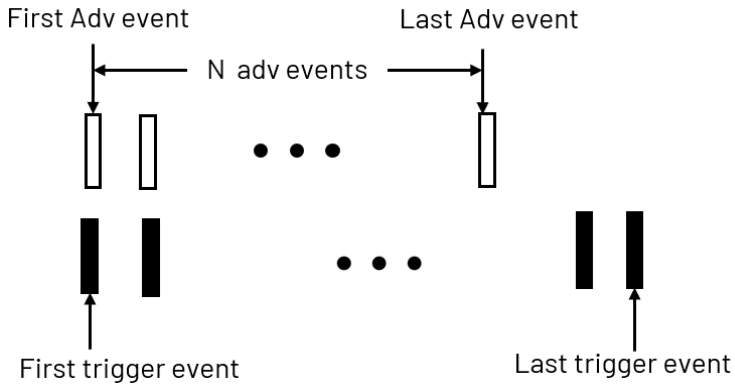
The event-driven trigger mode can be further divided into the following 4 modes:

- Mode 0: After the event is triggered, the device begins to advertise with the interval specified. The device keeps advertising for a specified number of advertising events regardless the status of the current trigger event, as shown in *Figure 5 (a)*. After finishing the specified number of advertisings, the device will stop advertising and remain in sleep forever.

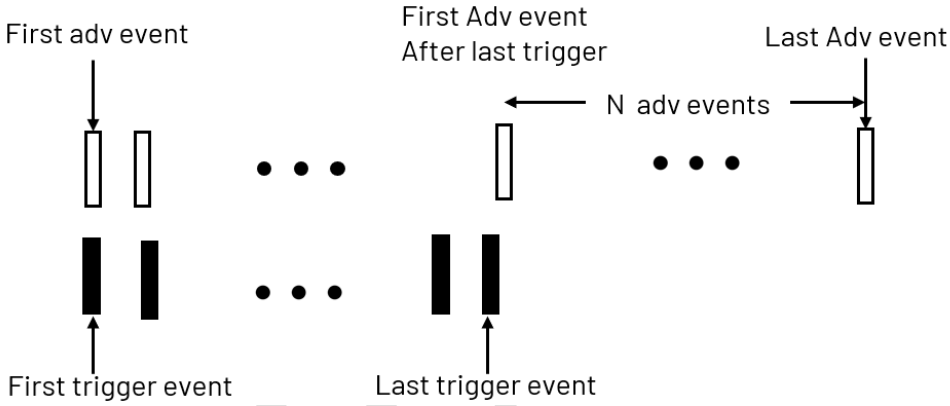
- Mode 1: After the event is triggered, the device begins to advertise with the interval specified. Different from mode 0, during every advertising wakeup, the device checks whether the sensor event is valid. After the last valid trigger event, the device keeps advertising for a specified number of advertising events as shown in *Figure 5 (b)*. Advertising will continue until the sensor event is not present. After finishing the advertising, the device will be in sleep forever.

- Mode 2: Similar to mode 0 except after finishing the advertising sequence, the device will periodically wake up to check the sensor status to see if it is triggered. If it is triggered again, the device will perform a specified number of advertising events.

- Mode 3: Similar to mode 1 except after finishing the advertising, the device will periodically wake up to check the sensor status to see if it is triggered. If it is triggered again, the device will perform a specified number of advertising events.



(a) Mode 0



(b) Mode 1

Figure 5 : Trigger modes

The trigger of the events can be one of the following conditions:

Table 4 : Trigger condition description

Condition index	Condition	Description
0	Battery too low	The battery level measured through the internal ADC is lower than a threshold provided in region 1 of the eFuse memory or SRAM.
1	Temperature too high	The temperature level measured through the internal ADC is higher than a threshold provided in region 1 of the eFuse memory or SRAM.
2	Temperature too low	The temperature level measured through the internal ADC is lower than a threshold provided in region 1 of the eFuse memory or SRAM.

Condition index	Condition	Description
3	Sensor 0 level too high	An external sensor connected to an MGPIO pin measured through the internal ADC is higher than a threshold provided in region 1 of the eFuse memory or SRAM. Sensor 0 can be specified as one of the GPIO inputs using control registers*.
4	Sensor 0 level too low	An external sensor connected to an MGPIO pin measured through the internal ADC is lower than a threshold provided in region 1 of the eFuse memory or SRAM.
5	Sensor 1 level too high	An external sensor connected to an MGPIO pin measured through the internal ADC is higher than a threshold provided in region 1 of the eFuse memory. Sensor 1 can be specified as one of the MGPIO inputs using control registers*.
6	Sensor 1 level too low	An external sensor connected to an MGPIO pin measured through the internal ADC is lower than a threshold provided in region 1 of the eFuse memory or SRAM.
7	GPIO wakeup	Any GPIO-triggered wake up. The wake-up condition can be specified through control registers*.

Note: the control register content can be generated by the NanoBeacon Config PC GUI tool provided by InPlay.

3.5.3. Advertising data source

Each advertising packet may contain up a sequence of up to 15 fields. Field 0 may contain specified header and/or address information, while all other 14 fields may contain one of the following types of data.

Table 5 : Advertising data source

Data type	Description
Predefined Data	The data (and their length) is defined in the eFuse memory directly and may not be changed later.
Timer value	Values from AON timers, or the converted SEC_CNT value in 0.1 second or 1 second resolution.
Random number	A random number created through the LFSR (see chapter 4.6). The random value might also be used in EAX encryption as the salt.
Internal Temperature/Battery voltage measurement	Internal ADC measurements of the device temperature or the VCC voltage value.
External analog sensor measurement	Internal ADC measurement of a signal from the external analog sensor through MGPIO 4 to 7.

Data type	Description
InPlay UUID	The InPlay UUID (universally unique identifier) value stored in the eFuse memory.
Customer UUID	The Customer UUID value stored in the eFuse menory.
EID	The EID value defined in the EddyStone specification.
Message authentication Code(tag)	The message authentication code (tag) value generated by the AES-EAX algorithm.
ADV CNT	The advertising counter value.
Sleep count	The number of sleeps since power up.
Digital GPIO status	The current or wakeup GPIO value.
Pulse counting value	The counting value from the pulse width or pulse sequencer counter logic from external digital sensors.
Register value	The value of a register from a specific address.

For details of the advertising control and packet definition in region 3 of the eFuse memory or SRAM, please refer to the NanoBeacon Config PC GUI tool and its user manual.

4. Sub-system Description

4.1. UART

A UART interface is provided as the additional control or debugging interface. See chapter 2.1. External devices may access the device's internal registers, memory, and eFuse memory through a UART interface. The interface supports byte-sequence commands. The NanoBeacon Config PC GUI uses the UART interface to communicate with the device, and other controllers can also access the device internal information through the UART interface.

4.1.1. UART speed detection

The UART block can automatically detect the speed of the external UART command, as its default baud rate is 115,200Hz when using the 26MHz external crystal. If the external device needs a different baud rate, and the UART auto detection feature is enabled, the external device can send in multiple commands at the new rate. The internal logic will automatically detect the new rate and reply with an ACK command to the external device when the detection is successful.

It is recommended to use the sequence of operations shown in *Figure 6* to achieve stable UART communication after initial device power-up (cold/warm boot) or UART sleep change.

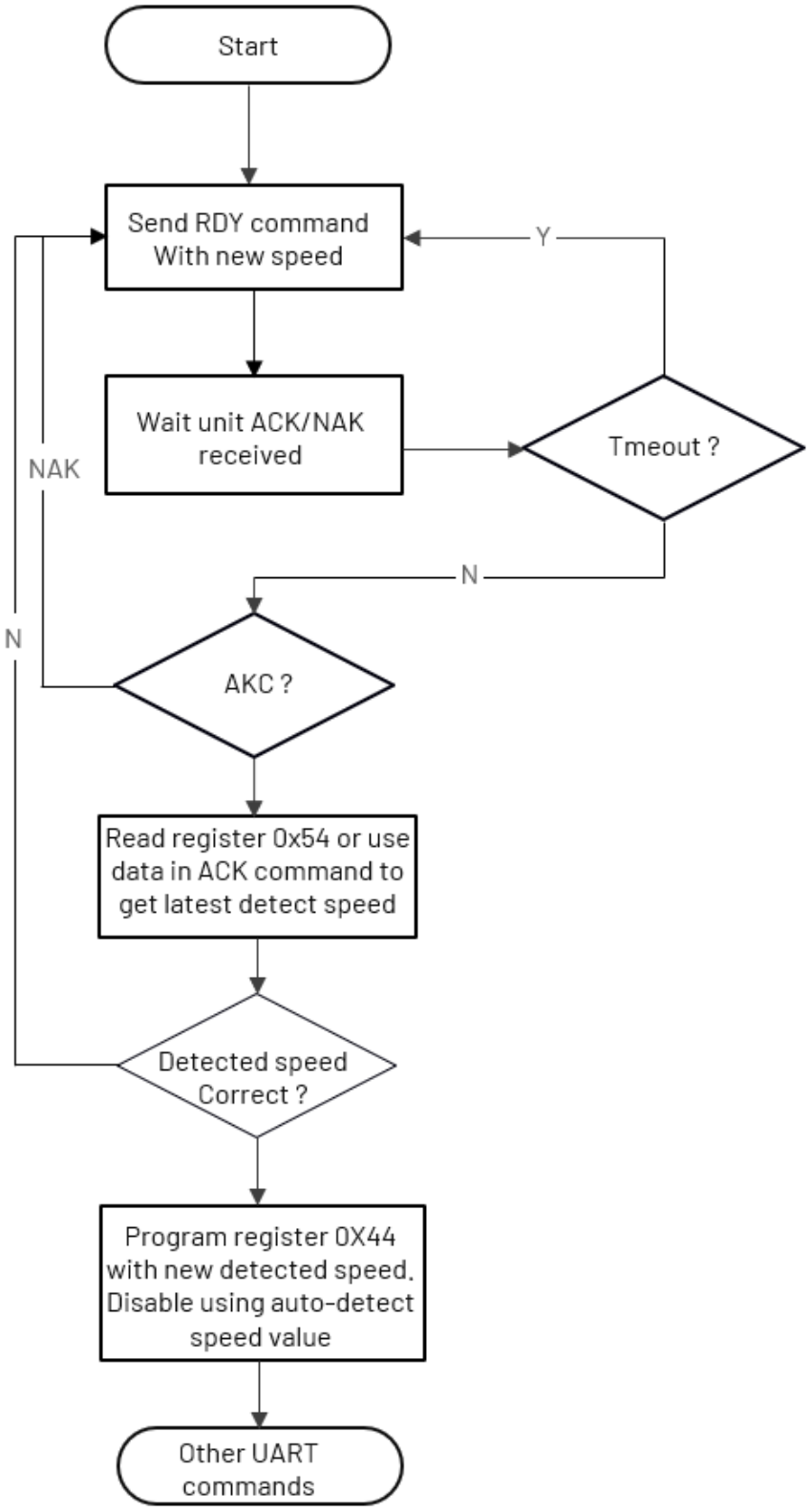


Figure 6 : Recommended UART speed detection sequence

4.2. I2C

To communicate with sensors that do not support UART, an I2C master is provided. The I2C master can communicate with multiple external I2C slave sensors/devices with different slave addresses in sequence. The I2C commands are stored in the region 4 of the eFuse memory. For each I2C slave, the I2C master (based on the preset values in the eFuse memory) can program registers or read back values. The I2C master can also insert delays between two I2C commands to give the I2C slave time to respond to the previous command. The read-back value will be stored in memory and can be broadcast through as part of packet payload. The operations of the I2C master can be defined through the NanoBeacon Config PC GUI. The I2C interface SCL and SDA pins can refer to *Table 1*.

4.3. Pulse train counting and pulse width detection

To interface with some external digital-interface sensors, the device can count the number of pulses in a pulse sequence (*Figure 7*). the device can also detect the high/low width ratio of the sequence of pulses (pulse-width modulation, *Figure 8*). The ratio between the time high and time low of a pulse can be encoded as a digital 0 or 1. The sequence can be applied to any of the available pins defined in *Table 1* above.

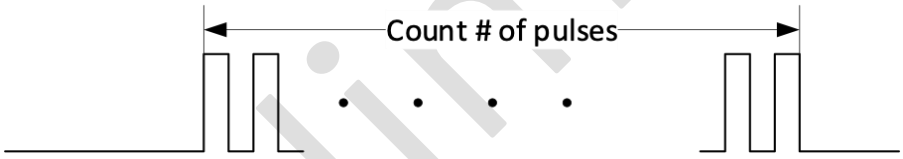


Figure 7 : Pulse counting

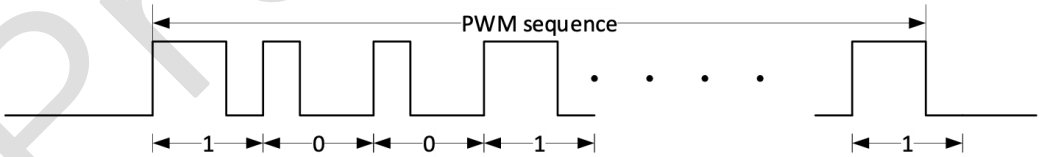


Figure 8 : PWM sequence

4.4. Sensor ADC

The Sensor ADC has 11 physical bits and can convert at a maximum of 64KSPS. The input to the ADC is preceded by a multiplexer which enables the user to sample up to 4 different channels, as shown in *Figure 9*. The package options and the pin assignments are shown in

Figure 3 and *Table 1*. In addition, the ADC can be used to measure the internal VCC (shown as VBAT in *Figure 9*) voltage level or the chip temperature. The required voltage reference (VREF) to the ADC can be selected from multiple sources, including an on-chip 0.8V reference (V0P8), the VCC voltage divided by 2, or external channels. The VREF shall not exceed 0.8V. The input voltage range to the ADC shall be between 0V and 2*VREF.

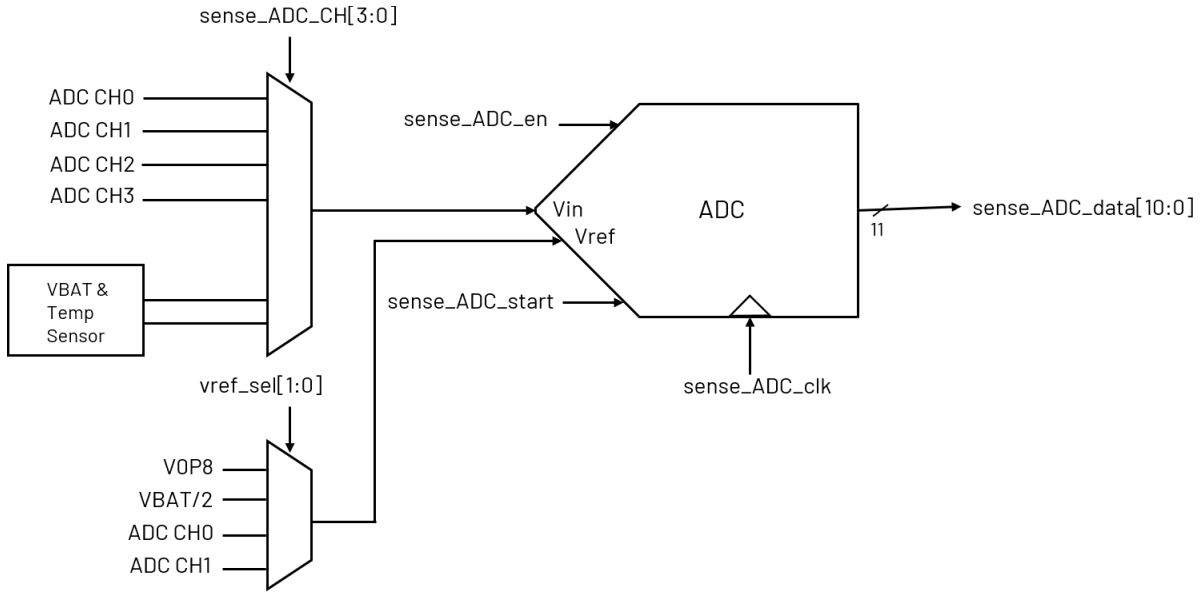


Figure 9 : Sensor ADC block diagram

4.4.1. On-chip VCC monitoring

Measured at: Ta = 25°C, VCC=3.0V, unless otherwise noted.

Table 6 : VCC monitoring characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Resolution	Using on-chip V0P8 as reference		0.3		mV/LSB
Range	Input to ADC = 0.4*VCC. Input range of ADC is 0V - 1.6V (FS).	1		3.6	V
Accuracy	With VREF calibration only	-3.3	1.1	3.3	%
	With ADC offset and VREF calibration	-0.9	0.3	0.9	%

4.4.2. On-chip temperature monitoring

Measured at: Ta = 25°C, VCC= 3.0V, unless otherwise noted.

Table 7 : Temperature Monitoring Characteristics

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Resolution	Using on-chip V0P8 as reference		-0.4		°C/LSB
Range		-40		85	°C
Accuracy	With VREF calibration	-4.5	1.5	4.5	%
	With ADC offset and VREF calibration	-2.7	0.9	2.7	%

4.4.3. MGPIO analog measurement

Measured at: Ta = 25°C, VREF=0.8V, VCC=3.0V, unless otherwise noted.

Table 8 : MGPIO Analog monitoring characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Resolution	Using on-chip V0P8 as reference		1.6		mV/ LSB
Range	Input range to the MGPIO PIN is 0V – 1.6V (FS).	0		1.6	V
Accuracy	With VREF calibration only	-3.3	1.1	3.3	%
	With ADC offset and VREF calibration	-0.9	0.3	0.9	%

The device supports ADC value linear scaling to convert from raw voltage to the meaningful user defined unit. For example, the device can convert a temperature sensor raw voltage output captured by its ADC to a Celsius temperature unit.

4.5. Load switch - power supply control

The device also provides two load switch pins. Switch 0 (SW0) provides a low impedance path to VCC when turned on, while Switch 1 (SW1) provides a low impedance path to ground when turned on as shown in *Figure 10*.

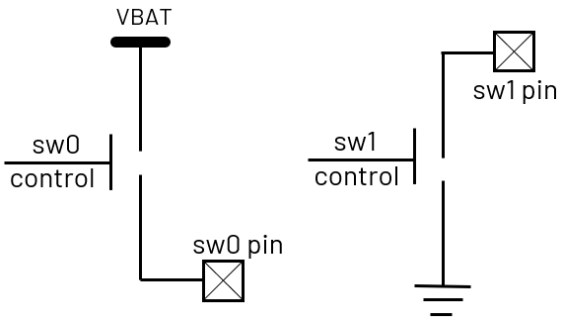


Figure 10: Load switch pins

These switches can be automatically turned on or off when the sensor ADC is measuring external analog signals through a mixed-signal GPIO pin or when the pulse counting/PWM detection logic is running to count pulses on the GPIO pins.

4.6. Random number generator

A 64-bit random number generator based on a linear feedback shift register (LFSR) is provided. The initial value of the LFSR is obtained from the least-significant bits of multiple sensor ADC channels and the initial value from the SRAM readout. The random values can be used in resolvable and non-resolvable address generation or the random number value in an advertising packet payload.

4.7. Timers (Always-on domain)

A 32-bit count-down timer and a 64-bit count-up timer are provided in the always-on power domain running with the 32kHz sleep clock. The 64-bit count-up timer value can be converted to units of 0.1s, 1s or customized unit values.

Another 32-bit watch dog timer is also provided which can be used to reset the device upon expiration.

4.8. Sleep and wake-up settings

Once VCC power is provided and the CHIP_EN pin is asserted, the device will start working according to the eFuse memory settings. If there is no valid eFuse memory settings present, an external MCU can control and configure the device through the UART interface.

The device can go to sleep automatically after event checking or transmission based on configuration. In this mode, the chip will also automatically wake itself up after the given time. During sleep, the contents of the 4Kbyte memory will be retained. If automatic sleep is not

configured, the device can also be put to sleep mode through a UART command. The user can wake up the device through a configured GPIO input.

4.9. Power management

4.9.1. Power supply

IN100's on-chip PMU supports a wide supply voltage range from 1.1V to 3.6V (*Figure 11*).

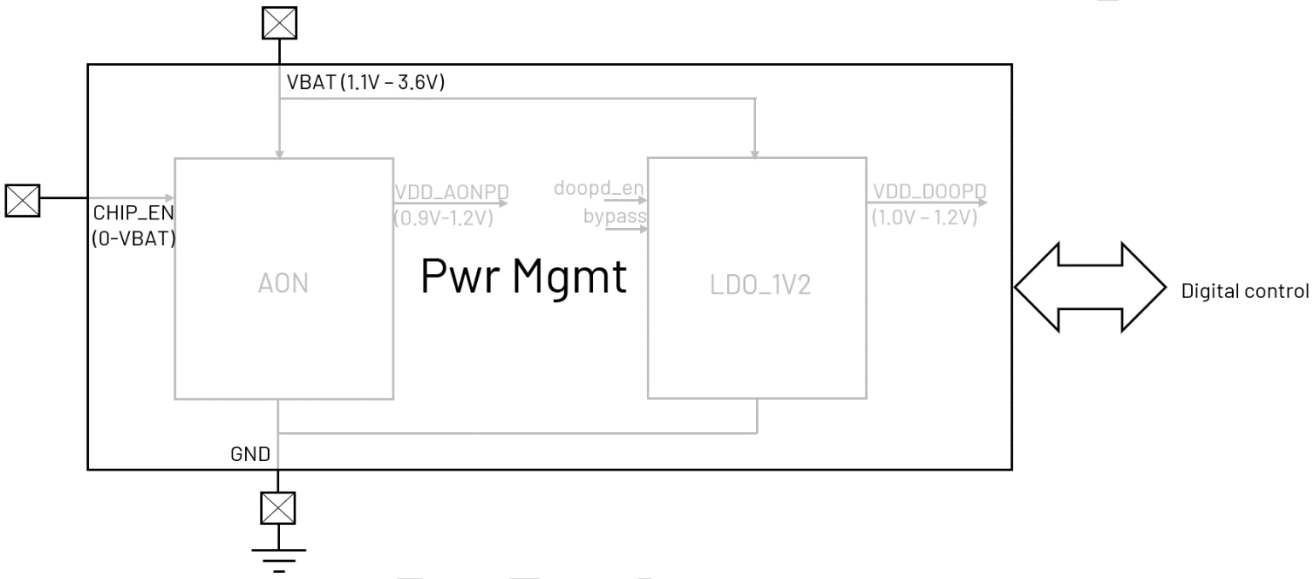


Figure 11 : Power management generates 2 domains (AON & DOOPD) from VCC

Power domain: There are two power domains, AON and DOOPD.

AON (Always ON domain): The AON domain includes an always-on LDO for the power supply, the 32kHz clock, a timer, and retention of data in the 4KB SRAM. The AON logic is powered by the AON LDO and its clock frequency is 32kHz. The 32kHz clock can be from an internal RC clock source or an external clock source such as a 32kHz RTC clock. The AON logic has a sleep timer inside, which can wake up the DOOPD (Dynamic On and Off Power Domain).

DOOPD (Dynamic On and Off Power Domain): The DOOPD consists of the GFSK modulator and RF transmitter, eFuse OTP memory, SRAM, the security engine and the peripherals.

Power operation modes:

Sleep mode: Only the AON domain is on. The DOOPD domain is shut down.

Active Mode: Both power domains are on.

Shut Down mode: Both power domains are powered down. The leakage current at this mode is less than 10nA.

4.10. Clock sources

There are four types of clock sources. They are: RC 32kHz, RTC 32.768kHz, RC 26MHz and XO 26MHz. RC 32kHz is the default clock source for the AON power domain.

The device's clock system is designed to provide clocks to all subsystems that require clocks, and to allow switching between different clock sources without degrading system performance or power consumption.

The clock calibration uses the accurate 26MHz crystal to determine precisely the frequency of the RC 32kHz. After the calibration, the device uses a division core to get the period and frequency of the RC 32kHz. The division core will also be used for conversion between number of sleep cycles and time slots, or other required time unit conversions.

4.10.1. RC 32kHz

The nominal value of this clock is 32kHz. The clock rate can vary from 16kHz to 48kHz and is calibrated by the XO clock. The AON (Always-On) domain uses this as clock source.

Clock performance reported below was measured at the following condition: Ta = 25°C, VCC=3.0V, unless otherwise noted.

Table 9 : 32kHz RC oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	Default RC setting		24		kHz
Temperature coefficient	Default RC setting		See *Figure 12*		Hz/°C

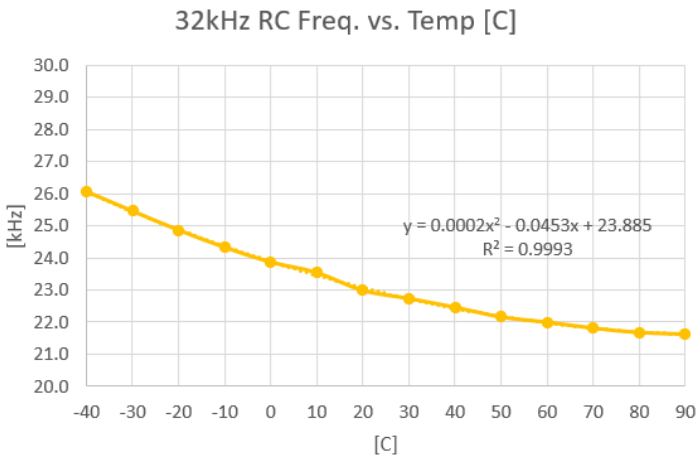


Figure 12 : 32kHz RC frequency vs. temperature

4.10.2. RTC 32.768kHz

This is a stable and high accurate 32kHz clock. It is optional, and for some applications, this crystal may not be installed. During cold boot, the RC 32kHz is the default clock for AON. After cold boot, If the RTC crystal is installed and the corresponding eFuse memory is set, the FSM (Finite State Machine) will enable the RTC clock and switch to the RTC 32.768 kHz clock for AON operation. *Figure 13* shows a block diagram of the 32.768kHz crystal. The device also supports an external 32.768kHz clock source as input as shown in *Figure 14*.

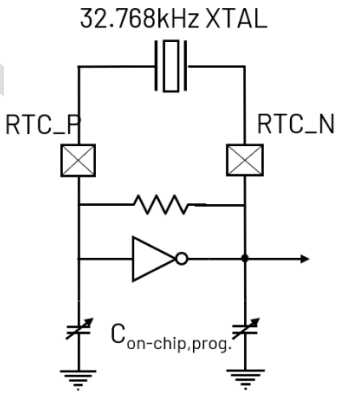


Figure 13 : 32.768kHz crystal

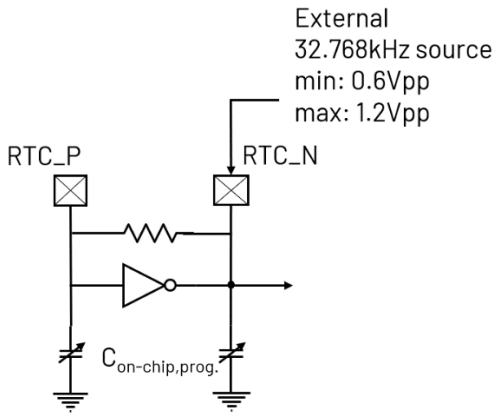


Figure 14 : External 32.768kHz clock source

Clock performance reported below was measured at the following condition: Ta = 25°C, VCC=3.0V, unless otherwise noted.

Table 10 : 32.768kHz RTC oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Crystal frequency			32.77		kHz
Crystal frequency tolerance	Including aging and temp. drift	-500		500	ppm
ESR			30	100	kohm
On-chip CL	Differential, programmable in 0.5pF steps	0.5		8	pF
CL crystal load capacitance	Differential	4	7	12	pF

4.10.3. RC 26MHz

RC 26MHz is a 26MHz high-frequency ring oscillator which provides a clock source while the crystal oscillator is starting up. The CPU will use RC 26MHz by default after code boot or wake-up from sleep mode and may switch to the XO clock after it becomes stable.

Clock performance reported below was measured at the following condition: Ta = 25°C, VCC=3.0V, unless otherwise noted.

Table 11 : 26MHz RC oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Oscillation frequency	Programmable with 1MHz resolution	16	26	48	MHz
Temperature coefficient			TBD (-0.15)		%/°C

4.10.4. XO clock

The XO clock is the high-frequency, high-precision clock source for 26MHz operation. The XO clock is sourced from an external 26MHz crystal as shown in *Figure 15*. The XO is controlled by the AON power state and is enabled by default after cold boot. This clock can be divided down to 13MHz, 2MHz and 1MHz upon the DOOPD requirements.

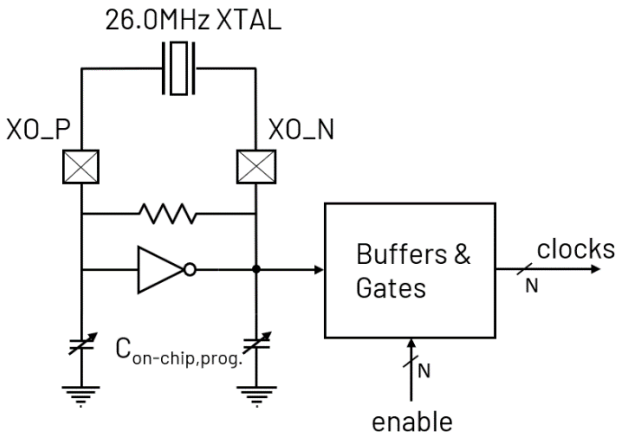


Figure 15 : XO clock source

Clock performance reported below was measured at the following condition: Ta = 25°C, VCC=3.0V, unless otherwise noted.

Table 12 : 26MHz crystal oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Crystal frequency			26		MHz
Crystal frequency tolerance		-40		40	ppm
ESR			60	200	ohm
Lm, motional inductance	(*1)		17	35	mH
Cm, motional capacitance	(*1)		2.2	3	fF

Parameter	Test conditions	Min.	Typ.	Max.	Unit
CL crystal load capacitance	(*1), differential		6	10	pF
C0	(*1)		0.7	3	pF
On-chip CL	Differential, programmable in 0.5pF steps	0.5		8	pF
Start-up time			500	1000	us

Note: Crystal data sheet must meet these requirements.

4.11. eFuse memory programming (OTP)

eFuse (OTP memory) programming requires a 3.3V power supply to the device VDDQ pin, and feeding the data through the UART port, as shown in

Figure 16.

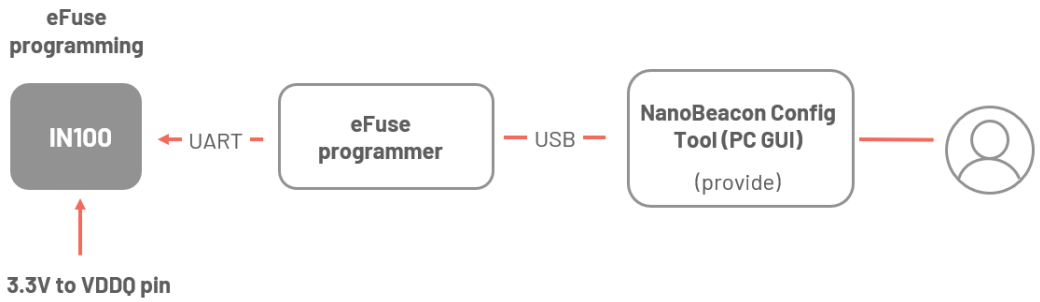


Figure 16 : eFuse memory programming process

4.12. Radio frequency sub-system

The device incorporates a 2.4GHz ISM frequency band radio and GFSK modulator capable of transmitting Bluetooth Low Energy 5 compliant advertising packets.

Table 13 : RF sub-system overview

Parameter	Description
Frequency band	2.4GHz ISM or medRadio-band
Data rate	125Kbps or 1Mbps
Power output	Maximum of +5dBm with adjustable settings

Parameter	Description
Output matching network	On-chip matching network

The 2.4GHz RF signal is transmitted through the RF_TX Pin as shown in *Figure 17*. An on-chip matching network has been implemented to minimize the number of external components. There is only one power supply pin (VCC) for the 2.4GHz transmitter, and an on-chip LDO brings that voltage level to the nominal 1.2V level used by the radio frequency sub-system. The transmitter needs a 26.0MHz crystal oscillator reference. To reduce BOM cost, the CL (the load capacitance) for the crystal is integrated on-chip. The on-chip CL can be programmed with registers from 0.5pF to 8pF in 0.5pF steps.

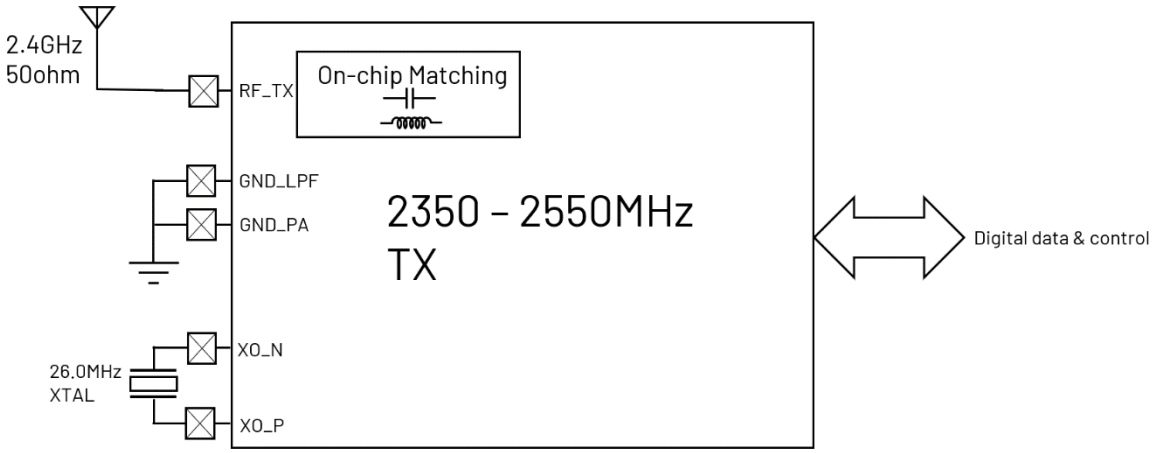


Figure 17 : RF sub-system interface

5. Electrical Characteristic

5.1. Absolute maximum ratings

The values listed in this section are ratings that can be tolerated for a short time by the device, but not sustained without causing irreparable damage to the device.

Table 14 : Absolute maximum ratings

Description	Comments	Min.	Max.	Unit
Supply voltage (VCC)		-0.3	3.9	V
Digital GPIO input	All digital GPIO pins	-0.3	VCC+0.3	V

Description	Comments	Min.	Max.	Unit
CHIP_EN pin		-0.3	VCC	V
Analog input	XO_N, XO_P, RTC_XO_N, RTC_XO_P, MGPIOs	-0.3	Min (2, VCC)	V
ESD HBM	All pins expect RF_TX pin	-4000	4000	V
	RF_TX	-2000	2000	V
Storage Temperature		-65	150	°C

5.2. Recommended operating conditions

Table 15 : Recommended operating conditions

Description	Min.	Typ.	Max.	Unit
VCC supply voltage	1.1	1.5	3.6	V
Operating temperature*	-40		125	°C

Note: for full range industrial grade product only. See ordering info chapter *10*.

The power sequence should follow the sequence as shown in *Figure 18*.

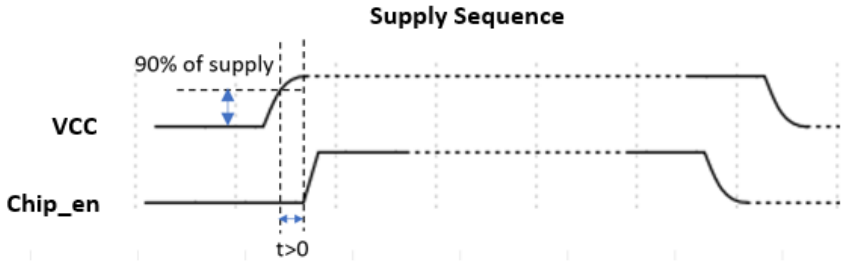


Figure 18 : Power supply sequence

5.3. GPIO characteristics

Performance below was measured at the following condition: Ta = 25°C, VCC = 3.0V, unless otherwise noted.

Table 16 : GPIO pin characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
VIL	Input low voltage			0.3*VCC	V
VIH	Input high voltage	0.7*VCC			V
VOL	Output low voltage			0.4	V
VOH	Output high voltage	VCC-0.4V			V
IOH	Output high drive current		4		mA
IOS	Output standard drive current		4		mA
tLH/tHL	Rising time/Falling time			4	ns
(standard drive)	@standard drive with 12pf load10%~90%				
RPU	GPIO pull-up resistance		25K		ohm
RPD	GPIO pull-down resistance		25K		ohm

Note: The data measured are preliminary and subject to change.

5.4. RF performance characteristics

Characteristics are measured over recommended operating conditions unless otherwise specified. The typical operation condition referred to is Ta = 25°C and VCC = 3.0V. The specifications are valid for -45°C ≤ TA ≤ +85°C and 1.1V ≤ VCC ≤ 3.6V. All performance data are measured via an evaluation board with a 50 ohm antenna connector.

5.4.1. General RF Characteristics

Table 17 : General RF characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Radio frequency range		2250		2550	MHz
RF PLL channel spacing	channel spacing is user programmable		1		MHz
Frequency modulation deviation	1Mbps BLE		±250		kHz

Parameter	Description	Min.	Typ.	Max.	Unit
Data rate		125		1000	kbps

5.4.2. RF transmitter performance characteristics

The performance below was measured at: Ta = 25°C, VCC=3.0V, f(RF)=2440MHz, unless otherwise noted.

Table 18 : RF Transmitter performance characteristics

Parameter	Condition	Test conditions	Min.	Typ.	Max.	Unit
Maximum output power		Averaged over band and build		5		dBm
Minimum output power				-50		dBm
Output power variation over band		2402MHz - 2480MHz	-0.5		0.5	dB
Output power build-to-build variation		Chip variation + matching component variation	-0.5		0.5	dB
In-band spurious emission	1Mbps, @ Pout,max	N +/- 2MHz		-54		dBm
		N +/- ≥3MHz		-44		dBm
Out-of-band spurious emission	@ Pout,max	f<1GHz, outside restricted bands		-50		dBm
		f<1GHz, restricted bands ETSI		-50		dBm
		f<1GHz, restricted bands FCC		-50		dBm
		f>1GHz, including harmonics		-44		dBm
		HD2		-44		dBm
		HD3		-61		dBm

5.5. System power consumption

Currents are measured at Ta = 25°C, VCC = 3.0V, unless otherwise noted.

Table 19 : System power consumption

Parameter	Description	Test conditions	Min.	Typ.	Max.	Unit
I_VCC	Current consumption	Chip disabled, CHIP_EN=0V		10		nA
		Sleep with 32kHz RC, sleep timer		0.625		uA
		2.4GHz TX mode - 1Mbps, Pout=0dBm		9.1		mA
		2.4GHz TX mode - 1Mbps, Pout=+5dBm (max)		13.8		mA

5.6. ESD characteristics (all pins)

The device passes all following ESD requirements.

HBM (human body model): Sensitivity pass +/-4500V, Class-3A (Reference ESDA/JEDEC JS-001-2017)

CDM (charge device model): TBA

6. Reference Design

6.1. IN100 QFN18 reference schematic

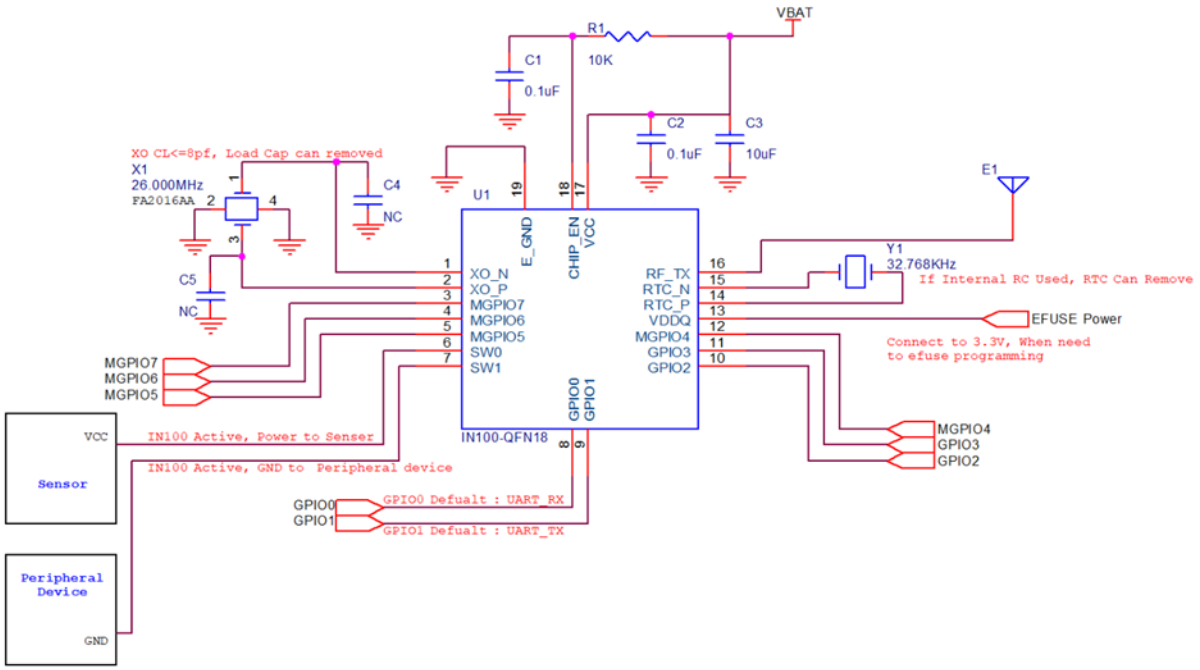


Figure 19 : IN100 QFN18 reference design

6.2. IN100 DFN8 reference schematic

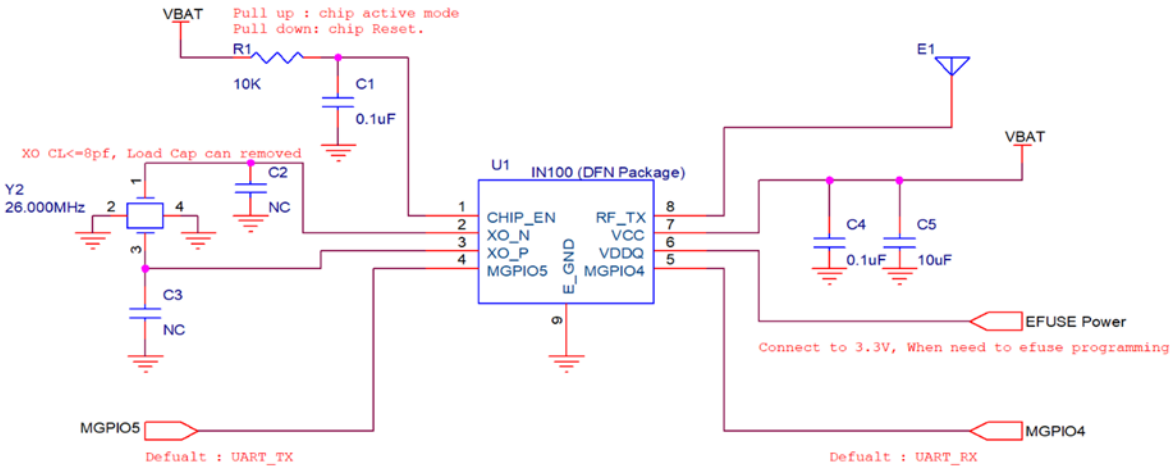


Figure 20 : IN100 DFN8 reference design

7. Layout

To ensure device performance, it is recommended to follow the general printed circuit board layout guidelines described below.

7.1. Layer stack-up

The recommendations in this document refer to the 2-layer standard flame retardant 4 (FR4) materials, a technology commonly used in commercial applications.

Table 20 : PCB layer stack-up

Layer	Purpose	Material	Thickness	Thickness control	Adjust to get desired total PCB thickness
Top layer +Plating	Signal	1/2 oz Cu	1.4	Yes	No
Dielectric		FR4	28.7	Yes	No
Bottom Layer + Plating	Signal/power	1/2 oz Cu	1.4	No	Yes
		Total thickness (mil)	32		

7.2. Crystal

7.2.1. 26MHz crystal

When there is a high-speed 26MHz crystal in the system, the parasitics associated with the clock trace affect the frequency of oscillation, so the crystal should be placed as close as possible to the device. Traces that are too wide can cause excessive capacitance, while traces that are too narrow can cause excessive parasitic inductance of the clock traces. For short clock traces, use a trace width of approximately 10 mils (0.010 inches or 0.254 mm). Keep the crystal tuning capacitor close to the crystal pad.

Avoid passing through the crystal lines on adjacent layers. Keep the ground plane below the crystal line to improve the return path. Try to keep the parasitic capacitances on both crystal lines equal. This can be done by keeping their lengths and widths equal.

7.2.2. 32.768kHz crystal

The slow clock signal line must be as short as possible. The trace of the slow clock signal should have a ground plane on each side of the signal trace to reduce unwanted signal coupling. In order

to reduce the capacitive coupling of unwanted signals to the clock line, the slow clock traces must not be crossed by other signals.

7.3. RF trace

Place the RF path on the top layer (component side) and keep the trace as short as possible. The RF trace must be immediately above a continuous ground on the next layer (Layer 2), The impedance of the RF trace must be controlled to 50 ohms by appropriate adjustment of the line width for the layer-to-layer separation and dielectric properties of the boards being used. In addition, ground vias are required for better RF isolation.

7.4. Antenna

The antenna is a key component in wireless system design to make sure the device will perform as expected. Make sure to select an antenna that covers the appropriate frequency band from 2.350GHz to 2.550GHz. Talk to the antenna supplier and make sure they understand that the antenna must cover the entire frequency range. Also make sure the antenna is designed for a 50Ω impedance system. Make sure the PCB pads to which the antenna is connected are properly designed to have a 50Ω impedance. The antenna supplier must specify the pad size, the pitch from the pad to the ground reference plane, and the spacing from the pad edge to the ground fill on the same layer as the pad. In addition, since the ground reference plane from the antenna pad to the 50Ω trace of the device may be on a different layer than the ground reference of the antenna pad, ensure that the pad design has an appropriate transition from pad to pad 50Ω trace.

7.5. Power supply

The DC supply voltage should be decoupled as close as possible to the VCC pin with high performance RF capacitors. Long power supply lines on the PCB should be avoided.

7.6. Thermal PAD vias

To increase the ground coupling, add at least 4 Vias directly from the DFN or QFN package paddle to the solid ground.

7.7. GND

In four or more layers PCB designs it is recommended to have a dedicated ground plane. In that case, make sure the ground plane is not broken by the routing of other signals. The power supply can be routed on all layers except the ground floor. The power path should be a heavy copper filled

plane to ensure the lowest possible resistive loss. For a PCB with a topside RF ground plane, the GND (exposed paddle) pins should be connected directly to the ground plane.

8. Reflow Profile Information

This section provides guidelines for reflow processes for soldering the device to the user's design.

8.1. Storage condition

8.1.1. Moisture barrier bag storage condition (sealed)

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product shall be 12 months from the date the bag is sealed.

8.1.2. Moisture barrier bag when opened

Humidity indicator cards must be blue, < 30%.

8.2. Stencil design

The recommended stencil is laser-cut, stainless-steel type with a thickness of 100µm to 130µm and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 25µm larger than the top can be utilized. Local manufacturing experience may find other combinations of stencil thickness and aperture size to get good results.

8.3. Baking conditions

This chip is rated at MSL level 3. After the sealed bag is opened, no baking is required within 168 hours so long as the devices are held at <= 30°C /60% RH or stored at <10% RH.

The chip will require baking before mounting if:

- The sealed bag has been open for > 168 hours OR.
- The Humidity Indicator Card reads >10%.

Chips need to be baked for 8 hours at 125 °C.

8.4. Soldering and reflow condition

8.4.1. Reflow oven

It is strongly recommended that a reflow oven equipped with multiple heating zones and Nitrogen atmosphere be used for lead-free assembly. A nitrogen atmosphere has shown to improve the

wettability of solder joints and reduce the temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

The following items should also be observed in the reflow process:

- Some recommended pastes include NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu or SENJU N705-GRN3360-K2-V Type 3, no clean paste.
- Allowable reflow soldering times: Three times based on the reflow soldering profile as shown in *Figure 21*.
- Temperature profile: Reflow soldering shall be done according to the temperature profile as shown in *Figure 21*.
- Peak temperature: 250°C.

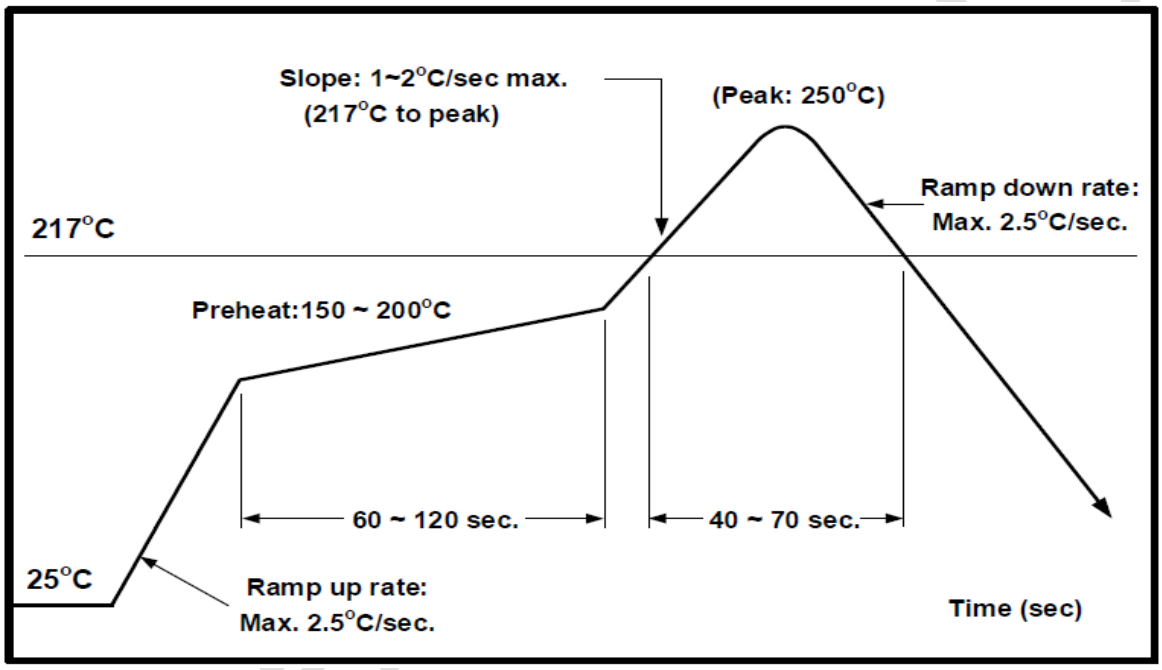
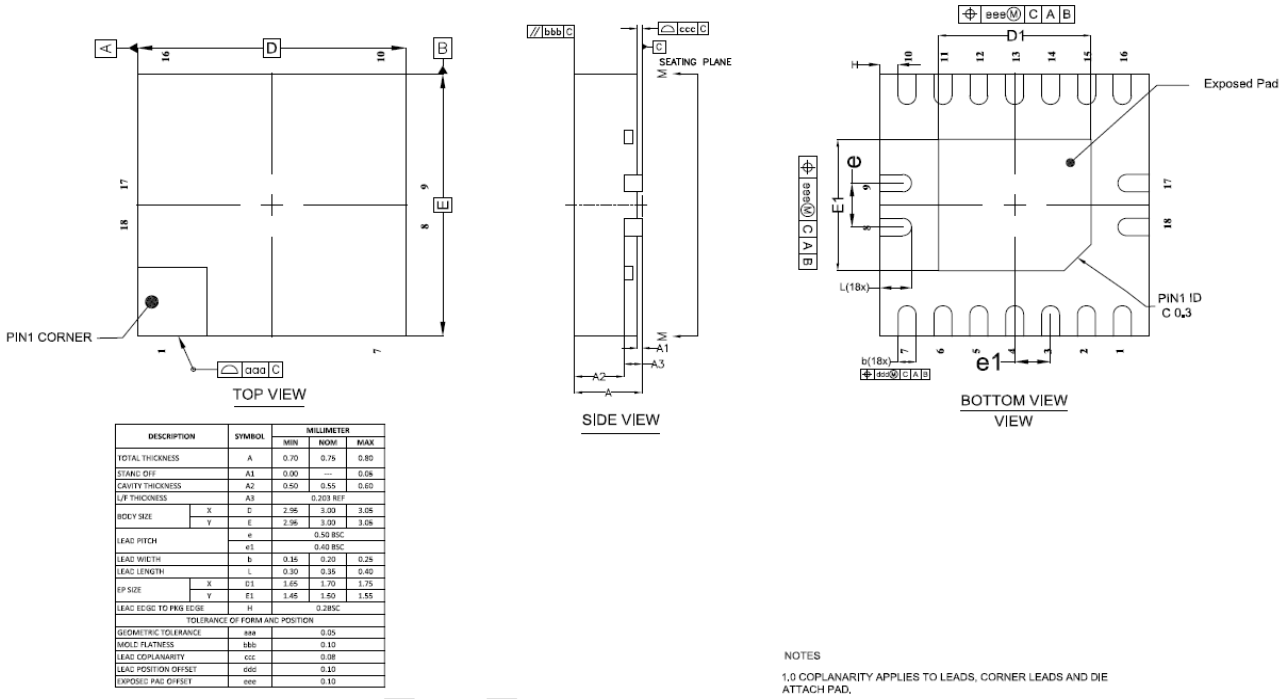


Figure 21 : Solder reflow profile

9. Package Dimension

The device is available in QFN18 and DFN8 packages. Both packages are RoHS/green compliant.

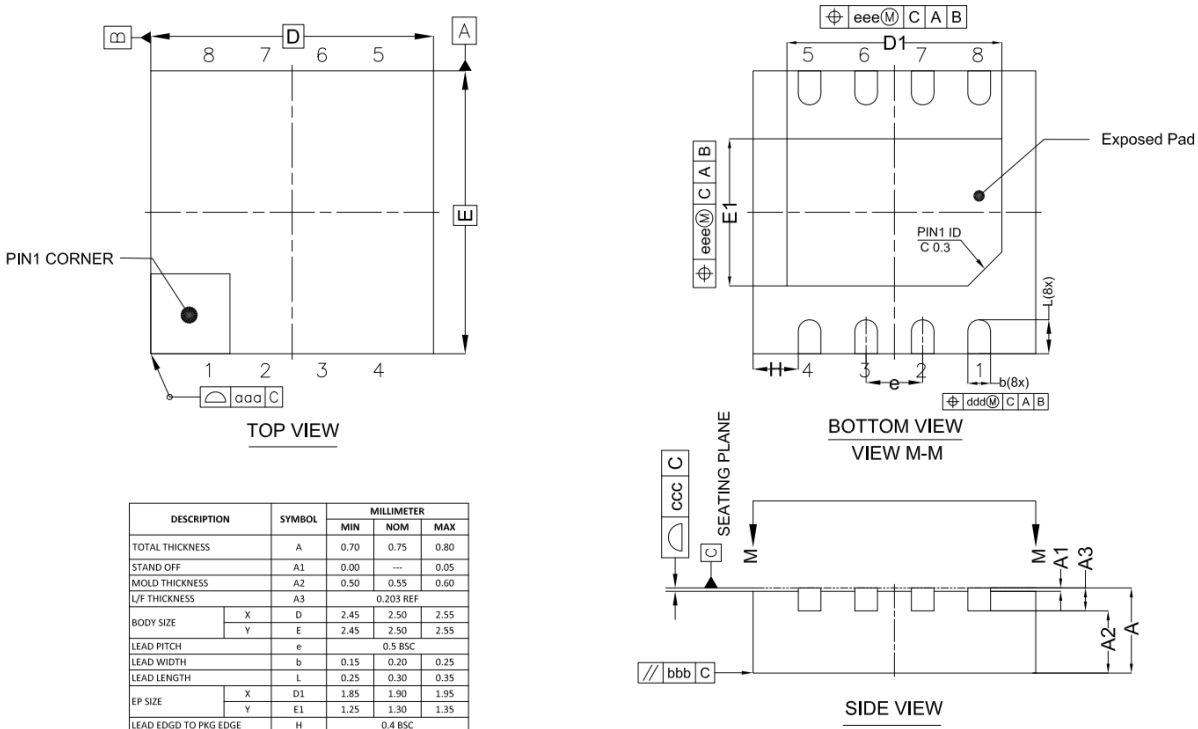
9.1. QFN18



DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0.00	---	0.05
CAVITY THICKNESS		A2	0.50	0.55	0.60
L/F THICKNESS		A3		0.203 REF	
BODY SIZE	X	D	2.95	3.00	3.05
	Y	E	2.95	3.00	3.05
LEAD PITCH		e		0.50 BSC	
		e1		0.40 BSC	
LEAD WIDTH		b	0.15	0.20	0.25
LEAD LENGTH		L	0.30	0.35	0.40
EP SIZE	X	D1	1.65	1.70	1.75
	Y	E1	1.45	1.50	1.55
LEAD EDGE TO PKG EDGE		H		0.285C	
TOLERANCE OF FORM AND POSITION					
GEOMETRIC TOLERANCE		aaa		0.05	
MOLD FLATNESS		bbb		0.10	
LEAD COPLANARITY		ccc		0.08	
LEAD POSITION OFFSET		ddd		0.10	
EXPOSED PAD OFFSET		eee		0.10	

Figure 22 : QFN18 POD

9.2. DFN8



DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0.00	---	0.05
MOLD THICKNESS		A2	0.50	0.55	0.60
L/F THICKNESS		A3	0.203 REF		
BODY SIZE	X	D	2.45	2.50	2.55
	Y	E	2.45	2.50	2.55
LEAD PITCH		e	0.5 BSC		
LEAD WIDTH		b	0.15	0.20	0.25
LEAD LENGTH		L	0.25	0.30	0.35
EP SIZE	X	D1	1.85	1.90	1.95
	Y	E1	1.25	1.30	1.35
LEAD EDGD TO PKG EDGE		H	0.4 BSC		
TOLERANCE OF FORM AND POSITION					
GEOMETRIC TOLERANCE		aaa	0.05		
MOLD FLATNESS		bbb	0.10		
LEAD COPLANARITY		ccc	0.08		
LEAD POSITION OFFSET		ddd	0.10		
EXPOSED PAD OFFSET		eee	0.10		

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 23 : DFN8 POD

9.3. IC marking

The device IC is marked like described below.

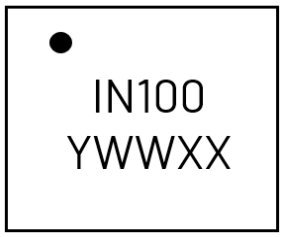


Figure 25 : DFN8 marking

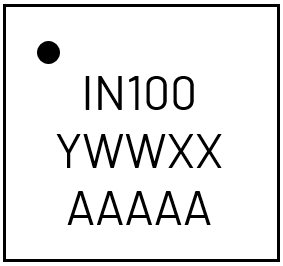


Figure 24 : QFN18 marking

Table 21 : IN100 marking description

Abbreviation	Definition and implemented codes
IN1	INPLAY NanoBeacon™ SoC product family name
00	Part number code
AAAAAA	Factory control code
XX	Chip version & temp code
Y	Year code
WW	Week code

10. Ordering Information

Contains information on IC marking, ordering codes, and package sizes.

Table 22 : Ordering information

Ordering part number	Package
IN100-D1-R-RC1I	DFN8 (-40°C ~ +85°C)
IN100-Q1-R-RC1I	QFN18 (-40°C ~ +85°C)
IN100-D1-R-RC1F	DFN8 (-40°C ~ +125°C)
IN100-Q1-R-RC1F	QFN18 (-40°C ~ +125°C)

10.1. Box package dimension

Defined here are the device package size for reel, inner box and outer box.

Table 23 : Size for reel inner box and outer box

Package	Reel size	QTY / Reel	QTY / Inner box	QTY / Outer box
QFN	13"	5,000	5,000	50,000
DFN	13"	5,000	5,000	50,000

11. Revision History

Revision	Description	Date	Drafted by
V1.0	Initial version	1/18/2022	

12. Disclaimer

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