ACCELERATING SEMICONDUCTOR RESEARCH, ACCELERATING AMERICA:

Bringing the Best Research and Development to The National Semiconductor Technology Center and The National Advanced Packaging Manufacturing Program

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Executive Summary

The 2021 National Defense Authorization Act's call to create a National Semiconductor Technology Center (NSTC) and a (NAPMP) recognizes the need for swift action to strengthen U.S. semiconductor leadership in the face of rising global competition.

To protect U.S. semiconductor leadership, manufacturing continually fueled by world-leading research and development is key. In this document, a broad coalition of industries, universities, consortia, national labs, and nonprofits offers a vision of a technology network, with hubs and geographically distributed centers of excellence, as the main technical driver of NSTC and NAPMP, supporting the research, development, prototyping and manufacturing transfer goals of the NSTC and NAPMP and ensuring they are met.

To reach that objective, the technology network must achieve the following:

- Provide an innovation ecosystem for research, development and prototyping with first-class resources, scientists, facilities, and partners who can work quickly and efficiently to demonstrate and transfer breakthrough technology to manufacturing to secure a strong domestic chip supply chain for the future.
- Create and execute on an ambitious, but practical, technical agenda focused on the transition from innovation to commercialization.
- Include teams experienced in taking discovery from "lab-to-fab."
- Expand existing large piloting and prototype integration centers to leverage prior investment and hit the ground running on day one.
- Upgrade the infrastructure and programs at key universities, reducing the time for tech transfer and facilitating workforce investment.
- Facilitate start-ups with access to prototyping facilities provided by the network.

The network must be held accountable for reaching clear and measurable goals. In reaching its objective, it will accelerate the American semiconductor industry.

Introduction and Context

A nationwide partnership to accelerate American semiconductor research, development, prototyping, and transfer to manufacturing will drive America's growth and is essential to safeguard U.S. global competitiveness and security.

Semiconductors are part of the backbone of modern life. The ongoing shortage is disrupting supply chains, impacting consumers and businesses, and threatening national security. It exposes the lack of sustained domestic investment in the semiconductor industry and highlights the need for the U.S. to reinvest to guarantee a steady supply of chips and world leadership in chip research and development.

The 2021 National Defense Authorization Act's (NDAA) call to create a National Semiconductor Technology Center (NSTC) and a National Advanced Packaging Manufacturing Program (NAPMP) establishes a pathway for this urgent investment. It will uniquely accelerate the U.S. transformation into a secure semiconductor powerhouse. Although much has been said about the impact this investment can have on manufacturing, America's semiconductor industry will need to be continually refreshed by world-leading research and development, as the Act recognizes. That research and development is the focus of this vision.

The NSTC is envisioned as a public-private partnership to conduct research, development and prototyping of advanced semiconductors, support startups and small businesses, and provide workforce training programs. It can serve as a hub to marshal semiconductor expertise and resources to deliver breakthroughs in chip innovation and production.

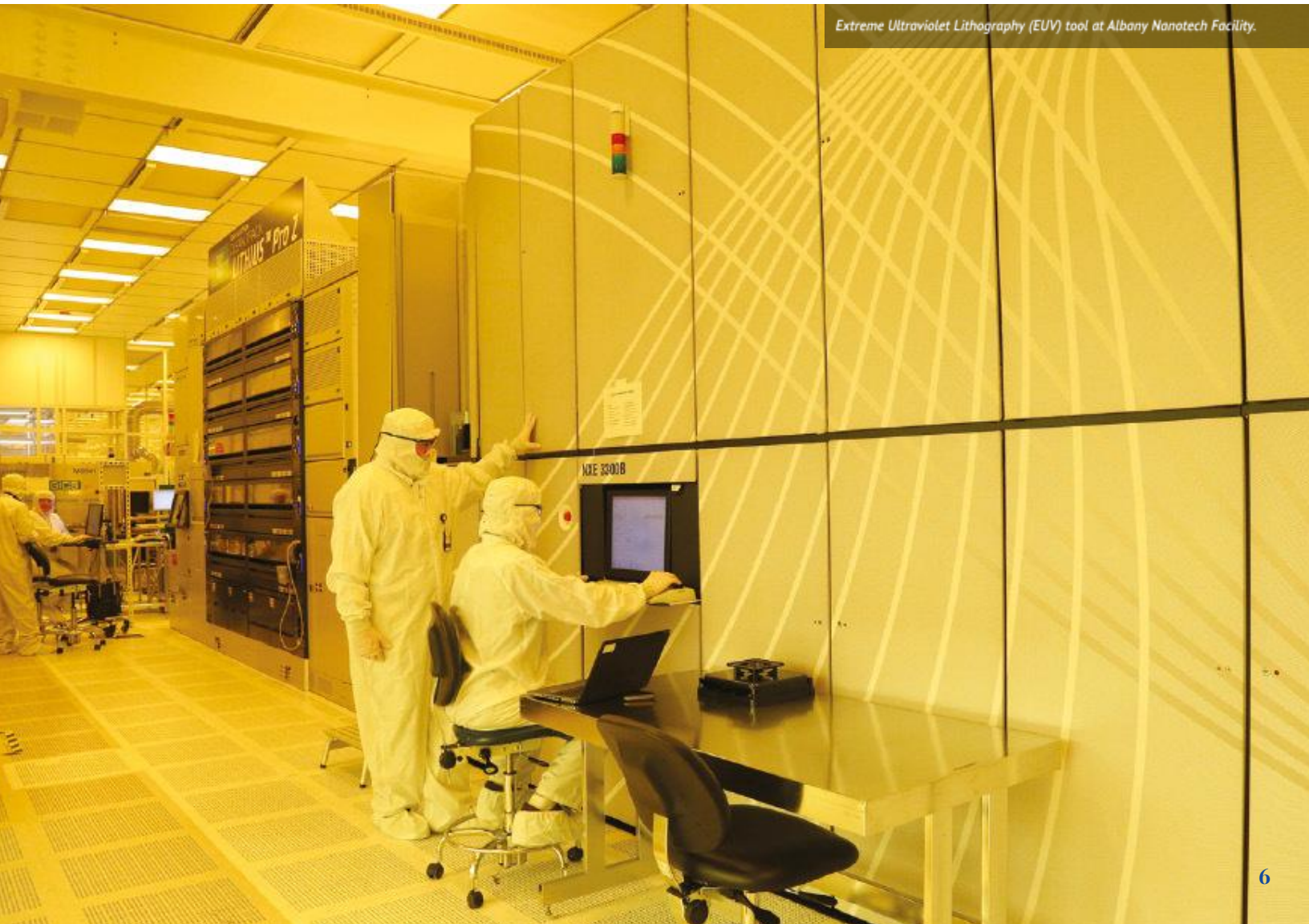
The NAPMP is intended to focus on embedding and combining chips into dense configurations that combine multiple functions resulting in benefits including lower costs, increased functionality, and improved energy efficiency. Packaging is the innovation engine that will drive next generation microelectronics, and chip-package co-optimization creates additional value and technology differentiation. Packaging requires many of the same tools, materials, infrastructure, and talent used for making chips. Co-location of NAPMP and NSTC technical activity will accelerate innovation across the full technology stack.

For the NSTC and NAPMP to meet the challenge, they must have at the core a technical group to lead and execute the research and development mission. We envision a technology network including leading companies, universities, consortia, and national labs. This network can provide a unique innovation ecosystem for the NSTC and the NAPMP that is "prototype ready" with first-class resources, scientists, facilities, and partners who can work quickly and efficiently to secure a strong domestic chip supply chain for the future.

The technology network will work with the Departments of Commerce, Defense, and Energy in support of the agenda laid out in the NDAA, including related programs such as metrology R&D at the National Institute of Standards and Technology (NIST). The overall governance of the NSTC, which in addition to the technology network's focus on research, development, prototyping, and transfer to manufacturing, will include a startup investment fund and broad-based workforce development programs, should be determined in consultation with government and other stakeholders.

The network must include teams with experience in taking discoveries from "lab-to-fab." It also must expand existing large piloting and prototype integration centers - leveraging prior investment - since entirely new centers would take years to become fully-operational – too late to impact the current battle. The network must also facilitate upgrading the infrastructure and programs at key universities, reducing the time for tech transfer and promoting workforce investment. Finally, start-ups need access to prototyping facilities provided by the network. Today, they lack the ability to rapidly prototype, creating an innovation and fairness gap.

By creating such a technology network the U.S. can reach its goals, and swiftly, as there is no time to waste.



Extreme Ultraviolet Lithography (EUV) tool at Albany Nanotech Facility.

Our Perspective

The success of the NSTC and NAPMP calls for accelerating the development and transfer to manufacturing of advanced semiconductor technology. This requires a technology network led by industry in close collaboration with government and academia. It needs a nationwide footprint orchestrated from hubs. These hubs, through which the activities of the technology network will be coordinated, should not serve the interests of a narrow set of actors but rather should meet the following criteria:

- **Proven Chip Innovation Results**
  This challenge calls for the leaders in semiconductor chip innovation ecosystems to orchestrate the R&D response. It requires a sophisticated infrastructure that is already operational and backed by partner companies, academic institutions, and a highly skilled workforce. It should have a history of leveraging its ecosystem to produce leading-edge semiconductor innovations.
- **Expansive Partnerships**
  Success will result from partnerships with universities and academic institutions across state borders, and at times across national borders (with like-minded nations). This structure strengthens the semiconductor R&D pipeline, cultivates a diverse and talented semiconductor workforce, and translates technology into tangible business and consumer solutions.
- **State-of-the-art Facility**
  Hubs should be in advanced, publicly-owned, R&D facilities in the U.S. where global leaders collaborate currently with engineers and scientists on technological breakthroughs.
- **Transfer-to-manufacturing Expertise**
  Hubs should have a proven chip innovation ecosystem and be placed in facilities with advanced tools and support, capable of continually moving new chip designs to production, ensuring collaboration on advanced semiconductor R&D, and meeting the full spectrum of U.S. economic and national security needs. Access to hubs and the network should be available to a national set of partner companies, universities, workforce partners, and startups to create a true national innovation capability and broad technical roadmap to drive innovation across the entire semiconductor supply chain.

Addressing a Vital Problem for R&D Competitiveness

The Problem Statement

U.S. leadership in semiconductor research and development is threatened by global competition and requires speed and expertise to meet the challenge.

The Critical Need to Avoid Delays

America faces growing competition in the semiconductor industry. In 1990, the U.S. produced 37% of the world's semiconductors, compared to 12% today.[1] An integrated global supply chain that had served industry now faces major disruptions fueled by geopolitical tensions and the pandemic.[1] The impact of these disruptions is wide – Americans are struggling to buy devices run by semiconductors and to ensure current levels of global competitiveness.

A change in approach is essential. While U.S. private investment in semiconductor R&D as a percentage of GDP has increased nearly 10-fold in the last 40 years, federal investment has been flat, creating a risk to continued U.S. innovation.

In comparison, in the last 20 years China has been closing the gap with the U.S. on R&D spending.[1] The *Made in China 2025 Plan* sets goals to achieve 70% self-sufficiency in semiconductors by 2025. The EU[2], Japan[3], and India are also making investments of tens of billions of dollars in semiconductor strategies. For example, in December India announced a $10 billion plan to attract semiconductor and display manufacturers as part of its efforts to become a global electronics production hub[4].

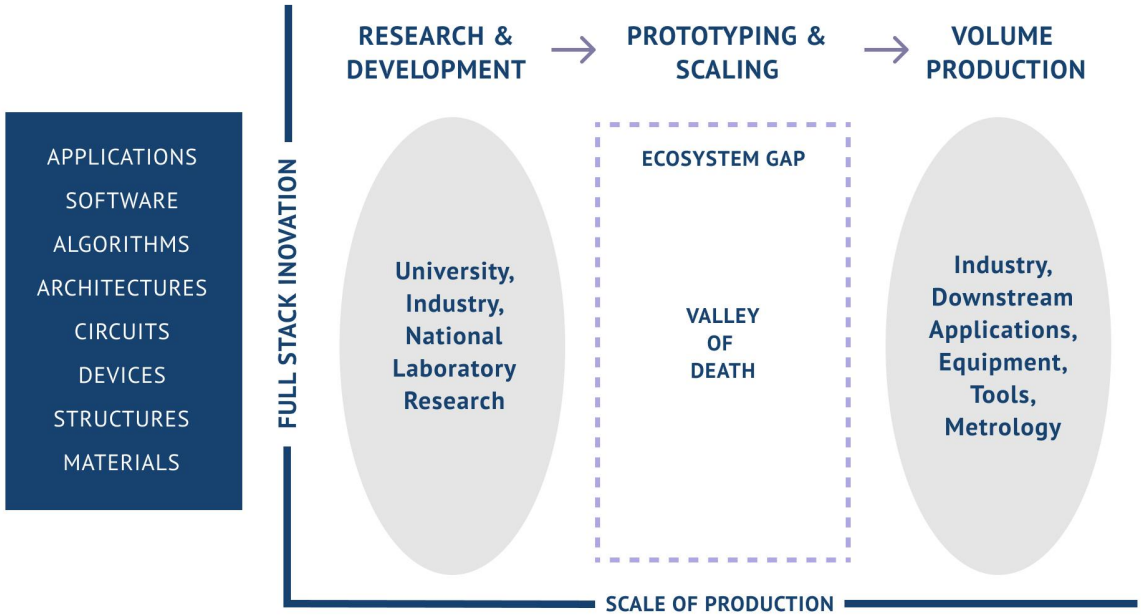
The ongoing chip shortage exposes the lack of sufficient U.S. investment in the semiconductor industry and the need for a new approach. The time for America to act is now, but with an accelerant – existing ecosystems and facilities. The U.S. must not waste precious time and resources.

Packaging Reliability testing Lab at Albany Nanotech complex.

The Difficulty in Bridging the "Valley of Death"

In the U.S. the ability to integrate systems, prototype, scale, and commercialize microelectronics innovations from "lab-to-fab" is hampered by a "Valley of Death" that is driven by a funding and resources gap. [7] In a recent announcement on hypersonics research, the U.S. Department of Defense (DOD) stated that the issue "plagues program development" and pointed to the need for the ecosystem to "help us figure out how to better move technologies from the laboratory to operational systems.[5]

The NSTC and NAPMP can address this critical gap by conducting research, development and prototyping in semiconductor manufacturing, packaging, and design, and prototyping that strengthens the entire domestic ecosystem and is aligned with the National Strategy on Semiconductor Research called for in section 9906a of the 2021 NDAA.



Valley of Death[6]

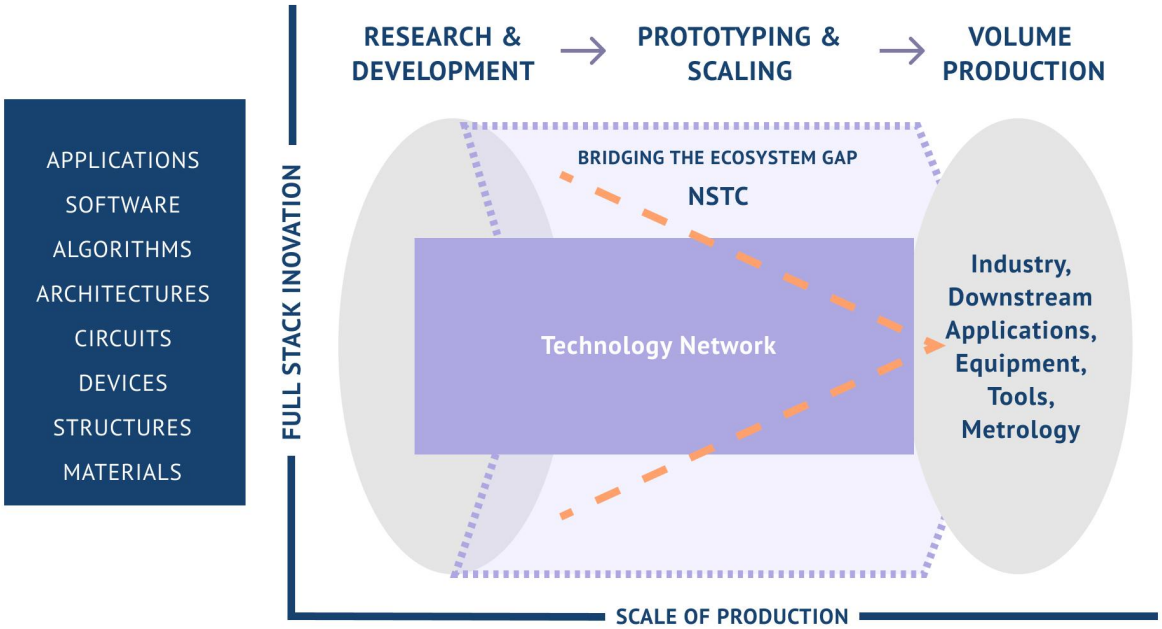
The Complexity of Coordinating "Full Stack" Innovation

For the full potential of future technologies to be reached, coordination across the "full-stack" must be orchestrated at the research and development stage. "Full-stack" refers to a semiconductor chip from the materials and devices (e.g. transistors) to packaging and interfaces (which connect chips to each other and to the outside world), and the design and software tools that are used to design chips and allow them to function. Currently, most entities in the U.S. semiconductor ecosystem focus on a subset of the stack with no coordinating entity. This hampers the ability to commercialize and scale innovations.

Providing World-Leading Semiconductor Technologies

The Value Proposition

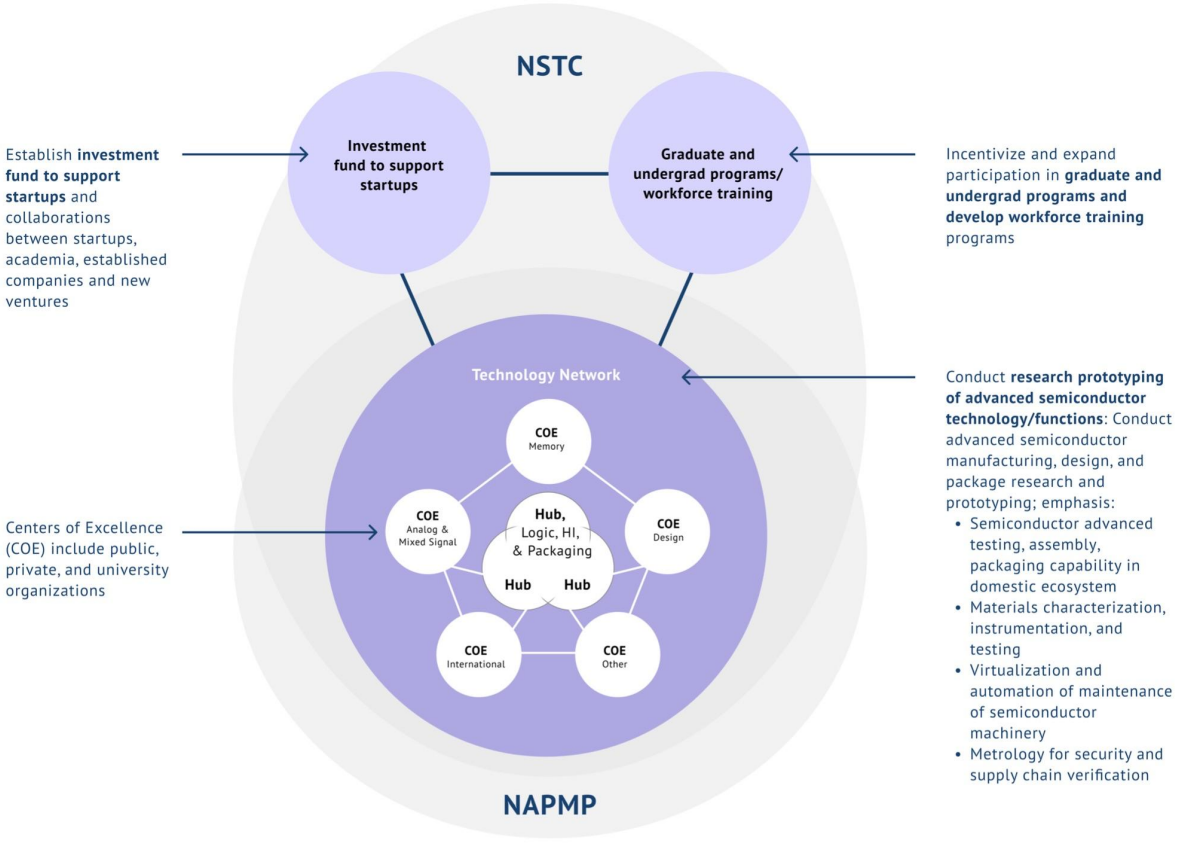
U.S. semiconductor leadership can be secured by ensuring the NSTC and NAPMP achieves their goals, which must be enabled by a technology network, with a nationwide footprint, orchestrated from hubs.



Bridging the Gap[7]

Creating the Technology Network

The technology network will be responsible for creating, coordinating and executing on a strong technical agenda that accelerates and enables the wider goal of the 2021 NDAA – U.S. semiconductor and advanced packaging leadership. This can be accomplished through proven chip innovation results, expansive partnerships, leveraging state-of-the-art facilities and transfer-to-manufacturing expertise.



Potential Structure of the Technology Network

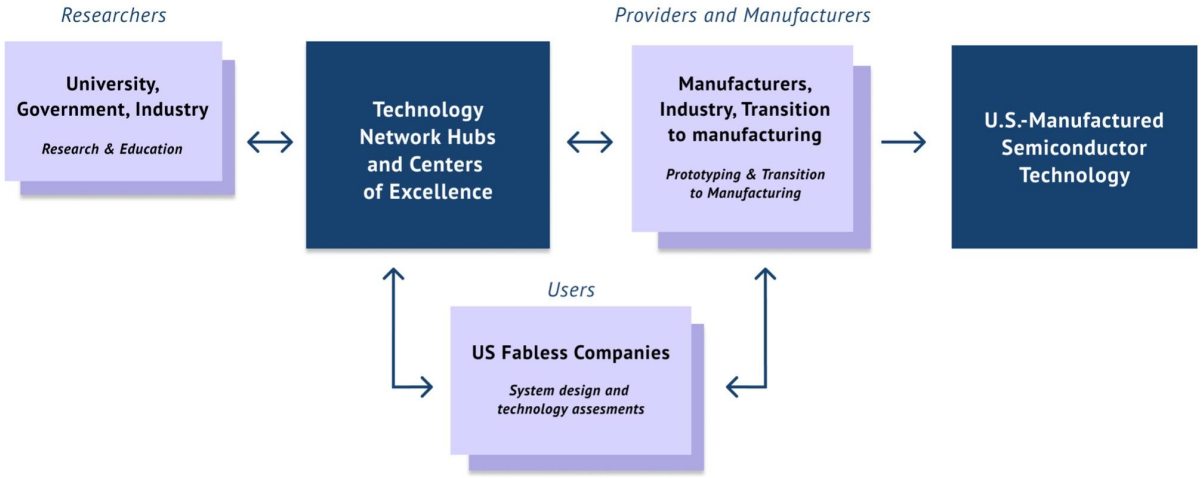
Technology Network Principles
• Coalition of industry, academia, and government (including national labs) • Start with the best U.S. semiconductor facilities and expertise, ensure ability to expand lab-to-fab capability • Robust governance model with member and U.S. government input • Coordinated NSTC member technical agenda and roadmaps (including adjacent spaces,e.g., photonics) • Coordination with related U.S. government programs • Facilitate easy access to NSTC capabilities to universities and small businesses • Select international participation of like-minded nations • Accessible IP for prototyping and piloting for semiconductor ecosystem • Core centers across the U.S. where the best physical and human resources exist • Robust education and workforce development across semiconductor ecosystem • Facilitate the maturation of technology and the subsequent translation to corporate R&D laboratories and manufacturing

Technology Network – Structure

The NSTC/ NAPMP technology network should include a wide variety of stakeholders engaged in semiconductor research, development, and manufacturing through hubs and "centers of excellence." Stakeholders will likely include:

- **Researchers** (university, government (including national labs), and industry) to collaborate in developing new technologies, to ensure "lab-to-fab" transfer.
- **Providers** (producers of materials and semiconductor design, manufacturing, and test equipment or software) to integrate new technologies into their commercial offerings.
- **Users** (IP developers, fabless companies, and system developers) collaborate in assessment of new technology tools, features, and architectures, and drive the technology development toward offerings that they can adopt for their products.
- **Manufacturers** (companies that manufacture semiconductor chips and associated technology) to scale the new technology to commercial production.

The network can provide managed infrastructure and governance, through the hubs, where stakeholders communicate and collaborate to define and drive a common technical agenda. Drawing on a pipeline of research innovations, the manufacturing capabilities of the U.S. can be strengthened through continuous feedback from the companies whose products are prototyped and manufactured in this ecosystem.



Technology Network Stakeholders and Activity Flow

The Role of Academia

An integral part of the technology network must be an academic component that will have the dual mission of education and advancing the R&D technology pipeline into the NSTC and NAPMP agenda. This is necessary to strengthen the "lab-to-fab" pathway which will accelerate the transition of viable technologies with a 5-10-year horizon to 300mm development and high-volume manufacturing—driving U.S. innovation and differentiation in chip manufacturing and packaging. The work with academia should be designed to access talent from the broadest range of institutions across the nation including Historically Black Colleges and Universities (HBCUs), other minority-serving institutions (MSIs), 4-year colleges, community colleges, and integrated high school to college programs (e.g. P-TECH).[8] Educating the workforce on the latest advances in design, new materials, devices, and packaging, and rapidly modernizing this training to stay ahead of the changing nature of jobs in this industry will be crucial for sustained long-term success. Students and professors, working with industry professionals in university labs, national labs, and NSTC/NAPMP facilities will have the opportunity to prototype and drive new technologies into commercial offerings, including by transitioning to the commercial workforce and/or seeking start-up investment funds. The role of academia in the technology network includes:

Education and workforce development

- Create a nationwide university, industry, and government program to develop and rapidly adopt educational content
- Invest in and support the maintenance of education and training facilities that are accessible to a broad range of institutions
- Create nationwide fellowship and internship programs for in-class and on-the-job education and training

Research

- Establish research programs to advance the NSTC and NAPMP agenda that foster a broad range of research, from fundamental to industry and national-security oriented programs, from single-investigator to multi-disciplinary and multi-institution programs

Technology translation, startups, and intellectual property

- Develop programs to facilitate the maturation of technology in appropriate university environments and the subsequent translation to external manufacturers and corporate R&D laboratories
- Create programs to support the generation and nurturing of microelectronics startups
- Establish translational fellows' programs to support graduate students and postdocs as they pursue the launch of startups

Infrastructure

- Make investments in updating design, fabrication, and metrology capabilities in university research facilities and make NSTC facilities available to university researchers.
- Ensure broad-based access to advanced technology processing equipment for on-the-job training

Regional networks

- Foster regional networks to leverage local resources and employers to create research programs, educational programs, startup support, outreach, and internship programs. [9]

Technology Network – Process

The Marketplace

A Marketplace would facilitate use of the NTSC design and prototyping capability by providing access to fabrication facilities, design tools and IP, cloud compute infrastructure, and top design and foundry technology experts to assist users in developing prototypes. It is a concept structure for allowing collaborative design and access-controlled IP and tools through a web-based user interface. This is a one-stop-shop where users can obtain, or exchange, value such as IP, tools, flows, MPWs, and human effort, and maintain a history of all transactions. Built on a cloud-based secure design platform, it would include best-in-class designs, tools and techniques, scoring these offerings in terms of quality, compatibility, and security. The Marketplace would support program-subsidized and customer direct-pay business models as methods to access offerings. Either direct revenue or subsidized support would be available to start-ups and academia. Training, internships, and other educational support would be part of the Marketplace. Through this structure, companies can be incentivized to participate in the wider NSTC and value will not be captured by a single entity. This method of engagement can also provide a sustainability model for the NSTC as government support tapers off.

Hubs

As a proven world leader in semiconductor chip innovation ecosystems, New York can be a critical part of the network and should serve as a major hub of the NSTC and NAPMP technology network.

As Senator Chuck Schumer[10] stated and New York Governor Kathy Hochul[11] recently wrote, to succeed, the NSTC needs a proven chip innovation ecosystem like the one in New York, which has a sophisticated infrastructure that is already operational and backed by partner companies, academic institutions, and a highly-skilled workforce. Albany Nanotech, which is part of the New York semiconductor ecosystem, is the product of billions of dollars in public and private investment over two decades and hosts more than 2,700 industry experts, staff, students, and faculty who have leveraged the complex to produce leading edge semiconductor innovations such as the world's first 2 nanometer node chip technology and VTFET design demonstration prototype. It is poised to host a major hub of the technology network.

Case Study: Vertical Transport Field Effect Transistor (VTFET) Design Demonstration Prototype

Developed by a joint team of researchers at the Albany Nanotech complex, IBM and Samsung Electronics jointly announced a breakthrough that defies conventional semiconductor design and aims to reduce the energy usage of chips by 85% or double performance compared to scaled finFET transistors. The new VTFET design prototype successfully implements transistors built vertically on the surface of a chip. Because transistors have, until now, been built horizontally to lie flat upon the surface of a semiconductor, this allows a greater number of transistors to exist on a chip and removes density and energy efficiency constraints. The VTFET process addresses many barriers to performance and limitations to extend Moore's Law as chip designers attempt to pack more transistors into a fixed space. It also influences the contact points for the transistors, allowing for greater current flow with less wasted energy.[12]

Successes like these do not result from serving narrow interests. Instead, they are the result of partnerships across borders and with universities and academic institutions, including the State University of New York, Rensselaer Polytechnic Institute, and the Massachusetts Institute of Technology. These partnerships strengthen the semiconductor R&D pipeline, cultivate a diverse and talented semiconductor workforce, and translate technology into tangible business and consumer solutions.

New York has been preparing to meet this moment for decades. Funded by $15 billion in public and private investment over two decades, Albany Nanotech is the most advanced publicly owned 300-millimeter semiconductor R&D facility in North America. Global industry leaders collaborate every day with state engineers and scientists on technological breakthroughs at this location.

Case Study: Scalable Model for Networked Lab-to-Fab Collaboration

In 2019, Applied Materials opened the Materials Engineering Technology Accelerator (META) Center at the Albany Nanotech Complex, aimed at speeding prototyping of new materials, process equipment technology and devices. The public-private partnership between Applied Materials and NY CREATES brought online 20,000 square feet of cleanroom, providing customers and partners access to state-of-the-art process systems to shorten the time from lab-to-fab. The public-private partnership also established a co-investment initiative with Empire State Development (ESD), New York State's economic development organization, providing an opportunity for startups and early-stage companies to benefit from capabilities at the META Center, and a joint research program with the entire SUNY system.

META functions as a key node in Applied's nationwide R&D environment, offering access to EUV lithography, well-established baseline process flows and a comprehensive set of Applied's advanced process systems in a robust pilot manufacturing environment. The company leverages these investments and capabilities in New York to drive complementary research across its network of other key R&D facilities in Silicon Valley, Arizona, Massachusetts, Montana and Texas, as well as joint work with customers, startups and universities nationwide. These include leading-edge innovations in Logic CMOS to enable scaling beyond 3nm and advanced 3D DRAM memory, as well as next-generation neuromorphic devices for Edge computing, partly in support of DARPA's Electronics Resurgence Initiative. Taken together, these elements demonstrate a scalable model for lab-to-fab collaboration across a nationwide network, and a novel playbook for industry innovation and collaboration, from materials to systems.

For the NSTC to be effective quickly, the technology network hubs must rely on proven chip innovation ecosystems and be placed in environments capable of continually moving new chip designs to production, ensuring collaboration on advanced semiconductor R&D, and meeting the full spectrum of U.S. economic and national security needs. Albany Nanotech, operated by NY CREATES, is just such an ecosystem. It has fostered a public-private partnership with the state of New York and equipment, materials, and manufacturing companies to achieve technological breakthroughs that are shaping the next generation of semiconductor innovation.

Through sustained investments and a collaborative R&D ecosystem approach, scientists at Albany Nanotech push the boundaries of semiconductor technology. For example, Albany Nanotech pioneered work in cutting-edge technologies such as extreme ultraviolet lithography (EUV), the key patterning technology enabling sub-7nm semiconductor chips, and is the only facility in the U.S. conducting collaborative research on EUV. The Albany Nanotech ecosystem has continued to be the hub of innovations for semiconductor chips, including first demonstrations of novel device architectures such as nanosheet.[13]

These advancements will have a direct impact on businesses, consumers, and national security. For instance, the latest 2 nanometer node chip built at Albany Nanotech in 2021 is projected to enable 45% performance improvement over today's 7nm chip using the same amount of power. Alternatively, it is projected to provide 75% power savings at the same performance level. This could translate to a longer cell phone battery life and a significant reduction in the carbon footprint of data centers.[14]

In addition, in the past half decade, Albany Nanotech has made significant inroads in setting up state of the art 14nm Magnetic Random Access Memory (MRAM) technology[15] and 14nm analog in-memory compute technology for AI applications[16] and made investments to enable a world-class micro-bump facility. This work has delivered significant progress in new heterogeneous integration techniques like advanced silicon bridges, ultra-dense substrate innovations and through silicon via (TSV)-enabled 3-D Integration technologies. This has resulted in Albany Nanotech being well positioned to lead the way for national research in Heterogeneous Integration and "More than Moore'' technologies.

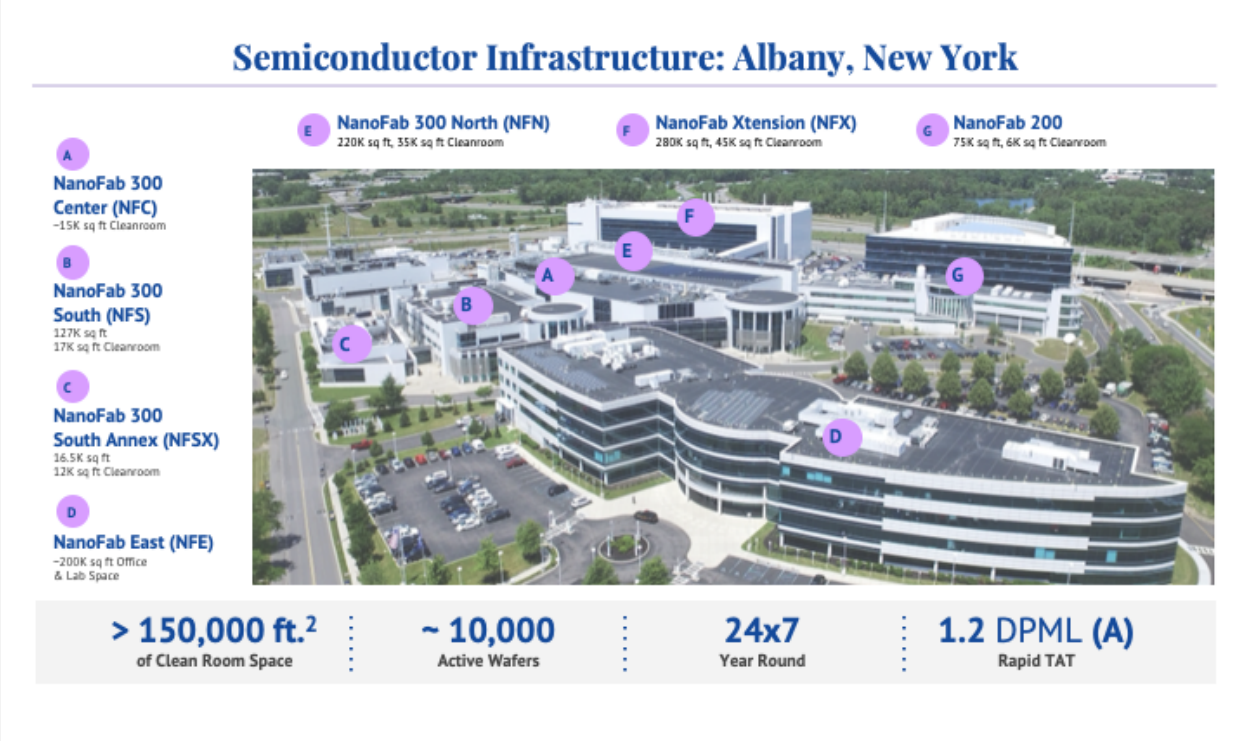
NY CREATES also benefits from a wide breadth of academic partnerships which translate into access to some of the best research centers and experts in the world. These wide and unique partnerships with academic institutions — not just in New York, but around the country — are invaluable to augmenting the research and development pipeline and promoting a diverse and talented semiconductor workforce. Critically, by leveraging this proven ecosystem, the hub of the NSTC could be operational on day one and be fully operational in a matter of months.

300mm Cleanroom at NFX building at Albany Nanotech complex.

NYCREATES

About NY CREATES

A New York State not-for-profit entity with a world leading state-of-the-art prototyping facility at Albany Nanotech, the New York Center for Research, Economic Advancement, Technology, Engineering and Science (NY CREATES) has end-to-end advanced fabrication capabilities as well as flexible infrastructure which can support innovative prototypes. It supports multiple advanced 300mm microelectronics research fabs, which house research centers for the top semiconductor equipment makers and chip researchers, in addition to the new 300mm based test, assembly, and packaging facility. NY CREATES' predecessors date back to 1993 and its history is filled with successful technological collaborations, innovations, prototypes, and development of customer programs. What is clear from this historical perspective is a pattern of continued investment from New York State, the U.S. government, and very strong industrial partnerships. State, federal, and industrial partners have invested over $15B to stand up and continuously update the world's most advanced semiconductor research center.



Strengthening the Ecosystem

The technology network can be tasked with expanding the semiconductor research and development ecosystem in the U.S. By placing a major hub in New York, it can expand rapidly in fertile ground.

In addition to The State University of New York (SUNY) and the industrial partners already engaged in the Albany Nanotech Complex, the New York region and the northeastern U.S. are home to several other organizations which are or can be engaged in this hub. These include Brookhaven National Lab, MIT, Cornell, Rochester Institute of Technology, Rensselaer Polytechnic Institute (RPI), the Air Force Research Laboratory in Rome, NY, and IBM's Bromont facility for advanced packaging in Canada, all of which bring capabilities that are critical to the mission.

Creating Workforce Impact

Semiconductor ecosystems are driven by the diverse and constantly evolving talents of American workers. The NSTC and NAPMP should be a force for inclusive, well-paying jobs across the U.S., with a continuing effort to diversify its workforce, leveraging support for veterans and underrepresented professionals and students, including women and people of color. The technology network can support this mission by collaborating with K-12 schools, universities, community colleges, vocational schools, and industry to build the skills that will prepare them to join the semiconductor workforce and thereby contribute to the next generations of semiconductor technologies. We recognize that solving the semiconductor workforce shortage requires coordinated cross-agency and cross-industry efforts, which the network cannot do alone. The following activities would support workforce development in the semiconductor industry:

- **Establish apprenticeship programs and work with the government to reduce obstacles to use apprentices on federal contracts.** Building stronger ties between academia (including community colleges and vocational schools), industry, and government to establish apprenticeship training models that will prepare the students to join the workforce. This partnership is needed to develop industry-led apprenticeships with sufficient flexibility to adjust to the rapidly changing advanced technologies driven by the semiconductor industry. Apprenticeship and on-the-job training will proactively address skills gaps and accelerate the students' ability to contribute at a higher level of productivity from the start. In the short term, these programs will reduce the barrier to entry for workers not trained in the semiconductor industry and offer a hands-on demonstration of the important contributions that can be made towards the next generation of computing.

- **Build a semiconductor partnership network.** Focus on partnerships with academia (K-12, community colleges, vocational schools, minority serving institutions, universities) and industry across the United States to create more STEM education opportunities as they relate to advanced semiconductor technology over the next 5-10 years including expansion and exchange of education and skills-based credentials to empower learners with trusted skills-based information and align their skills to in-demand jobs. An example of such a partnership has been the Semiconductor Research Corporation (SRC), a consortium including industry and the Department of Defense, to partner with and fund basic research in areas critical to the semiconductor industry. This enables the research agendas at universities to be informed by industry, so that teaching can be directed toward real industry problems. In addition to important technological advances, this program has helped train the next generation of semiconductor innovators. These types of partnerships need to be expanded and multiplied across the nation, to address the workforce gaps and specifically include minority serving institutions.

- **Create more opportunities with a focus on underrepresented communities.** The semiconductor industry in the U.S. faces the challenge of attracting and recruiting young workers with the necessary skills. Programs that have already been established such as P-TECH, apprenticeship programs, and others like those established by IBM's New Collar initiatives need to be scaled more broadly towards the semiconductor industry. A specific focus on recruitment and retention will require a national effort that provides high quality education across the U.S. This technology network can lead workforce programs to help train new workers in STEM fields, as noted in the National Science Board's Vision 2030 report, will help maintain our global competitiveness.[20]

Technical Agenda

The technical agenda for the technology network will be agreed to by the members of a steering committee, with ongoing input and collaboration from partners. The network footprint can be organized around hubs and geographically distributed centers of excellence. Complementing the Albany hub's technical focus on logic scaling, heterogeneous integration, and design automation, these centers should include one focused on advanced memory, one for fabless design, and another for analog/mixed-signal technologies. The centers of excellence will be in the U.S. with rare exceptions. Centers outside of the U.S. can be considered to advance certain technical capabilities. For instance, high-numerical aperture (high-NA) EUV lithography should include a European center based in Belgium where ASML is the unique worldwide provider of this differentiating technology.

The technical agenda of the technology network could be articulated around the following 4 axes:

- **Manufacturing Research** focusing on next generation nanosheet logic technology and interconnect scaling for the 3nm node and below, including advanced memory scaling, analog/mixed-signal technology and custom enhancements of existing technologies. This effort will be based on a domestic, open, and precompetitive infrastructure. It includes advanced characterization, instrumentation, and testing for silicon devices and for the materials used in fabricating the masks, interconnect, and packages for chiplets at such advanced nodes. The successful results of this research can be transferred to domestic foundries and packaging facilities for use in volume manufacturing. This effort can also include research on the virtualization and automation of tool maintenance, including AI/ML and digital twins, for advanced fabrication and packaging, and development of methods for measuring and analyzing manufacturing data for security and supply chain verification.

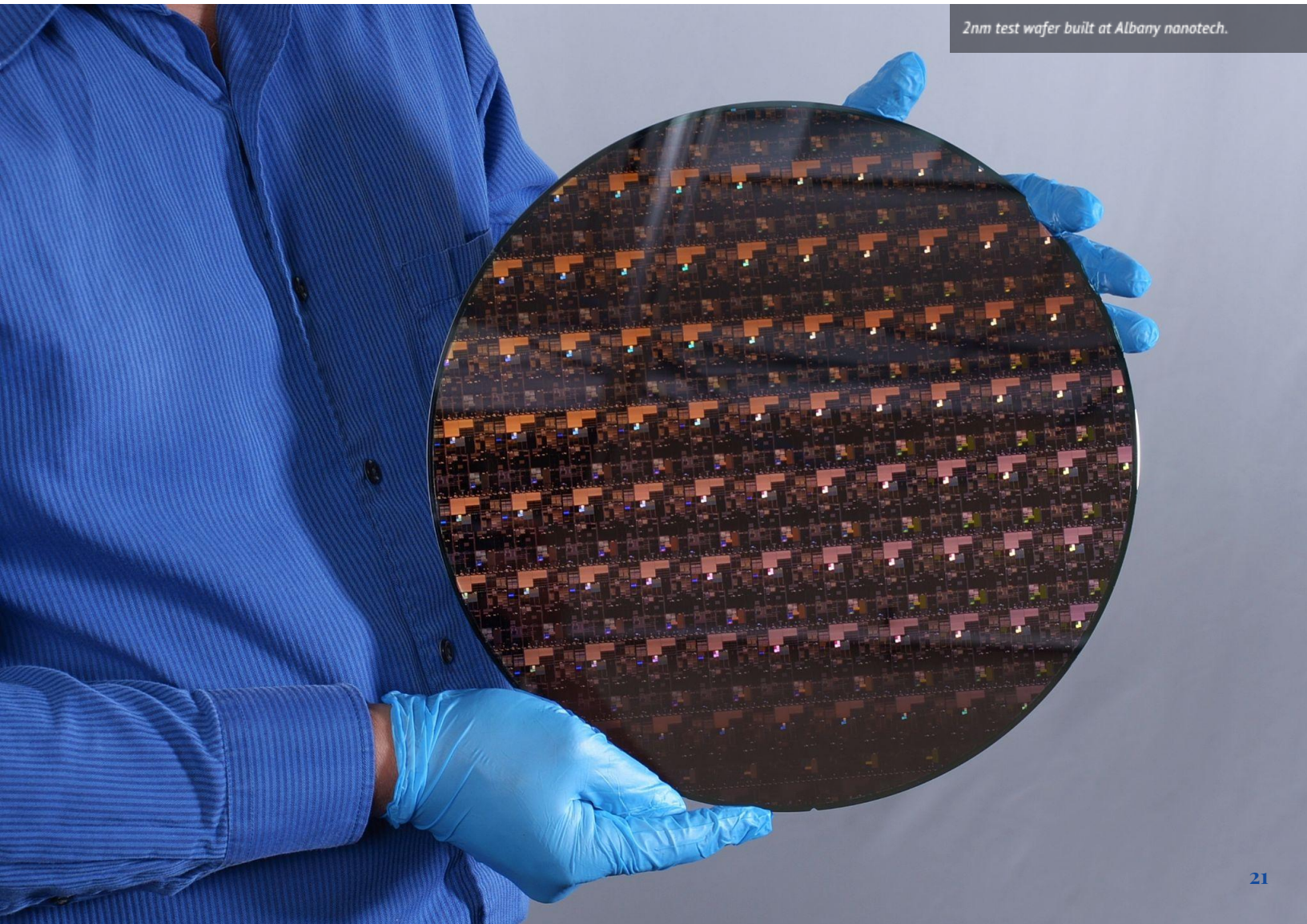
- **Packaging Research** for a next generation heterogeneous open chiplet ecosystem and 3D integration, bond, and assembly, as well as optical and 6G mmWave integration (THz). Chiplet packaging allows technologies – including mature silicon and non-silicon technology – to be mixed and matched at the package level for enhanced functionality. This effort also includes development of advanced packaging substrates, bond and assembly materials and techniques to achieve high density interconnectivity between chiplets, high off-module connectivity such as optical interconnects, and the establishment of open standards for chiplets.

- **Design Research** including chip/package co-optimization and the development of electronic design automation (EDA) tools necessary for next generation logic, interconnect, and packaging, including AI/ML methods for enhancing design productivity and quality, and physics-based design and emulation to allow technology options to be explored before expensive and time-consuming silicon is run. Work in this area can allow the development of novel, reusable IP to accelerate the adoption of new semiconductor technologies. A secure hybrid multi-cloud collaborative design environment using best-of-breed EDA tools and a testbed for cloud modernization of EDA tools and flows can be provided.


Heterogeneous Integration and Packaging Facility at Albany Nanotech complex.

- **Demonstration and Prototyping** to validate novel approaches for industry consumption of all the above technologies in advanced research fabs and manufacturing sites by providing multi-project wafer (MPW) runs and early user hardware through the NSTC and NAPMP network including partnerships with commercial manufacturers. For example, a hub should have a full suite of leading-edge, industry-relevant 300mm processing, testing, and failure analysis tools capable of advanced node CMOS development with 24/7 pilot line operation, building on existing infrastructure. The demonstration and prototyping capability includes engineering short loops for specialty technology and IP. Differentiated interconnect technologies, including advanced embedded memory for AI and other new data workloads on top of commercial transistor technology from U.S.-based foundries, can also be enabled.

For clarity, we define a technology demonstrator as a proof-of-concept for a new technology, proving its viability and illustrating conceivable applications in products - a pre-competitive prototype. A "prototype" is an early sample of a product, used to evaluate a new design and refine specifications (e.g, microarchitecture) for a future product. The technical agenda and research projects will be refreshed on a regular basis by the technical leaders.



2nm test wafer built at Albany nanotech.

Prospective Research Areas

Technology Area: **Manufacturing Research**

Prospective Projects	Technology Demonstrators *(pre-competitive prototypes)* – Path to Manufacturing
Nanosheet Pre-competitive Flow. A robust nanosheet transistor integration baseline flow with world-class inline and offline characterization capability. Fostering a process tool ecosystem around interconnect integration and performance improvements. Use nanosheets as a platform for further logic scaling.	**Multi-project Wafer (MPW) Runs** and early user hardware for demonstration of IP and functional circuit blocks with >10 level metals, advanced test, functional debug, failure analysis, and defect inspection.
Non-volatile Memory Elements and Selector Materials. (PCM/RRAM/FeRAM): develop and integrate embedded non-volatile memory (NVM) in a leading edge CMOS node for Analog In-memory Compute where Compute is performed in memory by mapping a deep neural network (DNN) to arrays of NVM for Deep Learning Acceleration. Fundamental development and characterization of novel memory and selector materials, for extensions to existing memory technologies, for 3D crosspoint memories, or for alternate future memory concepts.	**Analog In-memory Computing Accelerator Core.** A deep neural network (DNN) is mapped to crossbar arrays of non-volatile memory (NVM) devices and the associated matrix-vector-multiply (MVM) operations are performed via in-memory computing.
AI and Digital Twins for Optimized Secure Manufacturing. Methods for enhancing yield, improving factory productivity, and maintaining supply assurance. Development and implementation of analytics and manufacturing controls detecting aberrant events, diagnosing aberrant events, optimizing processes, and predicting the results of processes and the state of tools.	**High-resolution radar.** Arrays beyond 140GHz exploiting new materials and devices as appropriate.
EUV and High NA EUV. Building on the Albany Nanotech advanced lithography capability, provide early access to High-NA EUV exposure capability via a strategic partnership with imec and its ASML partner and foster a holistic mask ecosystem for High-NA EUV involving key investment in U.S.-based mask making capability.	**Greater than 100GHz communications.** Beyond 5G technologies to address wireless with adaptive arrays and interplay with optoelectronics.
mmWave/THz Devices. New optimized devices – both stand-alone and monolithically integrated – for interfacing and processing >100GHz signals.	**Power converter.** High efficiency, high voltage, small size
Power Devices. Optimized for power conversion, distribution efficiency towards higher voltages and frequency to drive high density power solutions.	**Memory Process Vehicles** for collaborative development of new tools and processes for extension of DRAM and NAND technologies, and for crosspoint memory and selector materials.
Passive Devices - i.e. inductors, capacitors, interconnect, MEMS - which complement active devices for high efficiency and integration value for performance/size.	
DRAM and NAND. Materials, processes, and tools to extend DRAM and NAND technologies.	
Crosspoint Memory. Stackable crosspoint arrays, with memory element and two-terminal selector. Process flow to support near-product level prototyping of crosspoint memory arrays, as well as high-density word and bit-line wiring, and memory-optimized transistors for R/W operation.	

Technology Area: **Packaging Research**

Prospective Projects	Technology Demonstrators *(pre-competitive prototypes)* – Path to Manufacturing
Chiplets. Enable chiplet-based architectures and multichip packages addressing physical data link options, internal bus options, compatibility with existing and emerging advanced packaging options, multichip co-simulation, and chip-packaging co-design. Develop specifications and libraries to enable an open design ecosystem and work with key industry participants to accelerate the adoption of standards for an Open Chiplet fabric to enable architectures for current and emerging workloads. **High Density Interconnect Laminates.** Enable prototyping and evaluation of chiplet and multichip packaging architectures. Assess performance (signal and power integrity), reliability, and wiring capability of multiple technologies in conjunction with Si based packaging technologies developed in the NSTC to establish next generation packaging solutions. **Si based Packaging Technologies.** Si fab based advanced wiring and interconnect process technologies for heterogeneous integration and chiplet architectures. Includes through-silicon vias chip and wafer stacking, Si bridges, Si and organic interposers, wafer level fan out, hybrid bonding, Si photonics, and other technologies to drive higher levels of Si integration in 1st level packaging with leading edge ground rules, and interconnect schemes required for emerging applications in the data center (AI and HPC) and edge/mobile computing. **Memory Packaging.** Extensions of current stand-alone memory packaging technologies, with emphasis on tool automation, and low-cost solutions suitable for the different cost structures required in memory versus logic. **Heterogeneous Integration for mixed signal applications.** Combining dissimilar technologies as multiple chips (or substrates) including chiplets, chip- on-chip, chips-on-substrate as well as other solutions. **Thermal and Power**. Package technology addressing high density power thermal management and current distribution. Thermal simulation tools with advanced capability to model thermal behavior from chip to system. **Bond and Assembly.** New materials and processes for pitch scaling and multi-chip packages, including advanced solder materials, discrete and integrated passives assembly, underfills, thermal interface materials, adhesives, epoxy molding compounds, and associated technologies to enable lower cost, high speed assembly, and higher Si integration with heterogeneous components (optics, memory, etc) to enable higher bandwidth, lower latency, and smaller form factors.	**Baseline Packaging Flows and Test Vehicles** to prove out new designs and architectures (logic and memory), and to enable prototyping of these technologies in conjunction with base substrates, new materials and processes to advance the state of the art. **On-module Interfaces.** High-bandwidth density, low power, and low latency electrical bus for on-package die-to-die data communication for system-on-package. **Off-module Interfaces.** Meter-scale interconnects using specialized I/O hub chips while doubling the current serial data rate using advanced modulations and digital signal processing. **Open-standard Chiplets** integrated from different sources connected with high-speed interfaces to create a functional construct.

Technology Area: **Design Research**

Prospective Projects	Technology Demonstrators *(pre-competitive prototypes)* – Path to Manufacturing
Cloud-based Design Platform. A common, shared, multi-organizational design platform for use by commercial, academic, and government organizations. Includes common reference design tool chains and flows based on commercial design automation software; various design tool license pools from "bring your own" licenses to fully cloud license models. Design from inception through mask build for prototype designs. Multiple cloud models will be explored; technology specific foundry support to NSTC design teams, such as foundry design kit support, technology enhancement support, how to bring new processes on-board for NSTC usage, technology assessment, resolving design to process issues, managing multi-party IP integration including block aggregation and MPW management; incorporate DoD Microelectronics Quantifiable Assurance methods. **Electronic Design Automation (EDA) Software.** Enhancing design tools and flows with the early advanced technologies that will be developed by NSTC such as next generation interconnect and scaling, nanosheet device technology, open chiplet interface protocols for 3D and heterogeneous integration; migration of tools and flows to a secure, collaborative, cloud-based design open platform across multiple foundries. Containerization of design tools and flows for multi-cloud design platform implementation. EDA workload characterization on cloud for performance enhancement; AI/ML techniques to enhance the design capabilities as well as to improve design productivity; secure reference flow including circuit protection techniques such as design obfuscation and mixed signal locking to prevent unauthorized design usage, and various side-channel attack analysis and prevention schemes using advanced verification and simulations. **Heterogeneous Integration (HI) Design.** Design methods that take advantage of and support HI including system partitioning, security, power management and delivery, use of AI for HI design, HI technology and system co-design, domain specific architectures, mmWave, and mixed-signal chiplet designs. **Memory Architecture.** Explore new memory architectures including memory-centric compute, analog and neuromorphic solutions for AI, and novel approaches to memory caching, pooling and disaggregation. **Mixed signal Design Methods.** Co-design of system, components, including heterogeneous capability. Multi-physics design, simulation, and validation including thermal, stress, electrical ,and magnetic. Intelligent Design Automation - tools combining advanced modeling and simulation capabilities with machine learning algorithms.	**Logic IP Design and Validation** using baseline flow on state-of-the-art and more advanced PDKs. **Pseudo-SoC Design** consisting of smaller chiplets with comparable performance to a monolithic SoC, but with greater modularity. **Model-based flows** connecting fundamental device physics to interactions with design architecture to optimize overall technology performance.

Centers of Excellence

Several centers of excellence should focus on critical strategic technologies cutting across the research areas. These will be organized by leading companies and universities in the respective areas in coordination with the technology network hubs.

Memory Center of Excellence. Memory is foundational to the data economy and is pervasive across advanced technologies such as AI, 5G and autonomous systems. Advancements in memory set the pace for the broader semiconductor ecosystem. The memory and storage industry revenues have grown faster than the broader semiconductor industry, from approximately 10% of semiconductor industry revenues in the 2000s to ~30% today, and the relative chip area devoted to memory has grown to 80% of the total. The semiconductor memory industry today is built upon two core technologies, DRAM and NAND Flash, both of which are increasingly critical to the U.S.-based information-technology supply chain and U.S. national and economic security .The steep growth in demand will continue given the essential role of DRAM and NAND Flash in all computing. In the coming decade, the U.S. memory industry faces enormous technical challenges in scaling these technologies. A U.S.-based collaboration framework and shared infrastructure focused on advanced development, and which supports sufficiently complete memory prototype vehicles, will help to address these challenges. 3D scaling is the next phase in memory technology advancement, and memory-centric compute is the logical path to perform advanced computing at low energy and high performance. Continued progress, however, requires a complete reimagination of the entire "compute stack" or hierarchy and rearchitecting across the entire stack.

One or more U.S.-based memory centers of excellence can address the challenges through a collaboration framework and shared infrastructure to support this transformation and technological innovation. The center should be equipped with process and metrology tools in a state-of-the-art 300mm clean fabrication space adjacent to existing facilities to maximize efficiency and synergy. The work should include: collaboration with tool vendors on cutting edge memory-specific process technologies for extension of DRAM and NAND technologies; next generation 3D memory technology and tools for complex 3D structures including TCAD materials/structure modeling and metrology; addressing the unique challenges of packaging for stand-alone memory, which are distinct from logic and heterogeneous packaging; heterogeneous integration (functional and/or physical); X-point array technology integrated with advanced CMOS for new memory cell technology validation; developing a broad system-architecture based approach and prototypes for integrating new memory concepts beyond DRAM and NAND; developing designs that eliminate costly data movement, including computational memory, taking advantage of analog or analog-like devices, and novel architectures for memory pooling and disaggregation.

The memory center would be configured to facilitate expanded interaction opportunities between industry and university researchers and to provide advanced facilities with state-of-the-art tools and a mentoring environment for workforce development. It should be designed to ensure easy access to facilitate a fast ramp from lab to fab, and for demonstrating new concepts by start-ups and small companies working at the leading edge of technology. These innovations will drive the future of modern computing systems which provide the basis for much of our national economic prosperity.

Analog/Mixed Signal Design Center of Excellence. This center will drive the technology which interfaces to the real world by sensing, converting, and processing signals and energy towards a more efficient and intelligent world. The technology spans multiple distinct segments, each of which may justify separate focused centers across a distributed structure. Specific technology segments include: power management, high-voltage power, mmWave/THz RF, data acquisition, high-speed communications and intelligent sensing as highlighted in the SRC Decadal Plan.[21] Each focused center would cover topics ranging from materials and devices to circuit and system design, heterogeneous integration, test, quality, design tools, and modeling. Centers will focus on advanced prototyping for analog components and will have capability via bridge tools to bring mature concepts to the NSTC hub as an integration element in a broader system context. Key applications include but are not limited to: autonomous vehicles, communications infrastructure, smart cities, green energy, and health care, which are all enabled by analog/mixed signal technology.

International Center of Excellence (imec High NA EUV and ≥N+4, N+3 technology). Together with ASML in a joint High-NA EUV Lab, imec (HQ in Belgium) is focusing on the infrastructure preparation which is necessary for high-NA scanner development. This includes dedicated EUV metrology, resist development, mask preparation, etch processes, and overall material development. For that purpose, imec collaborates with numerous material and equipment suppliers to contribute to the establishment of a complete high-NA ecosystem. Additionally, imec has on-going strategic partnerships with most key U.S. industry and academic stakeholders, focused on screening options for technology 3 to 4 generations (7 to 10 years) ahead of manufacturing including advanced CMOS, advanced memory, advanced 3D and heterogeneous integration, and advanced analog and derivative technologies. Imec's Lab-to-Fab operations deliver fast-paced demonstration capability and have been an invaluable resource for many companies, notably including ambitious deep-tech start-ups. A strong partnership within NSTC will help to advance NSTC capabilities and accelerate success of the collaborative effort of the technology network, other centers of excellence, and the Albany hub, complementing the U.S. innovation ecosystem. Leveraging the operations, strategy, and partnership structure of imec's proven world-leading innovation ecosystem, built over the past three decades, will provide both immediate and long-term benefit to NSTC.

Some Major National and International Capabilities - Key Partnerships. The capabilities of some of the contributors to this document are illustrated below. These and many other institutions will provide expertise that the technology network can bring to bear on the NSTC and NAPMP missions.

ALBANY NANOTECH - CENTER FOR SEMICONDUCTOR RESEARCH			
Greater than $15B investment	1.1M ft^2 Office & Lab Space	>150K ft^2 Clean Room Space	More than 200 Industry Partners
New York State, State University of New York, IBM partnership since 2002	300mm EUV Development Fab	Ecosystem - including Test, Meteorology, and Characterization	Recent Packaging Investment - C4 Line in Albany

MIT[17]		
40,000 ft^2 of class 100/1000 cleanroom housing shared capabilities for processing of silicon, compound semiconductors, and a wide range of nanomaterials for applications in devices and circuits. E-beam and ion beam tools for micro- and nano-scale patterning and metrology from wafer pieces up to 200 mm wafers.	15,000 ft^2 housing extensive shared facilities for materials characterization, including atomic-scale structure and chemical analyses (reaching resolution as high as 80 pm) and capabilities for in-situ studies of materials processes that control structure and properties.	Direct access to MIT Lincoln Laboratory's 200 mm Prototyping Facility, with 90 nm lithography capability, operating full-flow fabrication across a broad range of integrated circuit technologies, including FD-SOI CMOS, CCD imagers, superconducting electronics, photonics, MEMs, and microfluidics.
Extensive heterogeneous integration and packaging capabilities at MIT Lincoln Laboratory used to demonstrate technologies that led to 75 R&D 100 Awards since 2010. These are complemented by MIT campus toolsets for packaging and integration.	Pioneering research on microphotonic materials and devices, spintronics and magnetic materials, twistronics, quantum materials and devices, neuromorphic computing technologies, nano-scale devices and monolithic integration of GaN and nanomaterial-based devices with CMOS.	Interdisciplinary Laboratories and Centers that support a wide range of research on microelectronics research, microsystem design, artificial intelligence and machine learning, and many other topics. These labs and centers integrate research across the Schools of Engineering and Science, and the College of Computing.

ROCHESTER TEST, ASSEMBLY, AND PACKAGING FACILITY
300mm state-of-the-art advanced facility for integrated silicon photonics testing, assembly, and packaging with services to academia, private industry and government

BROOKHAVEN NATIONAL LABORATORY[18]		
State-of-the-art, medium-energy electron storage ring facility, National Synchrotron Light Source-II, provides spectroscopic tools for probing electronic state, binding energy, and chemical states, scattering methods sensitive to ferroelectric, magnetic and correlated domains, profiling from surface to bulk tunability and is non-destructive, in-situ	Next-generation materials and integration focus - novel materials including neuromorphic, 2D control and integration (e.g. twistronics) and 3D integration (e.g . self-assembly)	Microelectronics for extreme environments - testing and modeling at deep cryogenic temperatures and high radiation

RENSSELAER POLYTECHNIC INSTITUTE	
State of the art computing facilities including the Supercomputer AIMOS within the Center for Computational Innovations (CCI),the most powerful at any private university. Scientific Computation Research Center (SCOREC) with deep expertise in simulating semiconductor and packaging materials and process flows with an emphasis on the application of ML/AI techniques.	Center for Materials, Devices and Integrated Systems (CMDIS) for advanced materials processing and characterization including micro-scale and nano-scale cleanroom for a "universal "set of materials and geometries and development of new methods for nano-scale characterization of structure, chemistry and properties.

STATE UNIVERSITY OF NEW YORK SYSTEM			
Largest comprehensive system of higher education in US: 9 doctoral granting including 4 University Centers (University at Buffalo, Binghamton University, University at Albany, Stony Brook University), 20 tech and liberal arts colleges, 30 community colleges	~48% of BS/BA graduates annually are transfer students, many from community colleges and using SUNY's transfer paths.	370,000 credit-bearing students, 18.2% in STEM fields, 27.3% under-represented minority. 961,000 non-credit bearing enrollment. (Fall 2021)	High social mobility: SUNY has 6 campuses in the top 50, 16 campuses in the top 100, and 20 campuses in the top 200 campuses nationally for social mobility.[19]

CORNELL UNIVERSITY

Cornell NanoScale Science and Technology Facility (CNF) is a uniquely capable, open-access nanofabrication and nanocharacterization center offering outstanding tools and capabilities for both research and prototyping. As one of the largest (17,000 ft^2 of cleanroom space) and most comprehensive sites in the NSF-supported National Nanotechnology Coordinated Infrastructure (NNCI), CNF boasts 45 years of experience as a national and international user facility for start-to-finish fabrication of micro-, nanoelectronic and photonic devices, supporting both the academic research community as well as large and small companies.

Over 180 processing and characterization tools with emphasis on e-beam lithography, advanced stepper-based photolithography, and a wide array of deposition and etching, packaging, characterization, and software resources.

Experienced staff provide workforce training to hundreds of new undergraduate and graduate student users each year.

A strong engine of economic development, CNF has hosted over 125 companies, 61 U.S. academic institutions, 5 government labs, and 23 foreign institutions as part of NNCI. Partnerships with Cornell business incubators, Praxis and The McGovern Center have helped in founding over 15 companies in the last 5 years.

Cornell also maintains a range of state-of-the-art microscopy and materials characterization facilities through the Cornell Center for Materials Research and a suite of synchrotron beamlines through its Cornell High Energy Synchrotron Source.

UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

Holonyak Micro and Nanotechnology Laboratory (HMNTL), a shared user facility for semiconductor, nanotechnology and biotechnology research, with over 8000 sq. ft. of class 100 and 1000 clean rooms and state-of-the-art laboratories for ultra-high speed optical and electrical device measurements. Current capabilities include growth facilities for III-V and III-N compound semiconductors and a full suite of processing tools for device fabrication, including the highest accelerating voltage e-beam lithography system in North America. Those resources enable research on photonic devices from the UV through long-wavelength infrared, high-speed electronic devices to the THz regime, and novel devices at the intersection of semiconductors and biological systems.

The Materials Research Laboratory (MRL), one of the largest shared instrumentation facilities in the nation, with over 140 advanced instruments for materials characterization, including atomic resolution TEM and analytical scanning SEM with 0.2-nm beam for z-contrast imaging, ES, EEL, and nano-diffraction. The facility also contains resources for the fabrication of patterned micro- and nano-sized structures on flexible and other multi-layer electronic substrates, including class-100 cleanroom space, e-beam lithography, and thin film deposition.

GEORGIA INSTITUTE OF TECHNOLOGY			
3D Systems Packaging Research Center (PRC), a graduated NSF Engineering Research Center, is the largest academic center focused on advanced packaging in the world. The center has deep expertise in all aspects of packaging including design, materials, process, assembly, reliability, thermal, and system integration. The center currently collaborates with 41+ companies, 14 universities, several federal agencies and has a track record of translational activities, education, and workforce development. Georgia Tech is also home to the Institute for Electronics and Nanotechnology (IEN), which maintains one of the largest academic micro/nanofabrication facilities in the country with 25000 sq. ft. cleanroom space, 7500 sq. ft. microscopy space, and 170 tools with more than 1000 users.			
State of the art design, fabrication, assembly, and test facility dedicated to advanced packaging	150mm and 300mm panel scale processing and assembly with electrical characterization to 350GHz	Package curriculum both at the undergraduate and graduate level to educate students on fundamentals and advances in packaging	Coordinating office for the National Nanotechnology Coordinated Infrastructure (NNCI) for micro and nano-fabrication

PURDUE UNIVERSITY – A LEADER IN MICROELECTRONICS AND ADVANCED PACKAGING RESEARCH		
Lead institution on SRC-funded centers: JUMP Center for Brain Inspired Computing (C-BRIC), nCore NEW LIMITS center, and co-lead with Binghamton University on the Center for Heterogeneous Integration Research in Packaging (CHIRP)	Leads the DoD supported Scalable Lifecycle Engagement (SCALE) workforce development program with seventeen university partners for system on chip, heterogeneous integration and advanced packaging, embedded systems security, supply chain awareness, and radiation hardened technology.	Network for Computational Nanotechnology (nanohub)
Center for Secure Microelectronics Ecosystem sponsored by TSMC, Synopsys and DoD	Cooling Technologies Research Center, a graduated NSF Industry-University Cooperative Research Center	187,000 square foot Birck Nanotechnology Center, which includes the Scifres Nanofabrication Laboratory, a 25,000 sq. ft. ISO Class 3-4-5-6 (Class 1-10-100-1000) nanofabrication cleanroom

IMEC – UNIQUE 300MM R&D PARTNERSHIP IN LEADING-EDGE TECHNOLOGIES			
$4B leading equipment investment: 120K sq. ft. clean room space; 24x7 operation; 5000 people	Screening options for the N+3 and N+4 generations	Globally largest independent research program in industry partnership	Unique suppliers' hub infrastructure
Fundamental understanding and advanced introduction of novel materials	300mm high NA-EUV Fab (35 years of ASML partnership)	Unique metrology and characterization	Physics, modeling, reliability of new device architectures and interconnect schemes

UNIVERSITY OF CALIFORNIA, LOS ANGELES

Pioneer in Si-based packaging technologies and integration

Pioneered key concepts and technologies for heterogeneous integration of chiplets. Adapting silicon technology for advanced packaging constructs. Waferscale integration on a Silicon Interconnect Fabric for high performance systems and wafer-level fan-out technology

UCLA CHIPS is a vertically integrated packaging center driving applications, design methodologies, equipment, and process development and has a proven record of translation into scaled-up manufacturing at the design, equipment and process levels.

Ranked the best public university in the US and hispanic-serving institutions. 30% of undergrads are first time ever graduates in their families.

California NanoSystems Institute (CNSI), a semiconductor and packaging facility funded by the state of California, includes nm-scale lithography, advanced package assembly and early prototyping.

System modeling for chiplets, communication protocols, and disaggregation/re-integration methodologies.

ARGONNE NATIONAL LABORATORY

Argonne's world-class materials science and physics capabilities, backed by national facilities such as the Advanced Photon Source (APS), the Center for Nanoscale Materials (CNM), and the Argonne Leadership Computing Facility (ALCF) are positioned to develop the next generation of new materials and processes for energy efficient information processing science and technology.

The Advanced Photon Source, being upgraded now with scheduled first light in 2024, will be the brightest hard X-ray source in the US, 500X more intense and coherent than current levels. This will enable 3D nanometer scale chemical and physical imaging of mm^3 volumes on realistic timescales, offering unprecedented advantages in understanding the behavior of future microelectronic materials and circuits.

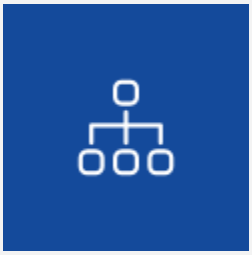
- Wide expertise in discovery science and processing of thin film dielectrics, polymers and magnetic materials.
- Green processing and the environmental costs of future computing.
- Materials discovery via autonomous synthesis and computational science, leveraging Aurora (being delivered now), one of the world's first exascale computers.

Defining Success

Near Term

Rapidly open a fully-operational hub for the technology network

Establish Centers of Excellence



Build sustainable ecosystem that includes a wide variety of stakeholders critical to the success of the NSTC and NAPMP mission

Define and execute on a research and development agenda focused on impact

Facilitate successful and consistent "lab-to-fab" transfers

Ensure the network is sustainable for long-term contributions to U.S. semiconductor leadership

Call-to-Action

These are unprecedented times for the semiconductor industry. The U.S. faces near-term challenges with dire economic and security implications, should the nation not rise to meet them. Thankfully, there is an existing foundation to build upon rapidly to safeguard the country in the near-term and the future. To ensure this outcome, the NSTC and NAPMP should have a national footprint and be enabled by a technology network for research, development, and prototyping with first-class resources, scientists, facilities, and partners who can work quickly and efficiently to demonstrate and transfer breakthrough technology to manufacturing. Basing a major hub in New York State provides a solid foundation to secure a strong domestic chip supply chain for the future.

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