EASY RADIATION-HARDENING OF CONVENTIONAL INTEGRATED CIRCUITS USING HARDSIL® TECHNOLOGY

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INTRODUCTION

The radiation present in space and other extreme environments can have a catastrophic effect on an integrated circuit (IC). HARDSIL® technology mitigates these radiation effects on the IC. In contrast to ICs designed and manufactured using standard commercial design and manufacturing processes, high-reliability Radiation-Hardened (Rad-Hard) electronic components are designed and manufactured so that exposure to ionizing radiation and/or extreme temperatures does not result in malfunctions or catastrophic failure of the device. VORAGO's HARDSIL® technology is an add-on module to the conventional IC manufacturing process, eliminating the need for costly and time-consuming modifications to the process or expensive specialized Rad-Hard design libraries. Re-use of the existing baseline process modules enables re-use of pre-existing design and IP libraries. It also enables radiation-hardening of existing products by retro-fitting of HARDSIL® process modules into the existing flow with little or no design work, depending on the details of the original design. HARDSIL® protects the device from the effects of harmful radiation including both instantaneous effects like Single-event Upset (SEU) and Single-event Latchup (SEL) and cumulative effects like Total Ionizing Dose (TID).

ENERGETIC PARTICLE STRIKES AND SINGLE-EVENT TRANSIENTS (SET)

When an energetic particle travels through an integrated circuit, it leaves a trail of electron-hole pairs in its wake, as shown in Figure 1. These can be created by direct ionization through inelastic interactions or indirect ionization through the by-products of nuclear interactions. Some of these electron-hole pairs recombine in the substrate but a large fraction of them diffuse and drift through the substrate to the Si surface. Strikes which pass through the transistor depletion regions deform these regions, forming a funnel-shaped elongation along the particle track. As the depletion region snaps back to its original shape, the generated charge within this is swept into the associated transistor Source/Drain region and circuit node. This "prompt collection" occurs on the order of a few tens of picoseconds and produces a short, sharp peak of current collection. After the depletion region funnel has collapsed, electron-hole pairs continue to diffuse and recombine in the substrate. As they reach the surface devices and are collected into biased device regions by the electric fields, there is a more prolonged period of charge collection. This current is less peaked than the prompt collection current and can last for hundreds of nanoseconds.

The overall flow of current will typically spread along and away from the initial strike path. The negative effects of the charge created by these ion strikes are known as Single-event Effects (SEE).

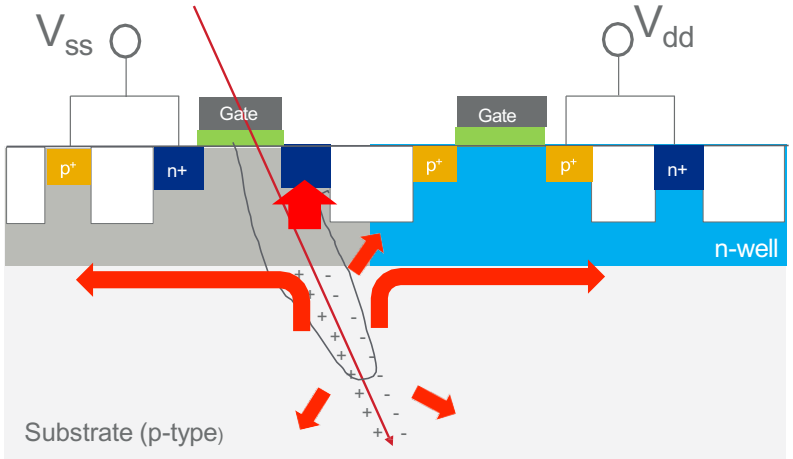

FIGURE 1. SCHEMATIC OF ELECTRON-HOLE PAIRS FORMED ALONG THE STRIKE PATH AND THE "FUNNEL EFFECT".
THE ELECTRON-HOLE PAIRS DRIFT AND DIFFUSE IN THE SUBSTRATE WITH A SUBSTANTIAL FRACTION BEING COLLECTED BY THE INTEGRATED CIRCUIT NODES.

In a commercial process, the charge generated by a strike in the silicon as deep as 3-5µm can migrate back to the surface devices, causing upsets. The charge generated by a strike can also travel laterally away from a particle strike by as much as 4-5µm. The vertical and lateral extents of the charge creation volume depend on the amount of energy deposited in the substrate by the energetic particle measured by its Linear Energy Transfer (LET).

Charge generated by energetic strikes which migrates to the Si surface will be collected by various nearby circuit nodes, altering the potential and currents at these nodes and ,thereby, potentially changing circuit operation. For example, if this charge ends up in a memory cell, the memory state can be flipped. If this charge ends up in a logic gate, several negative effects are possible. A strike can flip the state of a latch or flip-flop directly, temporarily change a logic state and cause an output transient, change a clock edge, or create a false clock edge.

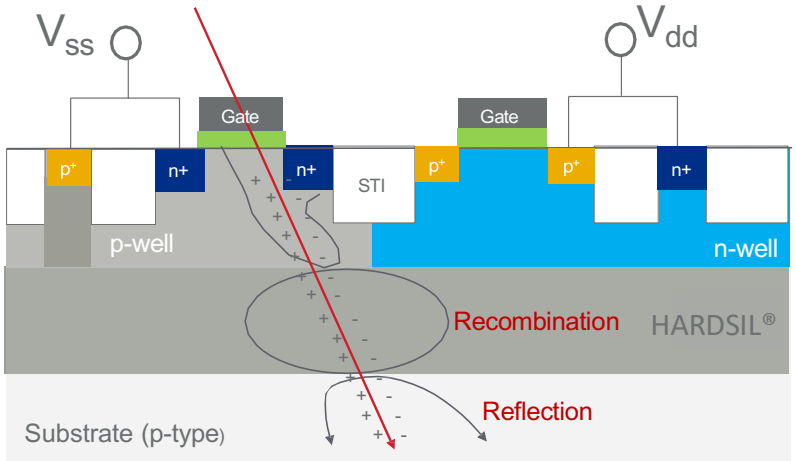

FIGURE 2. HARDSIL® REDUCES CIRCUIT NODE CHARGE COLLECTION BY REDUCING THE FUNNEL EFFECT, BY ACCELERATING RECOMBINATION AND BY REFLECTING CHARGE INTO THE SUBSTRATE.

HARDSIL® has been shown to reduce the charge collection depth to <0.5-1.5µm (depending on ion LET), as well as reduce the lateral extent to <1.5µm (for very high LET particles) and <1µm for low to intermediate LET particles. HARDSIL®, as illustrated in Figure 2, reduces the extent of the Funnel Effect, increases the rate of recombination in the substrate below the device region and reflects some charge back into the substrate to recombine. The reduced collection volume with HARDSIL® means that there is less charge to be collected and a smaller distance for the collected charge to travel. Shorter prompt collection and diffusion collection durations with lower current magnitudes in both is the end result. This reduced charge collection hardens digital and analog circuits against Single-event Transients (SET).

SINGLE-EVENT UPSET (SEU)

A Single-event Upset (SEU), a type of radiation-induced soft error, is the loss of the digital data state (0 --> 1 or 1 --> 0) in memory due to a radiation strike. Electron-hole pairs are generated along the particle strike path. Unrecombined electrical charge, generated by the passage of the particle, is collected to circuit nodes and can lead to corruption of memory cell contents.

When a heavy ion strikes a memory cell in an array directly, depending on the Linear Energy Transfer (LET) and strike location, the deposited charge is often enough to not only take the struck cell out of its original memory state, a Single Bit Upset (SBU), but can also upset multiple surrounding memory cells. HARDSIL® limits the upset of surrounding memory cells (reduced lateral upset extent), even for strikes from very high LET particles. HARDSIL® also helps reduce the amount of charge injected into the struck cell, which raises the minimum particle LET required to induce an upset in the struck cell itself. However, cells struck by particles with higher LET than this minimum threshold will be upset. For adjacent cells witin the “upset radius”,

smaller with HARDSIL®, to be upset, the effective LET for these cells must also be higher than the required threshold. Therefore, there is a second, even higher threshold for Multiple Cell Upsets (MCUs). The Single Bit Upsets (SBUs) which do occur can be mitigated with relatively low-cost error correction methods like Error Correcting Codes (ECC) as long as the number of errors per WORD is maintained below the number the method can correct. This can be done in multiple ways. By physically separating the bits in a WORD by greater than the lateral extent of a single strike disturbance, a single strike cannot upset multiple bits per WORD. Since it shrinks the lateral extent of the disturbance, the required minimum spacing is much smaller with HARDSIL®. To complement the physical spacing and prevent multiple strikes from overwhelming the chosen error correction algorithm, data WORDs in memory protected by HARDSIL® are periodically checked for errors and their contents refreshed. These memory SCRUBs are done at a frequency sufficient to prevent occurrence of uncorrectable Multiple Bit Upsets (MBU).

ICs designed for conventional CMOS processes use Fault-tolerant redundancy methods, such as Dual Interlocked Cell (DICE) and Triple Modular Redundancy (TMR) to provide robustness against upsets in latches and flip-flops. A DICE latch is made by combining redundant, mutually-repairing latches. However, the DICE latch will be still prone to SEU whenever the lateral extent of upset from a single particle strike exceeds the separation between critical nodes. In addition, DICE latches remain somewhat vulnerable to SET. HARDSIL® reduces the spatial extent of the disturbnces, allowing for more compact layout of the DICE latch while simultaneously reducing the strength of the disturbance from the energetic strike. TMR uses three copies of the same logic or analog block with a decision block which decides the correct final output by majority voting. The redundant copies need to be spaced to prevent two simultaneous malfunctions. HARDSIL® decreases the minimum required spacing for any confidence level. In addition, TMR remains vulnerable to a malfunction in the voting block. HARDSIL® allows the redundant copies to be placed more closely, increasing area efficiency, and improves the SEU and SET robustness of the decision block. The ability of HARDSIL® to drastically reduce the lateral upset extent of single particle strike, even for very high LET particles, significantly enhances the effectiveness of fault-tolerant techniques while significantly reducing the minimum required separation distance between critical nodes of these fault-tolerant techniques, easing implementation and improving performance.

The use of HARDSIL® decreases the lateral upset extent of a particle strike to less than one-third of what it would be for a non-Rad-Hard device. Also, the onset LET is increased by more than a factor of three, as compared to commercial CMOS devices. The particle strike saturation cross- section is reduced to less than one-tenth of the typical equivalent commercial device and has a more gradual transition from onset to saturation portions of the Weibull curve compared to the commercial process. The overall effect is a reduction of the SER in Geosynchronous Orbit, Solar Minimum to approximately one-tenth of that of the commercial process.

In VORAGO produts, a combination of HARDSIL®, SRAM ECC and memory SCRUB to eliminate accumulation of SBUs over time, has been used to drive uncorrectable SRAM SER to fewer than 1E-15 errors/bit-day.

SINGLE-EVENT LATCHUP (SEL)

In most CMOS technologies, parasitic bipolar devices are created underneath the CMOS transistors. The cross-coupled NPN and PNP together form a parasitic thyristor, or PNPN device, shown for bulk CMOS in Figure 3 . If either BJT turns on, its collector current acts to bias the other BJT on through the corresponding IR drop. The second BJT, in turn, now acts to drive the first even further into its forward active region. This runaway positive feedback creates a low- impedance path between V_{DD} and V_{SS}.

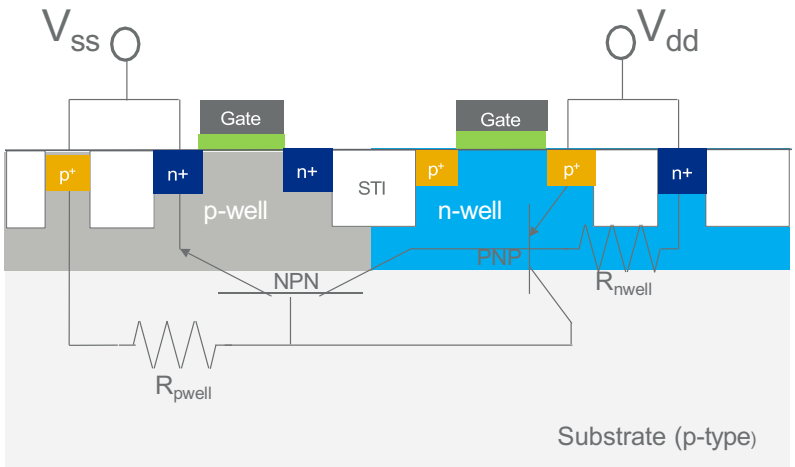

FIGURE 3. CROSS-SECTION OF A BIASED BULK CMOS PAIR SHOWING THE LUMPED REPRESENTATION OF THE PARASITIC BIPOLARS AND SUBSTRATE AND WELL RESISTORS WHICH ARE THE PRINCIPAL COMPONENTS OF THE CMOS LATCHUP THYRISTOR.

An example of the well-known device characteristic which results from this positive feedback is shown in Figure 4. The vertical dotted line indicates the supply voltage in this example. The points T and H are the Trigger and Holding Points. The Trigger Point is the point at which enough current is flowing in the thyristor to enable the latched state through positive feedback. The voltage at the Holding Point, known as the Holding Voltage, is the lowest voltage required to keep the thyristor latched. If the voltage drops below this value, the thyristor exits the latched state. State A is the normal low-current operating point. State B is a possible post-latch operating point if the latchup event does not impact the supply voltage and the system can supply the required current. Because B is unstable, the latched device is likely to draw more current through from the power supply. This can cause permanent damage to the interconnect and in the Si substrate, unless addressed immediately by forcing the device out of the latched state. Permanent damage leads to loss of correct functionality.

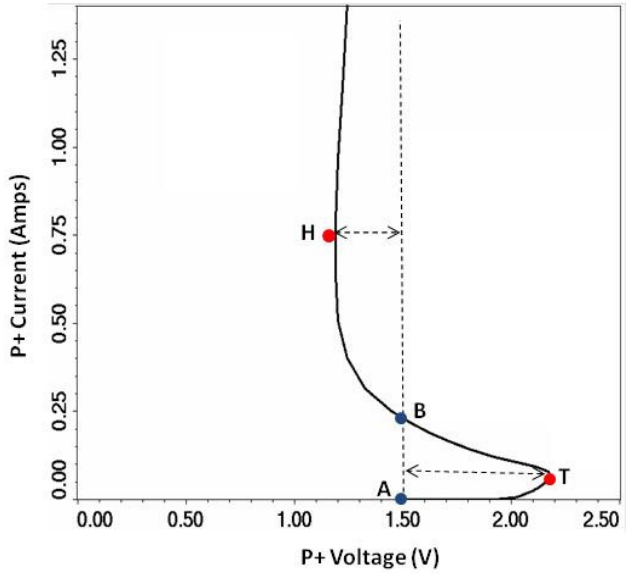

FIGURE 4. EXAMPLE LATCHUP CURVE SHOWING THE TRIGGER POINT (T) WHICH MARKS THE INITIATION OF THE LATCHED STATE AND THE HOLDING POINT (H) WHICH MARKS THE MINIMUM VOLTAGE NECESSARY TO SUSTAIN THE LATCHED STATE. A IS THE NORMAL OPERATING POINT AND B A POSSIBLE POST-LATCH OPERATING POINT.

The electron-hole pairs generated by a energetic strike flow through the parasitic PNPN thyristor on their way to being collected by circuit devices and well ties. A strike which can supply sufficient charge will turn the thyristor on, causing a self-sustaining low impedance pathway which can tie circuit nodes to either power rail, possibly leading to a Single-event Functional Interrupt (SEFI), or, more critically, a high current pathway from power to ground and a Single-event Latchup (SEL). A SEFI is a soft error and does not require power cycling but a SEL will persist until the power supply is cycled, unless the Holding Voltage is higher than the supply voltage or the device cannot supply enough current to sustain the latchup. This latter ondition is oftent the result of permanent physical damage due to the extremely high current flowing in the low impedance latched state. In the best cases, the condition is recognized and the power cycled, leading to an interruption of function. In the worst case, the device is destroyed by the extremely high current density.

HARDSIL® protects against SEL by weakening the parasitic PNPN. It does this in two ways, which can be illustrated with Figure *5*. In a typical implementation, HARDSIL® lowers the apparent P- Well resistance. This makes it significantly harder for current flowing through the substrate to forward-bias the parasitic NPN Emitter-Base junction and turn on the NPN. HARDSIL® also weakens the parasitic NPN transistor itself, driving its current gain down. With its decreased gain, the NPN is less able to drive the current needed to turn on the parasitic PNP, so that the positive feedback loop is degraded and a latched state becomes very hard to achieve. Once the

trigger current has been made sufficiently high, the initial currents induced by the particle strike will be less than the trigger current and induce latchup.

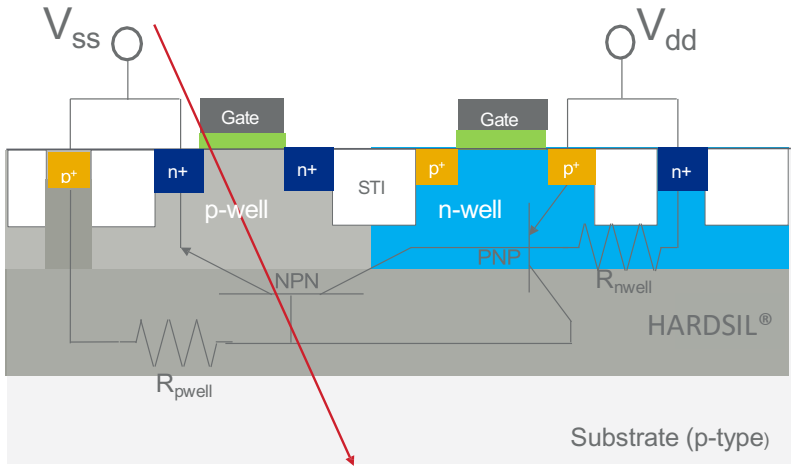

Figure 5. Cross-Section of a bulk CMOS pair with HARDSIL® layers introduced. HARDSIL® weakens the parasitic PNPN structures and makes it extremely difficult for an energetic strike to cause SEL.

The amount of energy that an ionizing particle transfers to the material, per unit distance, is called Linear Energy Transfer (LET). When comparing SEL of a commercial (non-Rad-Hard) device with a device that has been manufactured with HARDSIL® technology, the difference is dramatic. For a commercial CMOS device, without HARDSIL®, SEL can be induced by ion LETs as low as 3 MeV-cm^2/mg, depending on process. The VORAGO HARDSIL® CMOS device is immune to SEL for ion LETs greater than 110 MeV-cm^2/mg. By incorporating HARDSIL® into the semiconductor processing flow, the effects of energetic strikes, including the likelihood of SEL, are greatly reduced.

Total Ionizing Dose (TID)

Unlike SEU and SEL, TID is a cumulative degradation phenomenon. Natural ionizing radiation (gamma rays, X-rays, protons, and heavy ions) interact with atoms in the silicon and dielectric materials of integrated circuits, depositing energy within these materials. This deposited energy liberates electrons from atoms in the material and forms electron-hole pairs. In the presence of an electric field, the electrons and holes are separated before they can all recombine. Within oxides, electrons are more mobile than holes so, in the presence of an applied electric field, many leave the dielectric, leaving behind the positively charged holes. The holes move more slowly through the dielectric and, in the case of SiO_2, their hopping between localized states also liberates positively charged Hydrogen ions (protons). Some holes become trapped in in bulk traps within the dielectric while other holes and the liberated protons migrate to the interface

between the dielectric (SiO_2) and semiconductor (Si), if that is the cathode. Once at the interface, the holes can become localized in interface states while the protons can create additional interface states. As irradiation continues , positive charge build-up continues in the dielectric.

This accumulation of positive charge in oxides attracts mobile electrons to the Silicon side of Silicon-Silicon Dioxide interfaces. In highly scaled CMOS processes, the gate oxides are thin enough that quantity of trapped charge in the Gate dielectric is limited and has much less impact on device performance than in previous generations of technology. However, due to the use of oxide isolation techniques like shallow trench isolation (STI) to define transistor regions, significant charge build-up along the transistor channel sidewalls and bottom of the oxide isolation material will still occur. Most circuits are much more tolerant of raising the turn-on voltage / reducing source-drain leakage along the sidewall of PMOS devices than lowering the turn-on voltage / increasing source-drain leakage along the sidewall of NMOS devices. Another major issue in most CMOS processes is the existence of parasitic field NMOS devices (formed between the Nwell of a PMOS transistor and the source/drain region of an adjacent NMOS transistor). Accumulation of charge along the bottom of the oxide isolation will significantly lower the turn-on voltage and increase the leakage of these parasitic NMOS devices. Typically, it is the TID impact on NMOS and parasitic NMOS transistors which sets the TID tolerance of the device.

Total Ionizing Dose effects are resolved in HARDSIL® technology by raising the threshold voltages of the parasitic NMOS transistors, thereby increasing the total positive charge needed to induce any level of leakage current in the parasitic NMOS transistors. HARDSIL® is designed to accomplish all this without impacting the characteristics of the normal NMOS and PMOS devices.

A typical CMOS device, without protection from radiation, could potentially withstand TID of up to 50 krad(Si). A CMOS device that is produced using HARDSIL® technology can withstand TID of greater than 300 krad(Si).

CONCLUSION

HARDSIL® technology has been proven effective at significantly reducing Single-event effects (SEE) caused by radiation present in space environments. Single-event latchup (SEL) has been eliminated with HARDSIL®. A combination of HARDSIL®, ECC, along with memory SCRUB to eliminate accumulation of single bit errors over time, drives uncorrectable SER to below 1E-15 errors/bit-day in VORAGO products. Without HARDSIL®, a typical COTS CMOS device could potentially withstand TID of up to about 50 krad(Si), whereas a CMOS device that is produced using HARDSIL® can withstand TID of greater than 300 krad(Si). Table 1 is a summary of the reduced effects of radiation on a CMOS device when HARDSIL® is implemented into the manufacturing process.

Table 1. Comparison of the effects of radiation on commercial CMOS vs. VORAGO HARDSIL® CMOS devices.

	Digital CMOS (Combinatorial Logic, Registers, Flops, SRAM)			
Parameter	Commercial Process		HARDSIL Process	
	No DICE / TMR Registers - Flops or SRAM ECC	with DICE / TMR Registers - Flops & SRAM ECC	No DICE / TMR Registers - Flops or SRAM ECC	with DICE / TMR Registers - Flops & SRAM ECC
Total Ionizing Dose	Typical < 50 krad		> 300 krad(Si)	
Ionizing Patricle Effects				
Single Event Latch-up	Induced by ion LETs as low as 3MeV-cm^2/mg depending on process		Latch-up immune for ion LETs up to 110MeV-cm^2/mg	
Single Event Upset - single bit upsets (low LET particle strikes)	Weak to Single Event Upset for all ionized particle LETs. Without DICE/TMR or SRAM ECC no distinction between SBE and MBE impact on circuit	Improved immunity to SEUs due to DICE/TMR & SRAM ECC	Decreases upset diameter to <1/3 and Increases LETonset by >3x compared to commercial, reduces Saturation cross-section to <0.1x and has more gradual transition from onset to Saturation portions of the Weibull curve compared to the commercial process. Combined effect is a reduction of the SER @ Geosynchronous Orbit, Solar Minimum to ~0.1x that of the commercial process. Without DICE/TMR or SRAM ECC no distinction between SBE and MBE impact on circuit	Combination of HARDSIL and DICE/TMR & SRAM ECC (with some form of SCRUB to eliminate accumulation of single bit errors over time) drives uncorrectable SER to VERY low levels (<1e-15 errors/bit-day)
Single Event Upset - multi-bit from single particle strike upsets (higher LET particle strikes)		Weak to Single Event Multiple bit Upsets for higher ionized particle LETs, especially when particle strike is not normally incident		