Hiring Manager: Thomas Krawczyk
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Jariet is a mature startup with a large customer base in the aerospace and commercial markets. Our focus is on Digital Microwave, which takes our very high speed 64+ GS/s ADC and DAC data converters and marries them with our digital systems for up and down frequency conversion. We have developed test-chips and use them to demo our state-of-the-art hardware. We are now transitioning to production versions of our IP and ASICs. Our location in Redondo Beach has our test lab and analog AFE design team. In our second office in Aliso Viejo we have the digital and analog data converter team.

We are actively searching for highly motivated individuals that enjoy challenging, execution-oriented design work with high performance ADC, DAC, PLL devices. We currently utilize 14nm CMOS technology and are looking at scaling to smaller geometries. Our design team requires engineers capable of assuming a broad range of development responsibilities, including chip design, layout, design verification, and test validation. Candidates must have experience working in commercial analog development teams and executing standard design processes and flows.

CMOS Analog Design:

1. General (motherhood and apple-pie):
    a. Understand and analyze system level design requirements
    b. Review existing publications, literature, conference proceedings to investigate solutions to requirements
    c. Work within team to design and simulate viable circuits
    d. Support circuit layout and post-layout simulation
    e. Prepare and participate in design reviews
    f. Develop verification plans for design work
    g. Validate circuit performance in test laboratory facilities
    h. Diagnose problems and formulate rework or redesign solution.
2. Specific design skills in increasing order of need:
    a. High speed (>10 GHz) CMOS analog/RF
    b. 10+ GS/s DAC
    c. 20+ GHz VCO and PLL
    d. 10+ GS/s ADC

Keywords: ADC, DAC, PLL, AMS, analog design, CMOS

Qualification Requirements:

- MS or PhD in Electrical Engineering with a minimum of 6 years experience or BSEE degree with at least 8 years of applicable industry experience
- Familiarity with Cadence schematic, layout, and simulation tools. Spectre, PSS, noise, jitter analysis
- Experience working in a commercial IC development team
- Experience with IC engineering life cycle (system definition, system architecture, simulation, circuit design, reliability, test validation)